TPS65930/TPS65920 OMAP™ Power-Management and System Companion Devices Silicon Revision 1.2

Version D

Technical Reference Manual

Literature Number: SWCU052D
October 2008–Revised June 2010

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About This Manual

This technical reference manual provides information about the TPS65930 and TPS65920 integrated power-management devices (in addition, the TPS65930 provides audio coder/decoder (codec) functions.

The TPS65930 and TPS65920 devices are variants of the TPS65950. The TPS65950 has functions that are not available in the TPS65930 and TPS65920 because of their reduced package pin count. Internally (in the silicon), the TPS65930 and TPS65920 are almost identical to the TPS65950 and as a result they share the same register structure and mechanisms.

In this manual, when both devices are described, this is made clear, and "device" and "devices" refer to the TPS65930 and the TPS69520. When one devices is described, this is made clear, and "device" is used.

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History

The following table summarizes the TPS65930/20 OMAP Power Management and System Companion Device TRM versions.

Version	Literature Number	Date	Notes
*	SWCU052	October 2008	See (1)
A	SWCU052	November 2008	See (2)
B	SWCU052	April 2009	See (3)
C	SWCU052	April 2009	See (4)
D	SWCU052	May 2010	See (5)

(1) *TPS65930/TPS65920 OMAP Power Management and System Companion Device Silicon Revision 1.0* - SWCU052 - inital release

(2) *TPS65930/TPS65920 OMAP Power Management and System Companion Device Silicon Revision 1.0* - SWCU052A
- Chapter 13: Audio

(3) *TPS65930/TPS65920 OMAP Power Management and System Companion Device Silicon Revision 1.0* - SWCU052B Chapters impacted by changes between version A and version B:
- Chapter 5: Resets and Power Management

(4) *TPS65930/TPS65920 OMAP Power Management and System Companion Device Silicon Revision 1.0* - SWCU052C - Chapters impacted by changes between version B and version C:
- Chapter 12: Thermal Shutdown and Hot-Die Detector

(5) *TPS65930/TPS65920 OMAP Power Management and System Companion Device Silicon Revision 1.2* - SWCU052D - Chapters impacted by changes between version C and version D:
- Chapter 1: Introduction
- Chapter 3: Clocks
- Chapter 5: Resets and Power Management
- Chapter 6: Power Resources

Introduction

This chapter introduces the setup, components, and feature sets of the TPS65930 and TPS65920 power-management devices (with the TPS65930 providing audio coder/decoder [codec] capability) and provides a high-level view of their architecture.

Topic **Page**

1.1 Overview

The TPS65930 and TPS65920 are integrated power-management devices (with the TPS65930 providing audio codec functions) for use in portable designs that derive their power from batteries based on Li-ion, Li-ion polymer, or manganese-cobalt chemistries. The devices typically receive commands from an application processor or a modem and, as shown in Section 1.1.1, *Features*, Figure 1-1, and Figure 1-2, provide power conversion/regulation (with the TPS65930 including an audio codec). In addition to generic support capabilities, the devices meet the power requirements of the TI OMAP3430 and OMAP2430C devices.

1.1.1 Features

- Power:
  - Two efficient stepdown converters for processor cores
  - One efficient stepdown converter for input/output (I/O) power
  - SmartReflex™-compliant dynamic voltage management for the processor core
  - Two low-dropout (LDO) regulators for phase-locked loops (PLLs) and digital-to-analog converter (DAC)
  - Three miscellaneous linear regulator supplies for peripherals
- Audio:
  - Voice codec
  - 15-bit linear codec (8 kHz/16 kHz)
  - Differential input microphone
  - 8-Ω stereo class D drivers
  - Time-division multiplexing (TDM) interfaces
  - Automatic level control (ALC) function
  - Ability to mix paths in digital and analog domains
  - 16-bit linear audio stereo DAC (96 kHz, 48 kHz, 44.1 kHz, 32 kHz, and derivatives)
  - 16-bit linear audio stereo analog-to-digital (ADC) converter (48 kHz, 44.1 kHz, 32 kHz, and derivatives)
  - PLL for audio codec with 256*Fs or 128*Fs generation
  - Carkit (CEA-936A)
- Universal serial bus (USB):
  - USB 2.0 OTG-compliant high-speed (HS) transceivers
  - 12-bit USB transceiver macrocell interface (UTMI)+ low pin interface (ULPI)
  - USB power supplies (5 V, 3 V)
  - Carkit-compliant CEA936

- Plus:
  - LED driver
  - Two pulse width modulation (PWM) generators, PWM0 and PWM1
  - Embedded 10-bit ADC with 2 external inputs
  - Real-time clock (RTC) module and retention modules
  - HS inter-integrated circuit (I^2C™) serial control
  - Thermal shutdown protection and hot-die detection
  - Keypad up to 6 x 6 matrix
  - 0.65 mm pitch, 10 x 10 mm package
- Applications:
  - Cellular phone, PDAs, portable music players, etc.

1.1.2 Subsystems

NOTE: Subsystem refers to a feature of the TPS65930 and TPS65920 from the standpoint of what feature is provided.

However, when the devices are examined from the standpoint of the way a feature is provided, having to do with the design, subchip is more descriptive. Thus, In many chapters, subchip is used because the discussion centers on the way the feature is provided.

The TPS65930 and TPS65920 include the following subsystems:

- Power inputs and output sourcing
- Power management
- Monitoring ADC (MADC)
- Clocks
- External interfaces/control
- Audio (TPS65930 only)
- Security
- Overheating protection

The subsystems and their features are described in the following sections. Figure 1-1 is a block diagram of the TPS65930. Figure 1-2 is a block diagram of the TPS65920.

Figure 1-1. TPS65930 Block Diagram

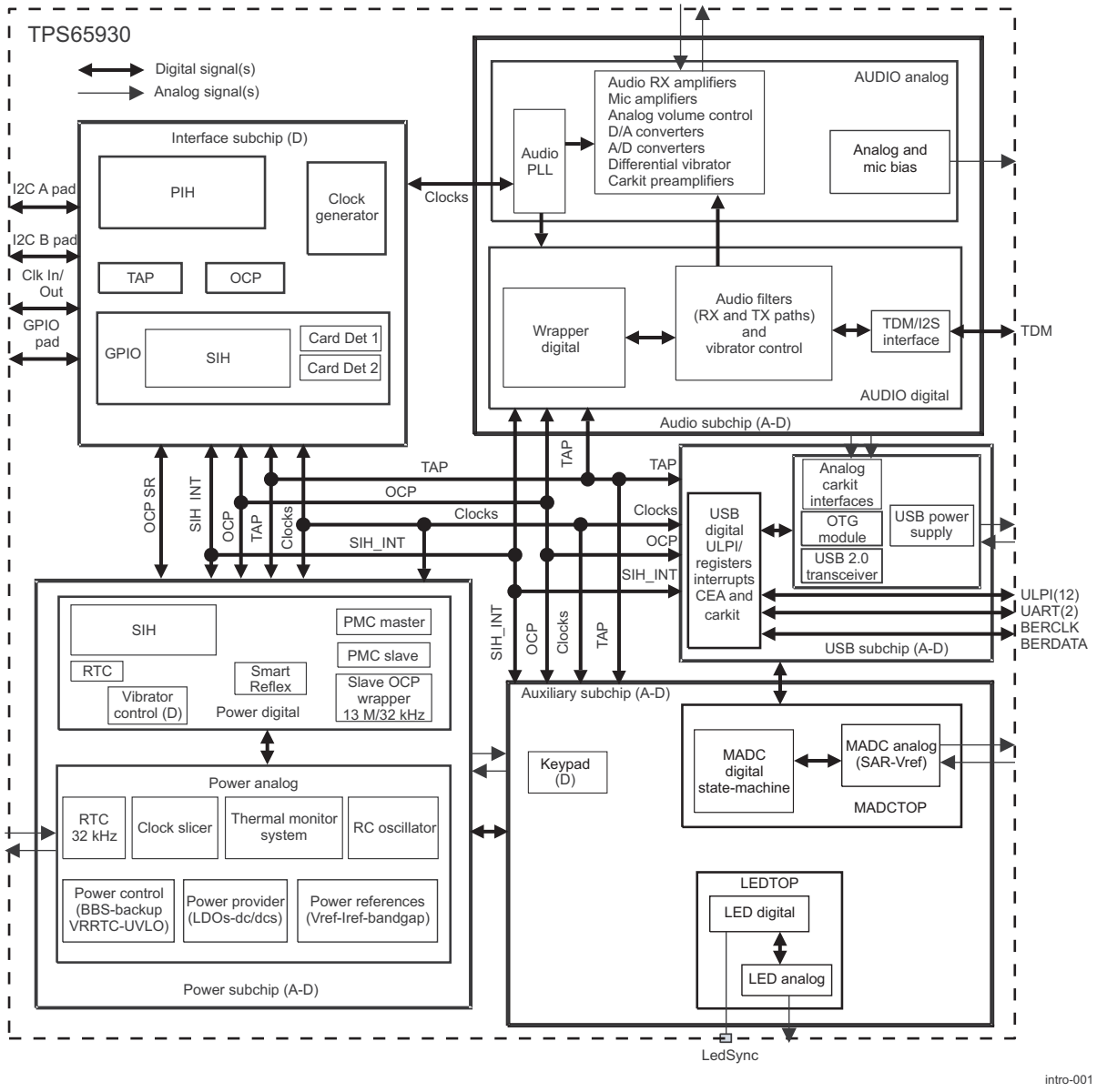
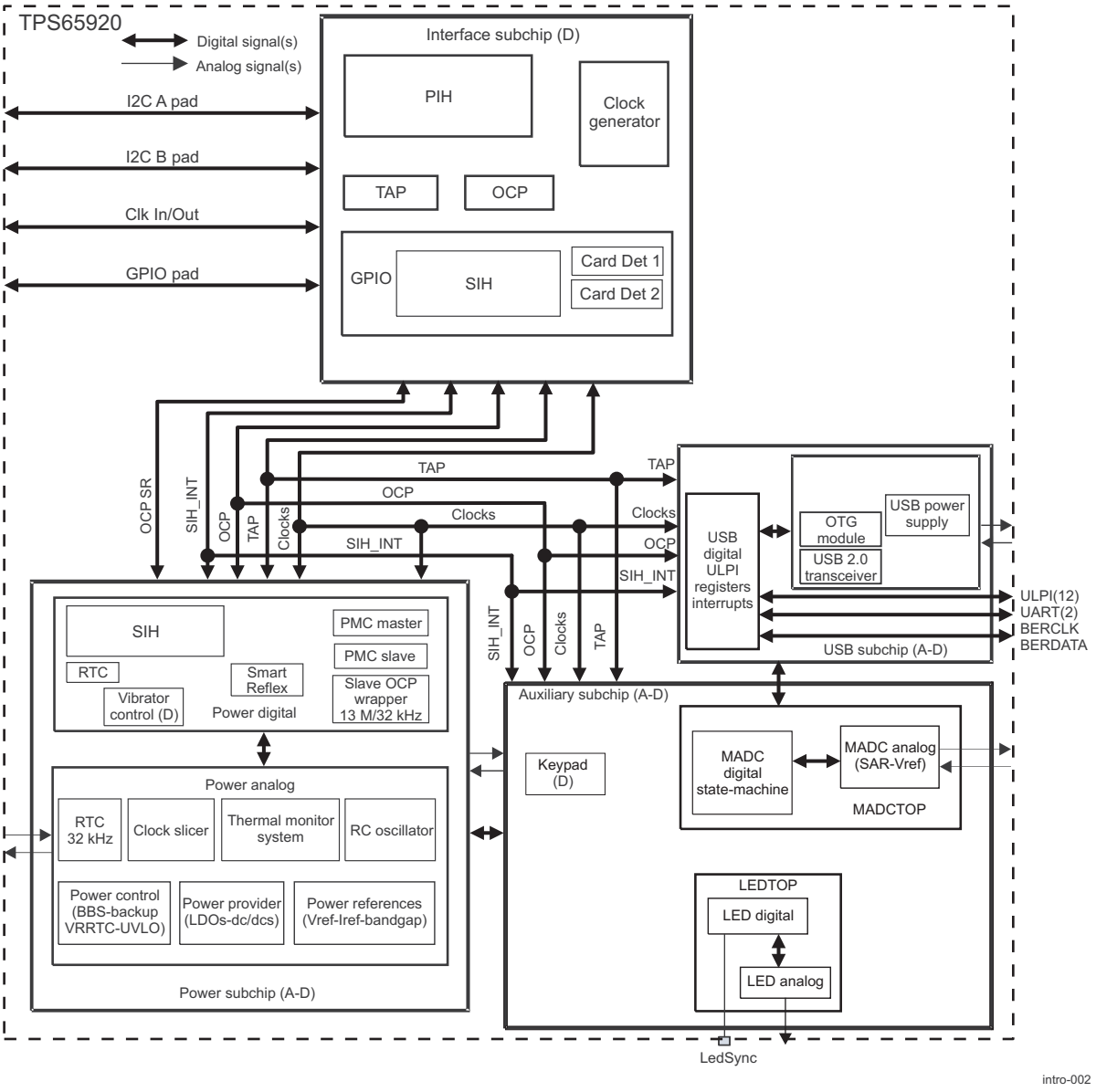


Figure 1-2. TPS65920



1.2 Power Input and Output Sourcing

The devices operate from an external power source (typically a battery) and have several switching and linear regulators to provide power to various devices.

1.2.1 Battery Interface

The devices operate from a DC input that is typically supplied by a battery.

1.2.1.1 Batteries

The battery powers all the internal logic and regulators of the devices.

1.2.1.2 Battery Characteristics

Table 1-1 lists the battery interface characteristics.

Table 1-1. Battery Interface Characteristics

Parameters	Value
Input voltage	0 V to 4.5 V
Protection	2.1 V

1.2.2 Power Resources

1.2.2.1 Switch-Mode Power Supplies

The devices contain three switch-mode power supplies (SMPS):

- VDD1: 1.2-A, buck DC/DC converter (V_{OUT} = 0.6 V to 1.45 V, in steps of 12.5 mV)
- VDD2: 600-mA buck DC/DC converter (V_{OUT} = 0.6 V to 1.45 V, in steps of 12.5 mV, and 1.5 V as a single programmable value)
- VIO: 600-mA buck DC/DC converter (V_{OUT} = 1.8 V or 1.85 V)

1.2.2.2 Linear Voltage Regulators

Several LDO linear voltage regulators are integrated in the devices. These regulators supply power to internal analog and digital circuits, to the digital baseband counterpart, and to external components. Most LDOs have short-circuit protection and an external decoupling capacitor between the output terminal and ground. For more information, see Chapter 6, *Power Resources*.

1.2.2.3 VDAC LDO

The VDAC LDO is a high-power supply rejection ratio (PSRR), low-noise, LDO, programmable linear regulator that powers the host processor dual-video DAC. For more information about this power resource, see Chapter 6, *Power Resources*.

1.2.2.4 VPLL1 LDO

The VPLL1 is a programmable linear LDO that offers high-PSRR, low-noise performance. It is used for the host processor PLL supply. For more information about this power resource, see Chapter 6, *Power Resources*.

1.2.2.5 VMMC1 LDO

The VMMC1 LDO is a programmable linear voltage converter that powers multimedia card (MMC) slot 1. For more information about this power resource, see Chapter 6, *Power Resources*.

1.2.2.6 VAUX2 LDO

The VAUX2 is a general-purpose (GP) LDO that powers auxiliary devices.

1.2.2.7 Internal LDOs

Three LDOs supply the devices' internal systems: one for the digital block (VINTDIG) and two for the analog blocks (VINTANA1 [1.5 V] and VINTANA2 [2.75 V/2.5 V]). The 2.5-V setting is selected when the battery voltage falls below 3.0 V.

1.2.2.8 VRRTC Regulator

The voltage regulator VRRTC is a programmable LDO linear voltage regulator that supplies 1.5 V to the embedded RTC (32.768-kHz oscillator) and dedicated I/Os of the digital host counterpart. The VRRTC also supplies the power-management digital state-machine.

1.2.2.9 USB Charge Pump

The USB charge pump can power some circuitry from the USB line when battery voltage is low.

1.3 Power Management

The devices have an internal power-management controller that provides close control of system battery resources and device thermal management (ensuring that the devices do not overheat). The controller responds to internal hardware and external software inputs (registers configured by the host processor through the I^{2}C™ bus).

The power-management controller controls the devices in a series of operating modes that define how device subsystems are operated, including which regulators providing power to external devices are turned on:

- No supply: The system is not powered by a battery.
- Wait-on: A subsystem is powered by the battery and maintains only the VBRTC and VRRTC supplies. It can accept switch-on requests.
- Active: A subsystem is powered by the main battery, all supplies are enabled and full-current capable, internal reset is released, and the associated processor is running.
- Sleep: A subsystem is powered by the main battery, selected supplies are enabled in low-consumption mode, and the associated processor is in low-power mode.

1.4 MADC

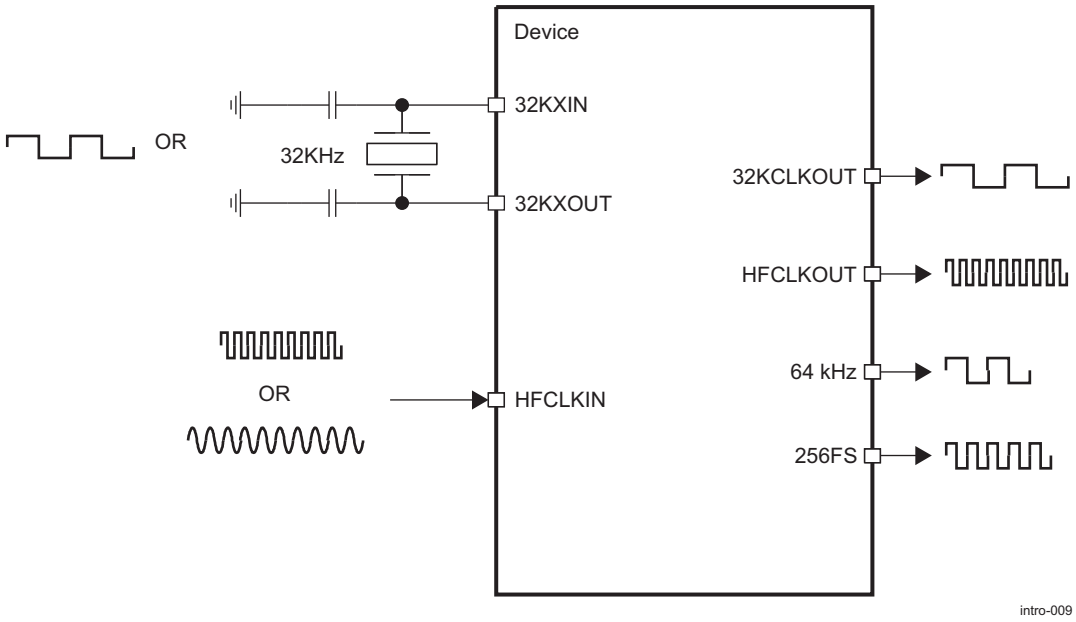
The MADC subsystem in the device consists of a 10-bit ADC combined with a 6-input analog multiplexer. It is used as a GP ADC subsystem that is shared by two external processors (modem and applications) and the USB subchip.

Two of the inputs are GP and are available externally. The remaining four MADC inputs are in the device and are dedicated to measurements of battery voltage, USB VBUS voltage, USB measurement (VRUSB supply), and right speaker polarization level. The two inputs with external access are ADIN0 and ADIN2. ADIN0 is configured to measure currents, and ADIN2 is for measuring voltages.

1.5 Clocks

As shown in Figure 1-3, the device requires a high-frequency clock and a 32-kHz clock to operate.

Figure 1-3. Clocks



1.5.1 External High-Frequency Clock

The device derives its overall synchronization from an externally supplied high-frequency clock signal (HFCLKIN) that can be 19.2, 26, or 38.4 MHz (26 MHz is preferred in some applications, because certain features of the audio subsystem are not otherwise available; for details, see Chapter 13, *Audio*).

HFCLKIN goes into a signal slicer that works with analog (sine) and digital (square wave) signals. For more information about the HFCLKIN input signal amplitude, see the device data manual.

1.5.2 32-kHz Clock

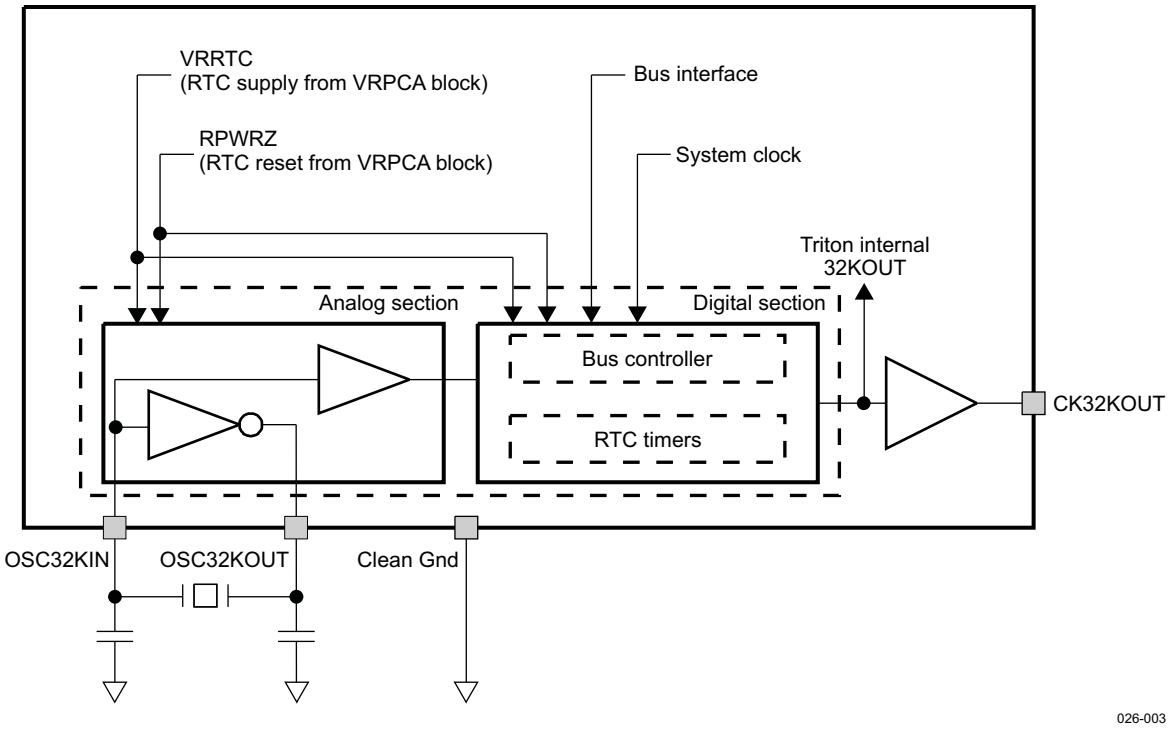
The 32-kHz clock (32.768 kHz) circuit works with an externally supplied digital signal or a quartz crystal. The 32-kHz clock drives the RTC circuitry and is kept running by the backup battery (if provided) if the main battery fails and no external power is applied. When HFCLKIN is available, the 32-kHz oscillator is synchronized with it. If HFCLKIN is not available but the device is powered, the 32-kHz oscillator synchronizes with the 3-MHz resistance/capacitive (RC) oscillators.

1.5.3 RTC

The RTC, shown in Figure 1-4, generates and maintains time for the handset and provides alarm-clock functions:

- Time information (seconds/minutes/hours) directly in binary-coded decimal (BCD) code
- Calendar information (day/month/year/day of the week) directly in BCD code up to year 2099
- Interrupt generation, periodically (1 second/1 minute/1 hour/1 day) or at a precise time (alarm function)
- 30-s time correction

Figure 1-4. RTC



1.5.4 3-MHz RC Oscillators

Internally, the device has three RC oscillators that free-run at roughly 3 MHz. These RC oscillators do not have external appearances; they are used to clock internal switching regulators. If the HFCLKIN signal is not present, the 32-kHz oscillator synchronizes with the RC oscillators if they are operating.

1.6 External Interfaces/Control

1.6.1 Keypad Interface Controller

The keypad interface controller provides an enhanced keypad decode capability and simultaneously reduces host processor software overhead.

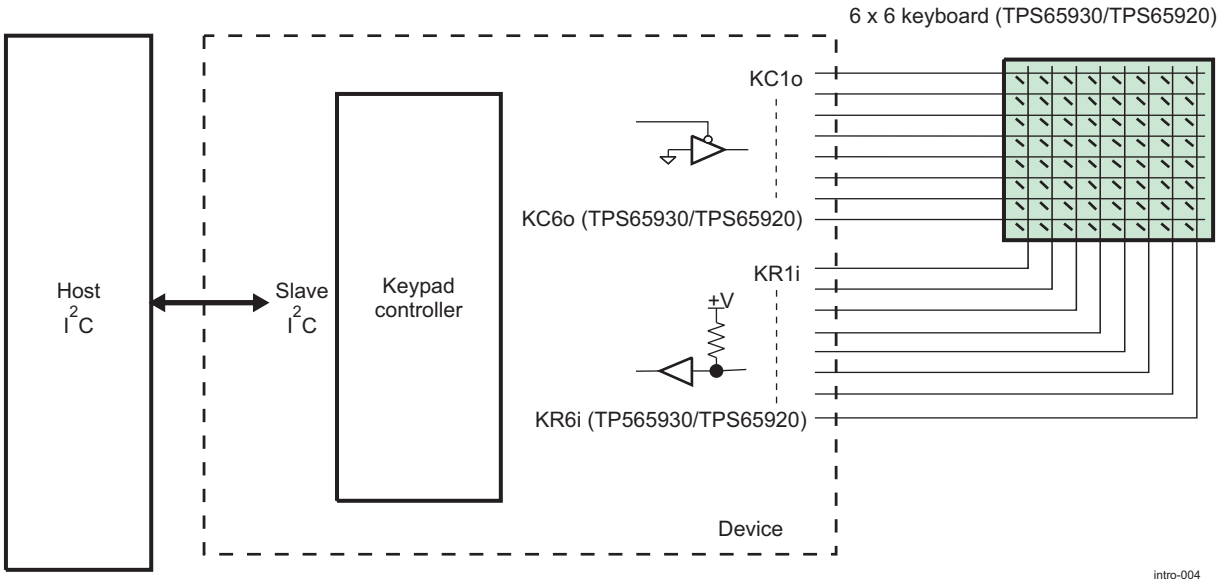
This subsystem is a stand-alone decoder that manages keypad events with hardware, as shown in Figure 1-5. It uses the 32-kHz clock in all device modes, including sleep. Features include programmable debounce time and interrupt management.

1.6.1.1 Principal Features

- Stand-alone module
- Support of multiconfiguration keypad, up to 6 columns * 6 rows
- Multiple key-press detection and decoding (two keys fully compliant but more than two with some limitations)
- Configurable
- Integrated timer with four programmable comparison values
- Three types of interrupts (IT_EVENT, IT_LONG_KEY or REPEAT_KEY, and IT_TIME_OUT)
- LONG_KEY, REPEAT_MODE, and TIME OUT detections enabled by a register
- Each interrupt enabled or disabled by register configuration
- Module generates an overrun if the host reads a register too late
- Each key coded on one bit in 8-bit registers
- Software reset capabilities

Figure 1-5 is an overview of the keypad interface controller.

Figure 1-5. Keypad Interface Controller Overview

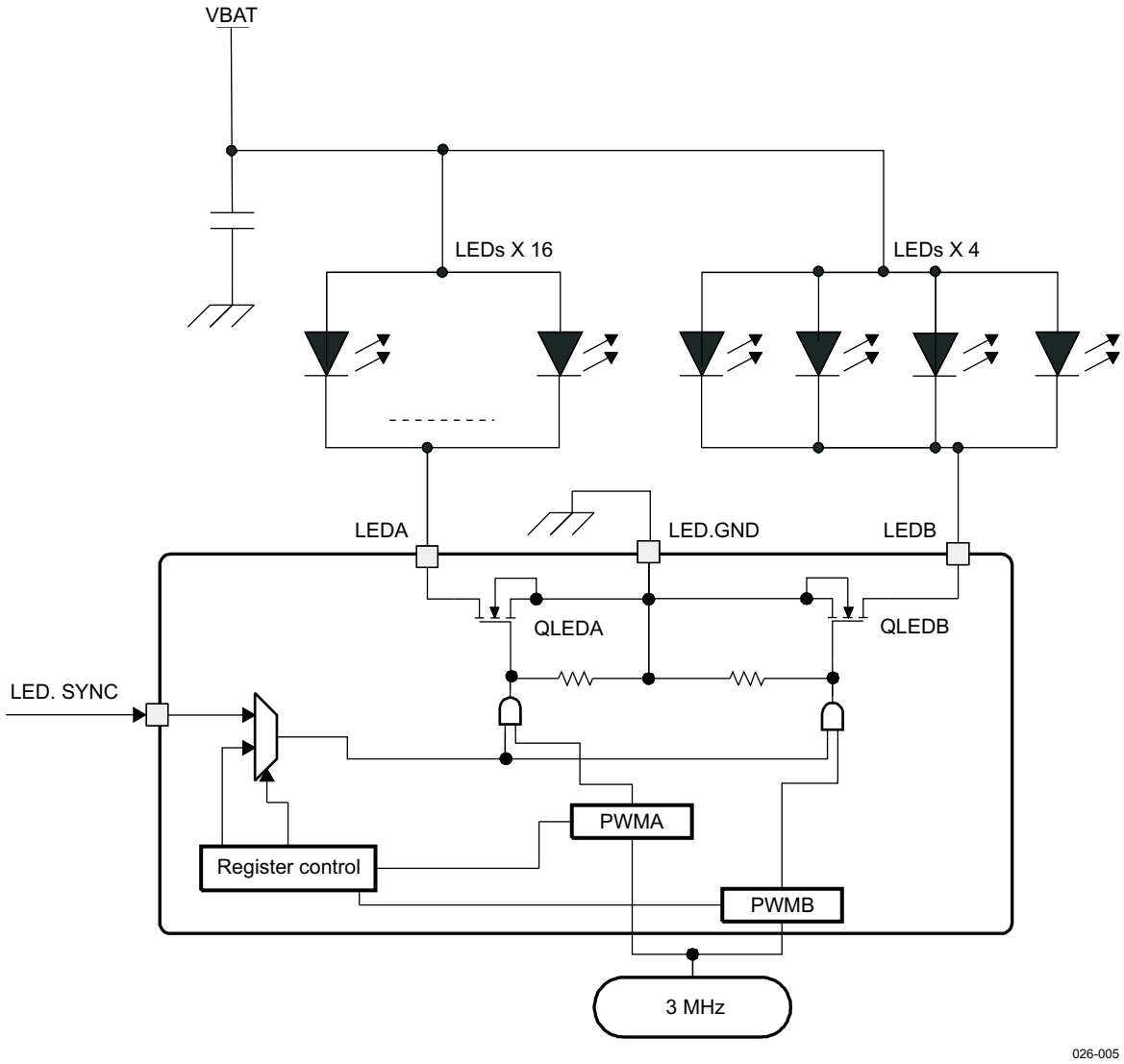


NOTE: Keyboard scan lines and keyboard size are for illustration and do not necessarily represent all devices described in this document.

1.6.2 LED Driver

The device provides LED driver circuitry (as shown in Figure 1-6) to power two LED (DC power) circuits that can illuminate a panel or provide user indicators. The first circuit can provide up to 160 mA and the second, 50 mA. Each LED circuit is independently controllable for basic power (on/off) control and illumination level (using PWM). Figure 1-6 is a block diagram of the LED driver.

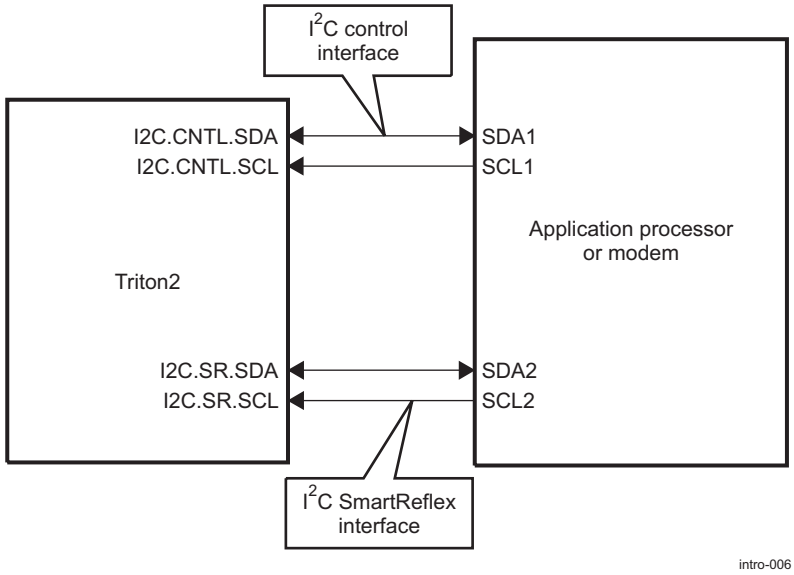
Figure 1-6. LED Driver Block Diagram



1.6.3 I^2C Control Interface

As shown in Figure 1-7 the device is controlled externally through two I^2C HS interfaces. One interface accesses the main control/configuration registers in the device and the other is dedicated to the power module SmartReflex capability. Figure 1-7 shows the I^2C interfaces.

Figure 1-7. I²C Interfaces



1.6.3.1 I²C Bus Compliance/Features

The I²C control interface has the following features:

- Complies with Philips I²C specification v2.1
- I²C slave only (receiver and transmitter)
- 7-bit device addressing mode with repeated start condition
- Decoding of five I²C slave addresses
- I²C standard mode (100 Kbps), fast mode (400 Kbps), and HS mode

1.6.3.2 Control Register Access

Functions are controlled using the I²C bus to program internal registers. The registers are clustered in five register address groups with each group containing 256 registers (each having 8 bits). Four groups are for general device controls and one is for SmartReflex power control.

1.6.4 I2S TDM Interface

The I2S TDM interface is the digital audio interface between the host processor and the device. For more information, see Section 1.7, *Audio Subsystem*.

1.6.5 GPIOs

The device has 6 digital GP input/output (GPIO) lines.

When configured as input, activity on a GPIO line can generate a register-programmable (selectable polarity) interrupt (INT1) that can be seen by the host processor. This interrupt can be configured through a register to clear-on-read (COR) or clear-on-write.

Because of physical limitations on device size, most GPIO lines share external access with other functions (through multiplexing), so there can be instances when some GPIOs are not available.

1.6.6 USB Interface

The device includes a USB OTG transceiver with a Consumer Electronics Association (CEA) interface, that can support USB 480 Mbps HS, 12 Mbps full-speed (FS), and USB 1.5 Mbps low-speed (LS) through a 4-pin ULPI.

1.6.6.1 Features

The USB interface includes a 5-V-tolerant USB 2.0 HS transceiver fully compliant with the following standards:

- *USB 2.0 Specification*:
  - 5-V-tolerant data-line at HS/FS, FS-only, and LS-only transmission rates
  - 7-V-tolerant VBUS line with internal 100-mA VBUS power supply
  - Integrated data-line serial resistors, requiring an external 1-percent calibration resistor
  - On-chip 480 MHz PLL from the internal system clock (12, 13, 19.2, or 38.4 MHz)
  - SYNC/EOP generation and checking
  - Data and clock recovery from USB stream
  - Bit stuffing/unstuffing and error detection
  - Resume signaling, wakeup, and suspend detections
  - USB 2.0 test modes
- *OTG Supplement* to the *USB 2.0 Specification*:
  - D+/– and VBUS pulsing session request protocol (SRP)
  - HNP commands and status registers
  - 5-V tolerant ID line with float/ground comparator
  - VBUS OTG comparators
- *CEA-2011 OTG Transceiver Interface Specification:*
  - 3-pin LS/FS serial mode (DAT_SE0)
  - 4-pin LS/FS serial mode (VP_VM)
- *CEA-936 Mini-USB Analog Carkit Interface Specification*:
  - 5-pin CEA mini-USB analog carkit interface
  - Universal asynchronous receiver/transmitter (UART) signaling (from 1.2 Kbps to 115.2 Kbps)
  - Audio (mono/stereo) signaling
  - UART transactions during audio signaling
  - Basic and smart 4-/5-wire carkit/chargers/accessory devices
  - ID CEA-resistor comparators
- *USB 2UTMI+ Specification.0 Transceiver Macrocell Interface (UTMI) Specification*
- *UTMI+ Specification*
- *UTMI+ Low Pin Interface (ULPI) Specification*:
  - 8-pin ULP interface with 4-pin parallel data for USB signaling and register access
  - 60-MHz clock generation
  - Register mapping

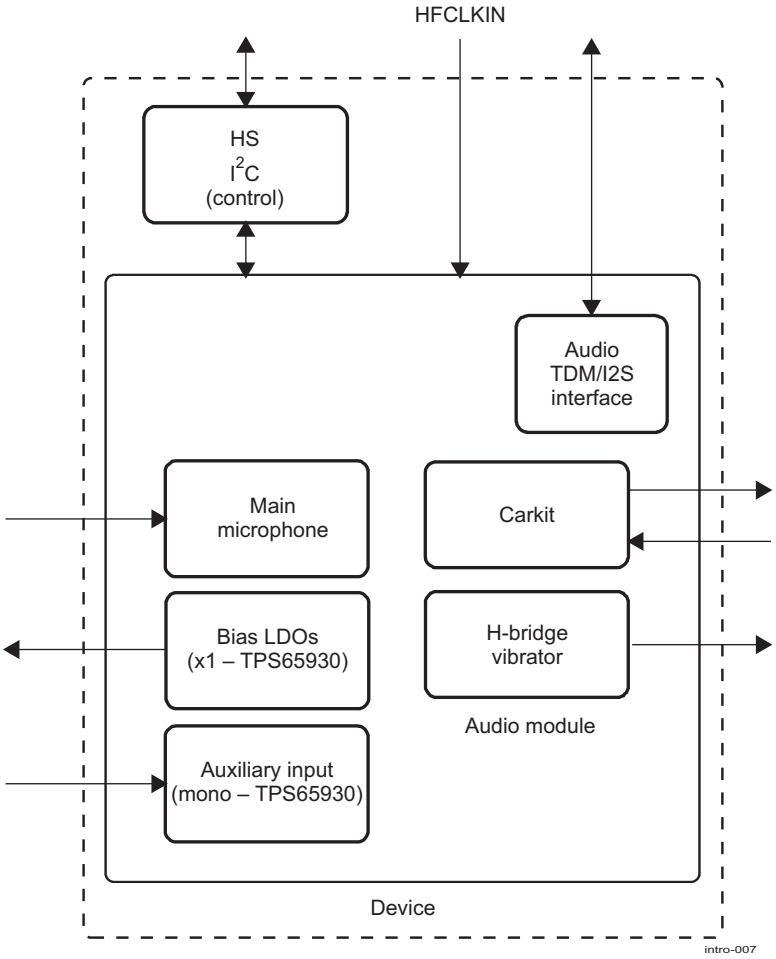
1.6.7 Vibrator Driver Output (Call Annunciator)

The audio subsection of the TPS65930 contains a differential amplifier, H-bridge, that can drive a vibrator under the control of a pulse-width modulator activated by the I^2C bus. The TPS65920 does not provide vibrator functionality.

1.7 Audio Subsystem (TPS65930 Only)

As shown in Figure 1-8, the TPS65930 contains numerous audio capabilities, including digital and analog inputs and outputs, and support for analog microphones. It is connected to a host processor through the TDM/I2S interface (audio). The audio subsystem is controlled by internal registers accessed by the HS I^2C control interface.

Figure 1-8. Device Audio Subsection



1.7.1 Audio TDM/I2S Interface

The TDM/I2S interface is used between the host processor and the device to send and receive audio data from an 8-kHz to a 48-kHz sampling rate, with four channels per frame and 16 or 32 bits per sample; supported frequencies are 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, and 48 kHz. A 96-kHz sampling rate is also available for receive audio data from the host processor, but the transmit audio data path from the device is inactive.

1.7.2 Output Stages

The audio subsystem includes the following output stages:

- Predriver output signals for external class-D amplifiers (single-ended)
- Mono/stereo preamplifier output signals for CEA carkit
- Vibrator H-bridge

1.7.3 Input Stages

The audio subsystem includes the following input stages:

- Main differential microphone input
- Single-ended auxiliary input (FM radio)
- CEA carkit enters the device USB block through the design-in (DIN) pin (single-ended).

1.7.4 Other Features

- The audio subsystem performs the programmable gain, volume control, and side-tone functions for the uplink and downlink path of the voice codec.
- Two analog microphone-biasing LDOs
- Hardware dual-tone multiple frequency (DTMF)/tone generator
- Soft volume for audio RX path
- Data scramble function for I2S data received
- Bass boost functions in one stereo audio RX path
- ALC: A limiter function that prevents loud sounds from overloading the ADC, while amplifying low-level sounds. The ALC is available only for the main microphone and the submicrophone.

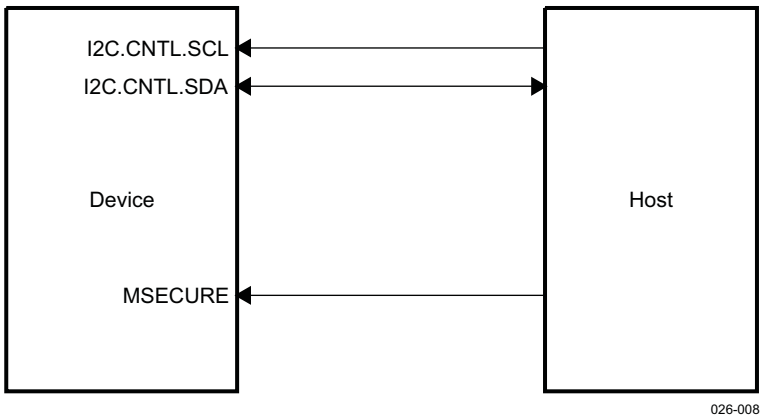
1.8 Security

Certain device components can be protected by restricting access to some internal registers to software running in the secure mode of the host. The following components or actions can be protected:

- All RTC registers
- 160 bits of memory in the backup domain (hash table)
- Degating of the 32.768-kHz output clock
- Degating of the HFCLKOUT output clock

The access protection activation of the device is defined by the level on its input MSECURE. This signal is driven by the device host. Figure 1-9 shows the MSECURE signal.

Figure 1-9. MSECURE Signal



NOTE: For every read operation of the calendar registers, the user must set GET_TIME to 1 prior to the read operation.

When in secured mode, writing to the RTC data registers and to the hash table is prevented, but read access is allowed. When in nonsecured mode, any access is allowed to the RTC registers and hash table.

1.9 Overheating Protection

The device has protective circuits that prevent it from being damaged by overheating.

1.9.1 Thermal Shutdown Detector

The thermal shutdown detector monitors the device junction temperature, as shown in Table 1-2. If the junction reaches a temperature (rising-edge threshold) at which damage can occur, all regulators are disabled by hardware, and thermal shutdown information is written to a status register. All internal registers are reset except the registers in the backup domain. While the device junction temperature remains higher than the hot-die falling-edge threshold, the device cannot be restarted. Inhibiting restart by using the hot-die falling-edge threshold, instead of using the thermal shutdown falling-edge threshold, prevents the possibility of instability.

When the junction temperature falls below the hot-die falling-edge threshold, the device can be restarted. The restart mechanism is register-configurable to be automatic or to require an external command. The thermal shutdown circuitry is always enabled, except in backup mode.

Table 1-2. Thermal Shutdown Thresholds

THERM Shutdown	Threshold (Nominal)
Enable	Rising temperature: 150°C
	Falling temperature: 140°C

1.9.2 Hot-Die Detector

The hot-die detector monitors the device junction temperatures for lower temperatures than does the thermal shutdown detector. Unlike the thermal shutdown detector, the hot-die detector does not shut down the device, but instead provides an early warning to the host processor to avoid excessive power dissipation (by the host processor reducing the power the device is delivering) to prevent a thermal shutdown. The adjustment of the hot-die detector is set several degrees below the thermal shutdown threshold, and there are three temperature ranges.

1.10 Distinguishing Between the TPS65930 and TPS65920 Silicon Versions

Table 1-3 lists the content of the device IDCODE.

Table 1-3. IDCODE Definition

IDCODE Bits	Content
31:28	Silicon version number
27:12	Part code number
11:1	Manufacturer code
0	Least-significant bit (LSB)

The TPS65930 and TPS65920 IDCODE is 0x0009802F.

NOTE: The IDCODE field cannot be read correctly using the I^2C interface (need JTAG access to read the complete IDCODE correctly). The IDCODE read back usbing the I^2C will have the value 0x1009 002F.

This information is split onto four 8-bit registers, as shown in Table 1-4. See Table 2-27 in Chapter 2, *Control Interface*, for information about the IDCODE registers and their access limitations.

Table 1-4. IDCODE Device Identification Registers

Register	Physical Address
IDCODE_31_24	0x0000 0085
IDCODE_23_16	0x0000 0086
IDCODE_15_8	0x0000 0087
IDCODE_7_0	0x0000 0088

Table 1-5 lists the device silicon version number according to the value in the IDCODE_31_24[7:0] register.

Table 1-5. Silicon Version Number

Silicon Version Number	IDCODE_31_24[7:0] Register Value
ES 1.0	0x00
ES 1.1	0x10
ES 1.2	0x30

Table 1-6 lists the device part number according to the values in the IDCODE_23_16[7:0] and IDCODE_15_8[7:0] registers.

Table 1-6. Part Number

Device	Part Code Number	IDCODE_23_16[7:0] Register Value	IDCODE_15_8[7:0] Register Value
TPS659xx	0x0098	0x09	0x80

NOTE: When accessed through the I^2C, the part code number has no meaning.

Control Interface

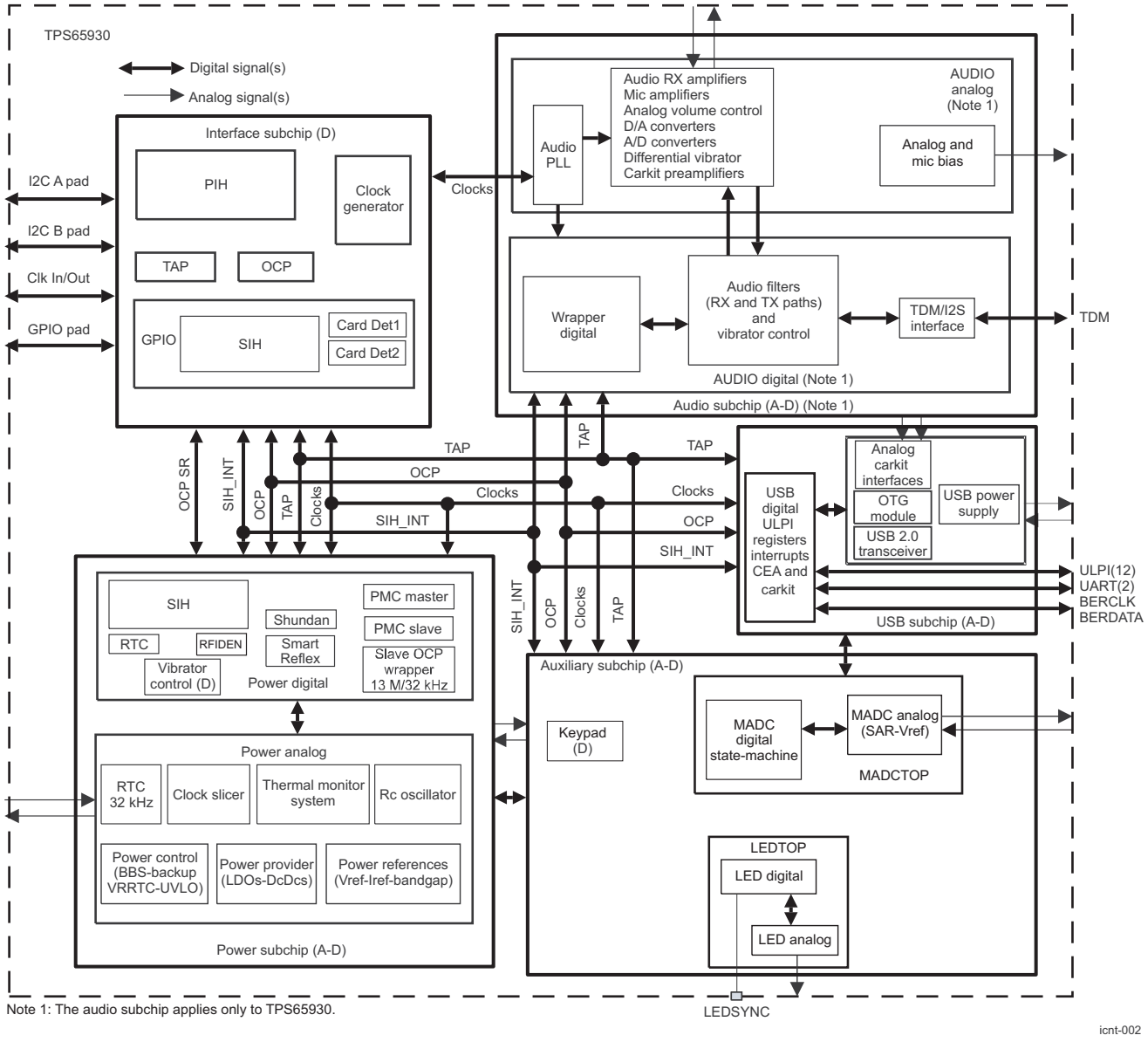
This chapter describes the control interface of the integrated power-management/audio coder/decoder (codec) devices.

Topic **Page**

2.1 Control Interface Overview

With the exception of the power-on and reset control lines (see Chapter 5, *Resets and Power Management*), the device is controlled through two inter-integrated circuit (I^2C) buses. The registers in the device are set to select the configurable characteristics. As shown in Figure 2-1, the open-core protocol (OCP) is used for communication within the device, but the I^2C-OCP conversion process is transparent. From an external perspective, the device registers are directly accessed by the I^2C buses.

Figure 2-1. Internal Control Communication



Note 1: The audio subchip applies only to TPS65930.

icnt-002

2.2 Control Interface Environment

The device uses two I²C buses to provide the control interface (see Figure 2-2).

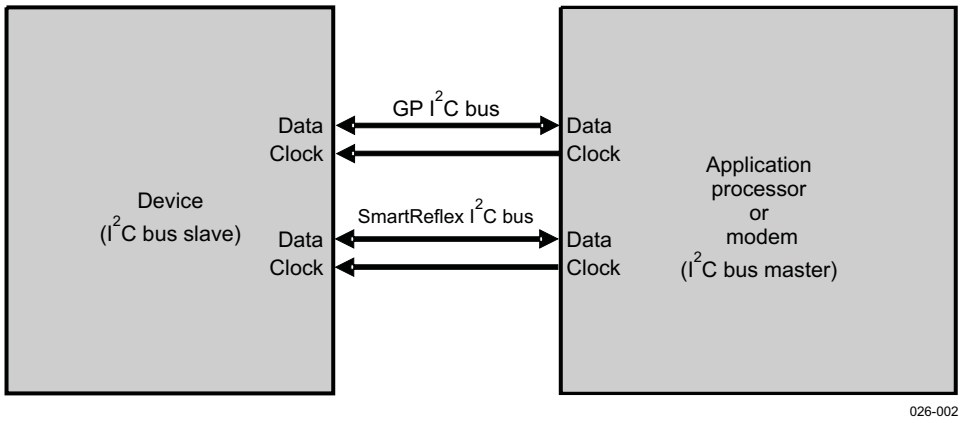
2.2.1 General-Purpose I²C Bus

The general-purpose (GP) I²C bus is the control interface for all device control functions, except SmartReflex™ technology functions. 3KΩ ±30% pullups are available in the GPPUPDCTR1 register (see Table 2-28). For more information about the use of pullups, see the device *Data Manual*.

2.2.2 SmartReflex I²C Bus

The SmartReflex I²C bus is the control interface for device SmartReflex power-management applications. Figure 2-2 shows the I²C bus external control. 3KΩ ±30% pullups are available in the GPPUPDCTR1 register (see Table 2-28). For more information about the use of pullups, see the device *Data Manual*.

Figure 2-2. I²C Bus External Control



2.2.3 I²C Bus Compliance

In accordance with standard I²C practice, each I²C bus in the device consists of a serial data (SDA) line and a serial clock (SCL) line, for a total of four lines: the data and clock lines for the GP I²C bus, and the data and clock lines for the SmartReflex I²C bus. Table 2-1 lists additional I²C features.

Table 2-1. I²C Bus Compliance

Supported	Not Supported
Complies with Philips I²C specification v2.1	General call
Slave only (receiver and transmitter)	Master mode (bus arbitration and clock generation)
Standard mode (100 Kbps), fast mode (400 Kbps), and high-speed mode up to 3.4 Mbps at 38.4-MHz system clock	10-bit device addressing mode
4 I²C ID slave-addressing decoding feature	
7-bit device addressing mode	

2.2.4 I²C Bus Performance Versus Device System Clock Frequency

The I²C module (the circuitry that provides the I²C capability) is driven by the device system clock. The maximum theoretical performance (bandwidth) of the I²C is 3.4 MHz for the three system clock rates that are supported (19.2, 26, and 38.4 MHz).

2.2.5 I²C Bus Addressing

GP I²C bus addressing uses four hard-coded addresses that cannot be changed:

I²C Address Group	Address
ID1	48 hex
ID2	49 hex
ID3	4a hex
ID4	4b hex

SmartReflex I²C bus addressing uses one hard-coded address that cannot be changed:

I²C Address Group	Address
ID5	12 hex

Each I²C address group allows access to a 256-byte register address map through which internal registers are accessed.

For a cross-reference of the device registers to the address groups, see Section 2.6.1, *I²C Address Groups – Cross-Reference*.

2.3 Control Interface Integration

Device register addressing differs from device I²C bus addressing. The two I²C buses in the device comply with I²C bus standards, but more than compliance is involved in addressing the device registers.

2.3.1 Register Addressing Versus I²C Bus Addressing

The I²C data protocol describes how to use a common bus to send and receive information between a master device and a slave device, but the standard does not specify what type of data is communicated or how it is used. Understanding the I²C protocol lets data be sent to (and, in some instances, received from) the device, but understanding how the device interprets the received data ensures that the device understands the commands issued by the I²C bus master device.

2.3.2 Register Addressing Using the I²C Buses

Device registers are clustered in five register address groups (ID1, ID2, ID3, ID4, and ID5). Each group can contain up to 256 registers. A specific register is accessed by first selecting its register address group. Then the register address in the group is selected using an 8-bit byte (this also fixes the maximum number of registers in each address group; 8 bits can uniquely identify 256 addresses).

Although I²C bus operation is not discussed in detail here, some general information about the operation helps explain how device registers are addressed.

I²C is a byte-by-byte protocol. Data is sent in 8-bit bytes, and the sending device must receive an acknowledgement (ACK) from the receiving device after each byte.

When an I²C bus master sends data, it first seizes the bus by issuing a START condition, then sends out the I²C address of the device for which the information is intended. In the 8-bit (1-byte) I²C address word, the least-significant bit (LSB) indicates whether the I²C operation that is starting is a read process or a write process.

2.4 Control Interface Functional Description

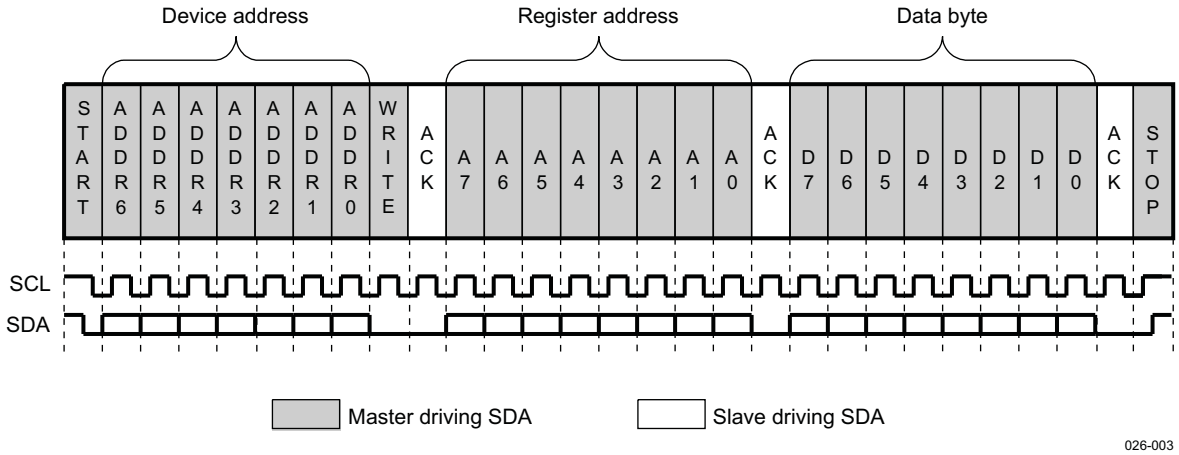
The processes of writing and reading device register data using I²C buses can be divided into two categories of operations: dealing with controls that require 8 bits or fewer and dealing with controls that require more than 8 bits. Internally, device registers are always 8 bits wide. When a control requires more than 8 bits, two or more registers secure the necessary number of bits.

2.4.1 Writing 8 Bits to a Device Register

When the I²C bus master writes 8 bits of data to a device register (see Figure 2-3), the I²C transmission is immediately identified (through the LSB in the I²C address byte) as a write operation. Following standard I²C protocol, the address byte is then followed by a data byte that the device interprets as the address of a particular register in the register address group that was initially addressed by the I²C address byte. The I²C bus master then sends a second I²C data byte, which the device loads in the register that was addressed. The command to the device is executed when the specified internal register is loaded with the correct value (the device acknowledges the byte immediately before loading the register).

The I²C bus recognizes an I²C device addressed and 2 data bytes sent to that address. The device recognizes one of its I²C register address groups addressed, a particular register (in the already-addressed register address group) addressed, and 8 bits of information loaded into the addressed register. Figure 2-3 shows an 8-bit I²C write access.

Figure 2-3. 8-bit I²C Write Access



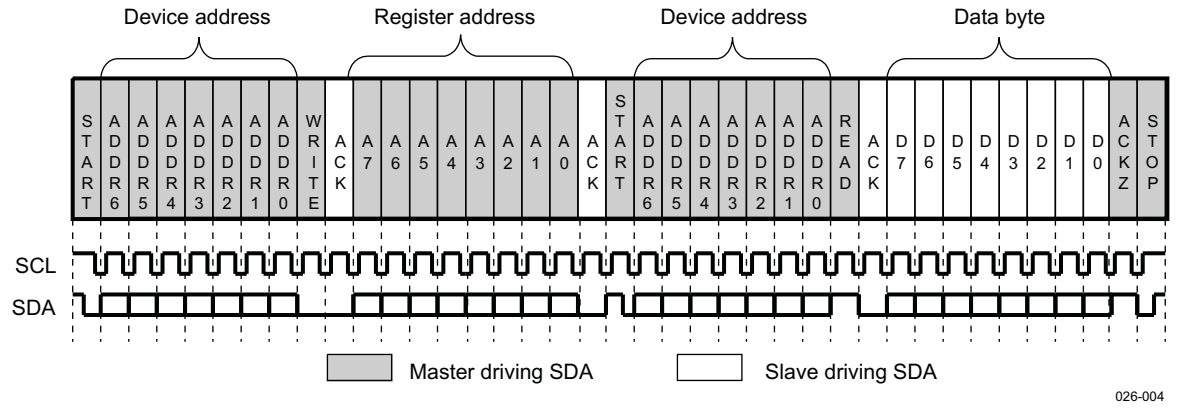
2.4.2 Reading 8 Bits From a Device Register

When the I²C bus master reads 8 bits of data from a device register (see Figure 2-4), the I²C bus master transmission is first identified (through the LSB in the I²C address byte) as a write operation so that the affected device register address group is accessed. Instead of immediately following with a data byte (as when writing to a device register), however, the I²C bus master sends out another START condition. Then another I²C address byte is sent, but this byte is for the particular register in the device in the register address group that the first I²C address byte addressed.

The I²C bus master sends a second I²C START condition/second I²C address so that the second I²C address lets its read/write bit (LSB) be set to read. The device register thus knows to read out its value to the I²C bus.

The I²C protocol allows for multiple START signals to be sent to address a device register that is to have its value read. With an I²C bus master, the first byte sent after a START command is always viewed as an I²C address byte, and the LSB in that byte is the read or write (R/W) indicator. Therefore, when a device register is to be read, the correct device register address group must be addressed with an I²C address identified as a write operation (to select that device register address group). Then a second I²C address must be sent to address the particular device register, but with the R/W bit set to read so that the device responds with the register value. Figure 2-4 shows an 8-bit I²C read access.

Figure 2-4. 8-Bit I²C Read Access



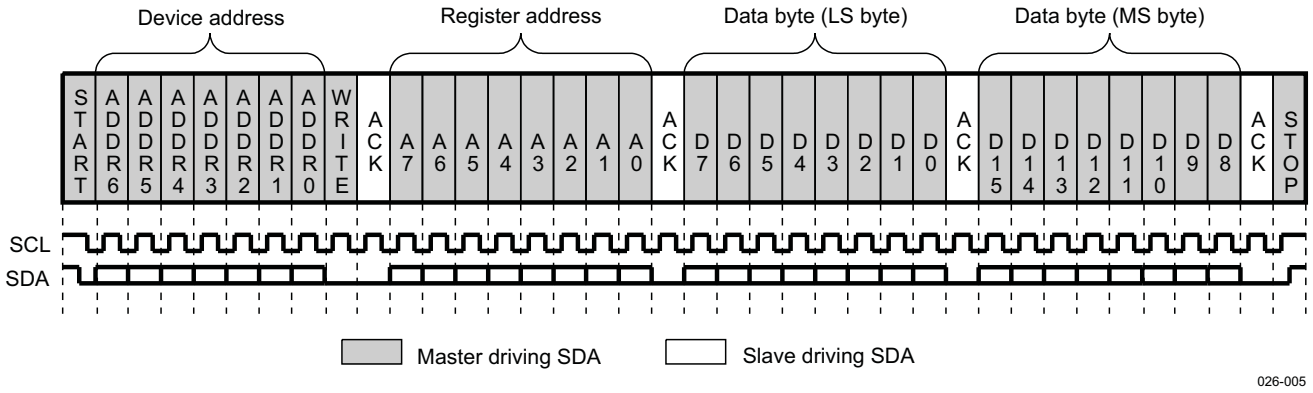
2.4.3 Additional Device Register Addressing Modes

The register-addressing scheme in the device allows for enhanced methods that provide the ability to write to or read from multiple adjacent registers with simplified I²C signaling.

2.4.3.1 16-Bit Write Register Access

When writing data to two adjacent device registers (in the same register address group and having relative addresses of *n* and *n* + 1) (see Figure 2-5), the same technique is used as when writing to an 8-bit address, except that after the second I²C data byte (which the device writes to a register at address *n*), the session is not concluded by the I²C bus master setting a STOP condition. Instead, a third I²C data byte is sent. The device writes that data to the register having the address *n* + 1. This is done through a register counter that tracks which register was accessed and increments the register address by 1 for the third I²C data byte (which the device recognizes as the second byte that must be written to a register). Figure 2-5 shows a 16-bit I²C write access.

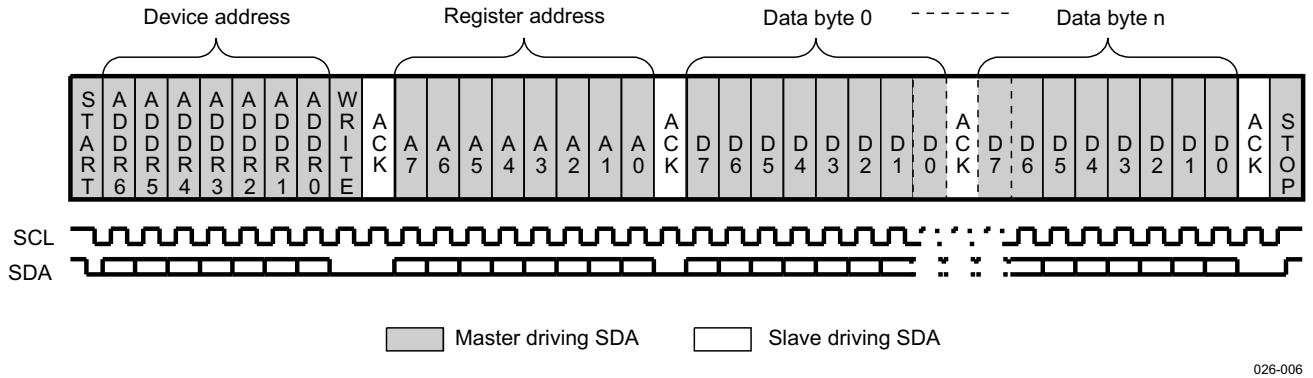
Figure 2-5. 16-Bit I²C Write Access



2.4.3.2 Burst Write Register Access

The device supports an I²C burst write protocol that extends the method used to write 16 bits to two adjacent registers (see Figure 2-6). If more than two adjacent device registers are to be written to, the I²C bus master continues to send I²C data bytes to the device until it is finished (signaled by setting the I²C STOP condition). Because the device increments the register counter to the adjacent register (*n* + 1) when it acknowledges receiving the value for register *n*, the I²C bus master does not need to send individual register addresses. Figure 2-6 shows an I²C burst write access.

Figure 2-6. I²C Burst Write Access



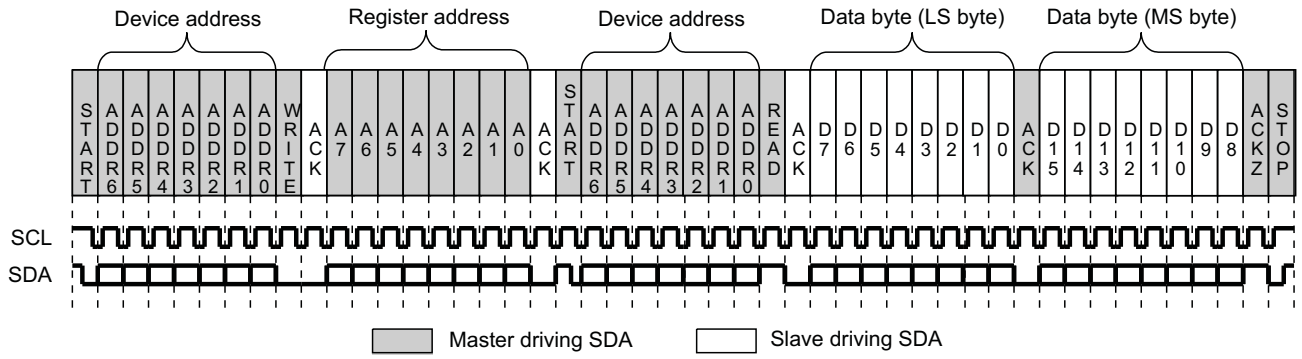
2.4.3.3 Register Counter Overflow (Write)

If a 16-bit or burst write I²C procedure causes the device register counter to try to exceed the maximum of 256 registers in a register address group, the counter rolls over and continues counting from 0. The software that controls the I²C bus master must track which device register is written to. The device register counter increments with every data byte received from the I²C bus master, and the registers addressed are written to until the I²C bus master stops sending data bytes and concludes with a STOP command.

2.4.3.4 16-Bit Read Register Access

When reading 16 bits of data from two adjacent device registers (in the same register address group and having relative addresses of *n* and *n* + 1) (see Figure 2-7), the same technique is used as when reading from one 8-bit address, except that after the first data byte comes from the device, the I²C bus master (after sending an ACK of the first data byte from the device) does not send a STOP command. Instead, it keeps monitioring. Not detecting a STOP command from the I²C bus master, the device sends the value of the register at address *n* + 1. This is done through a register counter that tracks which register was accessed and increments the register address by 1 for each ACK received from the I²C bus master. Figure 2-7 shows a 16-bit I²C read access.

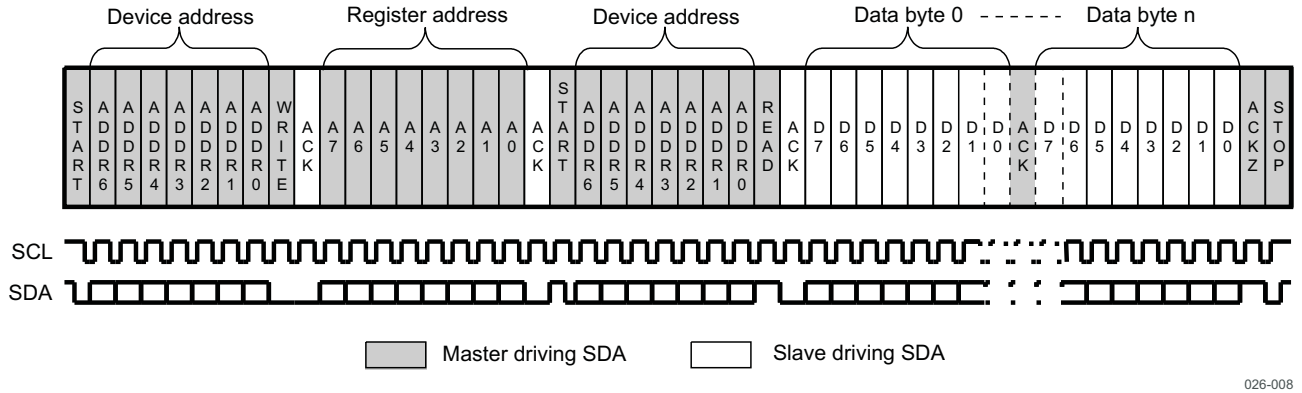
Figure 2-7. I²C 16-Bit Read Access



2.4.3.5 Burst Read Register Access

The device supports an I²C burst read protocol that extends the method used to access 16 bits (two adjacent registers) (see Figure 2-8). If more than two adjacent device registers are to be read, the I²C bus master continues to send ACKs for each data byte received. When the I²C bus master does not immediately send a STOP command, the device continues to send byte after byte of adjacent register values until the I²C bus master issues a STOP command. It is not necessary for the I²C bus master to issue new device register addresses. When the device hears an ACK from the I²C bus master for the data byte sent for register *n*, the device automatically increments the register counter to the adjacent register address *n* + 1 and sends its value. Figure 2-8 shows a burst read access.

Figure 2-8. Burst Read Access



2.4.3.6 Register Counter Overflow (Read)

If a 16-bit or burst read I²C procedure causes the device register counter to try to exceed the maximum of 256 registers in a register address group, the counter rolls over and continues counting from 0. The software that controls the I²C bus master must track which device register is being read from. The device register counter increments with every ACK from the I²C bus master, and the registers addressed are read from until the I²C bus master stops sending ACKs and concludes with a STOP command.

2.5 Control Interface Programming Model

The I²C bus, which is not programmable, applies external commands to device internal registers. The following example shows how the I²C bus is used to write data to a register.

2.5.1 Example: Setting a Device Register (8 Bits)

1. If the I²C bus is not busy, the I²C bus master (which sends commands to the device) issues an I²C START command. This signals the other I²C devices to be in listening mode in case they are about to be addressed.
2. The I²C bus master generates the I²C address (with the LSB set to write) for the correct device register address group.
3. The device acknowledges the address of the I²C register address group.
4. The I²C bus master sends a data byte that is the address of the desired register in the register address group that was addressed by the I²C address byte. (From the perspective of the I²C bus, what is being sent is a byte of data, so all 8 bits are available.)
5. The device acknowledges the byte of data (which it views as a register address in the already-accessed register address group).
6. The I²C bus master sends another byte of data to be loaded into the register.
7. The device acknowledges the byte of data and loads the 8 bits into the register addressed by the previous I²C data byte.

   (The command to the device is executed as a result of loading the register with the new data.)
8. When the I²C bus master device completes sending data to the device, it issues an I²C bus STOP command and releases the I²C bus.

2.6 Control Interface — Register Addressing

The device control interface (the I²C bus) does not have registers. The control interface is the gateway to the device registers that are discussed in other chapters in this TRM.

This section provides a cross-reference of the device registers and the I²C address groups. For information about I²C addressing, see Section 2.2.5, *I²C Bus Addressing*.

NOTE: The names Triton and Triton 2 are a direct reference to the device, indicating that the originating source material is from TI's product-development organization.

2.6.1 I²C Address Groups — Cross-Reference

Table 2-2 through Table 2-11 describe the device registers with the I²C group address 4b hex.

Table 2-12 through Table 2-23 describe the device registers with the I²C group address 4a hex.

Table 2-24 describes the device registers with the I²C group address 48 hex.

Table 2-25 through Table 2-30 describe the device registers with the I²C group address 49 hex.

Table 2-31 describes the device SmartReflex registers with the I²C group address 12 hex.

2.6.1.1 Address Group — 4b Hex

2.6.1.1.1 BACKUP_REG

Table 2-2. BACKUP_REG Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
BACKUP_REG_A	RW	8	0x0000 0014
BACKUP_REG_B	RW	8	0x0000 0015
BACKUP_REG_C	RW	8	0x0000 0016
BACKUP_REG_D	RW	8	0x0000 0017
BACKUP_REG_E	RW	8	0x0000 0018
BACKUP_REG_F	RW	8	0x0000 0019
BACKUP_REG_G	RW	8	0x0000 001A
BACKUP_REG_H	RW	8	0x0000 001B

2.6.1.1.2 INT

Table 2-3. INT Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
PWR_ISR1	RW	8	0x0000 002E
PWR_IMR1	RW	8	0x0000 002F
PWR_ISR2	RW	8	0x0000 0030
PWR_IMR2	RW	8	0x0000 0031
PWR_SIR	RW	8	0x0000 0032
PWR_EDR1	RW	8	0x0000 0033
PWR_EDR2	RW	8	0x0000 0034
PWR_SIH_CTRL	RW	8	0x0000 0035

2.6.1.1.3 PM_MASTER

Condition: P(ONNOFF) = 0

Table 2-4. PM_MASTER Register Summary for ONNOFF Mode Active

Register Name	Type	Register Width (Bits)	Physical Address
CFG_P1_TRANSITION	RW	8	0x0000 0036 – 0x0000 0036
CFG_P2_TRANSITION	RW	8	0x0000 0037 – 0x0000 0037
CFG_P3_TRANSITION	RW	8	0x0000 0038 – 0x0000 0038
CFG_P123_TRANSITION	RW	8	0x0000 0039 – 0x0000 0039
STS_BOOT	RW	8	0x0000 003A – 0x0000 003A
CFG_BOOT	RW	8	0x0000 003B – 0x0000 003B
SHUNDAN	RW	8	0x0000 003C – 0x0000 003C
BOOT_BCI	RW	8	0x0000 003D – 0x0000 003D
CFG_PWRANA1	RW	8	0x0000 003E – 0x0000 003E
CFG_PWRANA2	RW	8	0x0000 003F – 0x0000 003F
BGAP_TRIM	RW	8	0x0000 0040 – 0x0000 0040
BACKUP_MISC_STS	R	8	0x0000 0041 – 0x0000 0041
BACKUP_MISC_CFG	R	8	0x0000 0042 – 0x0000 0042
BACKUP_MISC_TST	R	8	0x0000 0043 – 0x0000 0043
PROTECT_KEY	RW	8	0x0000 0044 – 0x0000 0044
STS_HW_CONDITIONS	RW	8	0x0000 0045 – 0x0000 0045

Table 2-4. PM_MASTER Register Summary for ONNOFF Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
P1_SW_EVENTS	RW	8	0x0000 0046 – 0x0000 0046
P2_SW_EVENTS	RW	8	0x0000 0047 – 0x0000 0047
P3_SW_EVENTS	RW	8	0x0000 0048 – 0x0000 0048
STS_P123_STATE	R	8	0x0000 0049 – 0x0000 0049
PB_CFG	RW	8	0x0000 004A – 0x0000 004A
PB_WORD_MSB	RW	8	0x0000 004B – 0x0000 004B
PB_WORD_LSB	RW	8	0x0000 004C – 0x0000 004C
RESERVED_A	R	8	0x0000 004D – 0x0000 004D
RESERVED_B	R	8	0x0000 004E – 0x0000 004E
RESERVED_C	R	8	0x0000 004F – 0x0000 004F
RESERVED_D	R	8	0x0000 0050 – 0x0000 0050
RESERVED_E	R	8	0x0000 0051 – 0x0000 0051
SEQ_ADD_W2P	RW	8	0x0000 0052 – 0x0000 0052
SEQ_ADD_P2A	RW	8	0x0000 0053 – 0x0000 0053
SEQ_ADD_A2W	RW	8	0x0000 0054 – 0x0000 0054
SEQ_ADD_A2S	RW	8	0x0000 0055 – 0x0000 0055
SEQ_ADD_S2A12	RW	8	0x0000 0056 – 0x0000 0056
SEQ_ADD_S2A3	RW	8	0x0000 0057 – 0x0000 0057
SEQ_ADD_WARM	RW	8	0x0000 0058 – 0x0000 0058
MEMORY_ADDRESS	RW	8	0x0000 0059 – 0x0000 0059
MEMORY_DATA	RW	8	0x0000 005A – 0x0000 005A

Condition: P(POR) = 0

Table 2-5. PM_MASTER Register Summary for POR Mode Active

Register Name	Type	Register Width (Bits)	Physical Address
CFG_P1_TRANSITION	RW	8	0x0000 0036 – 0x0000 0036
CFG_P2_TRANSITION	RW	8	0x0000 0037 – 0x0000 0037
CFG_P3_TRANSITION	RW	8	0x0000 0038 – 0x0000 0038
CFG_P123_TRANSITION	RW	8	0x0000 0039 – 0x0000 0039
STS_BOOT	RW	8	0x0000 003A – 0x0000 003A
CFG_BOOT	RW	8	0x0000 003B – 0x0000 003B
SHUNDAN	RW	8	0x0000 003C – 0x0000 003C
BOOT_BCI	RW	8	0x0000 003D – 0x0000 003D
CFG_PWRANA1	RW	8	0x0000 003E – 0x0000 003E
CFG_PWRANA2	RW	8	0x0000 003F – 0x0000 003F
BGAP_TRIM	RW	8	0x0000 0040 – 0x0000 0040
BACKUP_MISC_STS	R	8	0x0000 0041 – 0x0000 0041
BACKUP_MISC_CFG	R	8	0x0000 0042 – 0x0000 0042
BACKUP_MISC_TST	R	8	0x0000 0043 – 0x0000 0043
PROTECT_KEY	RW	8	0x0000 0044 – 0x0000 0044
STS_HW_CONDITIONS	RW	8	0x0000 0045 – 0x0000 0045
P1_SW_EVENTS	RW	8	0x0000 0046 – 0x0000 0046
P2_SW_EVENTS	RW	8	0x0000 0047 – 0x0000 0047
P3_SW_EVENTS	RW	8	0x0000 0048 – 0x0000 0048
STS_P123_STATE	R	8	0x0000 0049 – 0x0000 0049
PB_CFG	RW	8	0x0000 004A – 0x0000 004A
PB_WORD_MSB	RW	8	0x0000 004B – 0x0000 004B

Table 2-5. PM_MASTER Register Summary for POR Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
PB_WORD_LSB	RW	8	0x0000 004C – 0x0000 004C
RESERVED_A	R	8	0x0000 004D – 0x0000 004D
RESERVED_B	R	8	0x0000 004E – 0x0000 004E
RESERVED_C	R	8	0x0000 004F – 0x0000 004F
RESERVED_D	R	8	0x0000 0050 – 0x0000 0050
RESERVED_E	R	8	0x0000 0051 – 0x0000 0051
SEQ_ADD_W2P	RW	8	0x0000 0052 – 0x0000 0052
SEQ_ADD_P2A	RW	8	0x0000 0053 – 0x0000 0053
SEQ_ADD_A2W	RW	8	0x0000 0054 – 0x0000 0054
SEQ_ADD_A2S	RW	8	0x0000 0055 – 0x0000 0055
SEQ_ADD_S2A12	RW	8	0x0000 0056 – 0x0000 0056
SEQ_ADD_S2A3	RW	8	0x0000 0057 – 0x0000 0057
SEQ_ADD_WARM	RW	8	0x0000 0058 – 0x0000 0058
MEMORY_ADDRESS	RW	8	0x0000 0059 – 0x0000 0059
MEMORY_DATA	RW	8	0x0000 005A – 0x0000 005A

Table 2-6. PM_RECEIVER Register Summary for SECURE Mode Active

Register Name	Type	Register Width (Bits)	Physical Address
SC_CONFIG	RW	8	0x0000 005B – 0x0000 005B
SC_DETECT1	RW	8	0x0000 005C – 0x0000 005C
SC_DETECT2	RW	8	0x0000 005D – 0x0000 005D
WATCHDOG_CFG	RW	8	0x0000 005E – 0x0000 005E
IT_CHECK_CFG	RW	8	0x0000 005F – 0x0000 005F
VIBRATOR_CFG	RW	8	0x0000 0060 – 0x0000 0060
DCDC_GLOBAL_CFG	RW	8	0x0000 0061 – 0x0000 0061
VDD1_TRIM1	RW	8	0x0000 0062 – 0x0000 0062
VDD1_TRIM2	RW	8	0x0000 0063 – 0x0000 0063
VDD2_TRIM1	RW	8	0x0000 0064 – 0x0000 0064
VDD2_TRIM2	RW	8	0x0000 0065 – 0x0000 0065
VIO_TRIM1	RW	8	0x0000 0066 – 0x0000 0066
VIO_TRIM2	RW	8	0x0000 0067 – 0x0000 0067
MISC_CFG	RW	8	0x0000 0068 – 0x0000 0068
LS_TST_A	RW	8	0x0000 0069 – 0x0000 0069
LS_TST_B	RW	8	0x0000 006A – 0x0000 006A
LS_TST_C	RW	8	0x0000 006B – 0x0000 006B
LS_TST_D	RW	8	0x0000 006C – 0x0000 006C
BB_CFG	RW	8	0x0000 006D – 0x0000 006D
MISC_TST	RW	8	0x0000 006E – 0x0000 006E
TRIM1	RW	8	0x0000 006F – 0x0000 006F
TRIM2	RW	8	0x0000 0070 – 0x0000 0070
DCDC_TIMEOUT	RW	8	0x0000 0071 – 0x0000 0071
VAUX2_DEV_GRP	R	8	0x0000 0076 – 0x0000 0076
VAUX2_TYPE	RW	8	0x0000 0077 – 0x0000 0077
VAUX2_REMAP	RW	8	0x0000 0078 – 0x0000 0078
VAUX2_DEDICATED	RW	8	0x0000 0079 – 0x0000 0079
VMMC1_DEV_GRP	RW	8	0x0000 0082 – 0x0000 0082
VMMC1_TYPE	RW	8	0x0000 0083 – 0x0000 0083

Table 2-6. PM_RECEIVER Register Summary for SECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
VMMC1_REMAP	RW	8	0x0000 0084 – 0x0000 0084
VMMC1_DEDICATED	RW	8	0x0000 0085 – 0x0000 0085
VPLL1_DEV_GRP	RW	8	0x0000 008A – 0x0000 008A
VPLL1_TYPE	RW	8	0x0000 008B – 0x0000 008B
VPLL1_REMAP	RW	8	0x0000 008C – 0x0000 008C
VPLL1_DEDICATED	RW	8	0x0000 008D – 0x0000 008D
VDAC_DEV_GRP	RW	8	0x0000 0096 – 0x0000 0096
VDAC_TYPE	RW	8	0x0000 0097 – 0x0000 0097
VDAC_REMAP	RW	8	0x0000 0098 – 0x0000 0098
VDAC_DEDICATED	RW	8	0x0000 0099 – 0x0000 0099
VINTANA1_DEV_GRP	RW	8	0x0000 009A – 0x0000 009A
VINTANA1_TYPE	RW	8	0x0000 009B – 0x0000 009B
VINTANA1_REMAP	RW	8	0x0000 009C – 0x0000 009C
VINTANA1_DEDICATED	RW	8	0x0000 009D – 0x0000 009D
VINTANA2_DEV_GRP	RW	8	0x0000 009E – 0x0000 009E
VINTANA2_TYPE	RW	8	0x0000 009F – 0x0000 009F
VINTANA2_REMAP	RW	8	0x0000 00A0 – 0x0000 00A0
VINTANA2_DEDICATED	RW	8	0x0000 00A1 – 0x0000 00A1
VINTDIG_DEV_GRP	RW	8	0x0000 00A2 – 0x0000 00A2
VINTDIG_TYPE	RW	8	0x0000 00A3 – 0x0000 00A3
VINTDIG_REMAP	RW	8	0x0000 00A4 – 0x0000 00A4
VINTDIG_DEDICATED	RW	8	0x0000 00A5 – 0x0000 00A5
VIO_DEV_GRP	RW	8	0x0000 00A6 – 0x0000 00A6
VIO_TYPE	RW	8	0x0000 00A7 – 0x0000 00A7
VIO_REMAP	RW	8	0x0000 00A8 – 0x0000 00A8
VIO_CFG	RW	8	0x0000 00A9 – 0x0000 00A9
VIO_MISC_CFG	RW	8	0x0000 00AA – 0x0000 00AA
VIO_TEST1	RW	8	0x0000 00AB – 0x0000 00AB
VIO_TEST2	RW	8	0x0000 00AC – 0x0000 00AC
VIO_OSC	RW	8	0x0000 00AD – 0x0000 00AD
VIO_RESERVED	RW	8	0x0000 00AE – 0x0000 00AE
VIO_VSEL	RW	8	0x0000 00AF – 0x0000 00AF
VDD1_DEV_GRP	RW	8	0x0000 00B0 – 0x0000 00B0
VDD1_TYPE	RW	8	0x0000 00B1 – 0x0000 00B1
VDD1_REMAP	RW	8	0x0000 00B2 – 0x0000 00B2
VDD1_CFG	RW	8	0x0000 00B3 – 0x0000 00B3
VDD1_MISC_CFG	RW	8	0x0000 00B4 – 0x0000 00B4
VDD1_TEST1	RW	8	0x0000 00B5 – 0x0000 00B5
VDD1_TEST2	RW	8	0x0000 00B6 – 0x0000 00B6
VDD1_OSC	RW	8	0x0000 00B7 – 0x0000 00B7
VDD1_RESERVED	RW	8	0x0000 00B8 – 0x0000 00B8
VDD1_VSEL	RW	8	0x0000 00B9 – 0x0000 00B9
VDD1_VMODE_CFG	RW	8	0x0000 00BA – 0x0000 00BA
VDD1_VFLOOR	RW	8	0x0000 00BB – 0x0000 00BB
VDD1_VROOF	RW	8	0x0000 00BC – 0x0000 00BC
VDD1_STEP	RW	8	0x0000 00BD – 0x0000 00BD
VDD2_DEV_GRP	RW	8	0x0000 00BE – 0x0000 00BE

Table 2-6. PM_RECEIVER Register Summary for SECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
VDD2_TYPE	RW	8	0x0000 00BF – 0x0000 00BF
VDD2_REMAP	RW	8	0x0000 00C0 – 0x0000 00C0
VDD2_CFG	RW	8	0x0000 00C1 – 0x0000 00C1
VDD2_MISC_CFG	RW	8	0x0000 00C2 – 0x0000 00C2
VDD2_TEST1	RW	8	0x0000 00C3 – 0x0000 00C3
VDD2_TEST2	RW	8	0x0000 00C4 – 0x0000 00C4
VDD2_OSC	RW	8	0x0000 00C5 – 0x0000 00C5
VDD2_RESERVED	RW	8	0x0000 00C6 – 0x0000 00C6
VDD2_VSEL	RW	8	0x0000 00C7 – 0x0000 00C7
VDD2_VMODE_CFG	RW	8	0x0000 00C8 – 0x0000 00C8
VDD2_VFLOOR	RW	8	0x0000 00C9 – 0x0000 00C9
VDD2_VROOF	RW	8	0x0000 00CA – 0x0000 00CA
VDD2_STEP	RW	8	0x0000 00CB – 0x0000 00CB
VUSB1V5_DEV_GRP	RW	8	0x0000 00CC – 0x0000 00CC
VUSB1V5_TYPE	RW	8	0x0000 00CD – 0x0000 00CD
VUSB1V5_REMAP	RW	8	0x0000 00CE – 0x0000 00CE
VUSB1V8_DEV_GRP	RW	8	0x0000 00CF – 0x0000 00CF
VUSB1V8_TYPE	RW	8	0x0000 00D0 – 0x0000 00D0
VUSB1V8_REMAP	RW	8	0x0000 00D1 – 0x0000 00D1
VUSB3V1_DEV_GRP	RW	8	0x0000 00D2 – 0x0000 00D2
VUSB3V1_TYPE	RW	8	0x0000 00D3 – 0x0000 00D3
VUSB3V1_REMAP	RW	8	0x0000 00D4 – 0x0000 00D4
VUSBCP_DEV_GRP	RW	8	0x0000 00D5 – 0x0000 00D5
VUSBCP_TYPE	RW	8	0x0000 00D6 – 0x0000 00D6
VUSBCP_REMAP	RW	8	0x0000 00D7 – 0x0000 00D7
VUSB_DEDICATED1	RW	8	0x0000 00D8 – 0x0000 00D8
VUSB_DEDICATED2	RW	8	0x0000 00D9 – 0x0000 00D9
REGEN_DEV_GRP	RW	8	0x0000 00DA – 0x0000 00DA
REGEN_TYPE	RW	8	0x0000 00DB – 0x0000 00DB
REGEN_REMAP	RW	8	0x0000 00DC – 0x0000 00DC
NRESPWRON_DEV_GRP	RW	8	0x0000 00DD – 0x0000 00DD
NRESPWRON_TYPE	RW	8	0x0000 00DE – 0x0000 00DE
NRESPWRON_REMAP	RW	8	0x0000 00DF – 0x0000 00DF
CLKEN_DEV_GRP	RW	8	0x0000 00E0 – 0x0000 00E0
CLKEN_TYPE	RW	8	0x0000 00E1 – 0x0000 00E1
CLKEN_REMAP	RW	8	0x0000 00E2 – 0x0000 00E2
SYSEN_DEV_GRP	RW	8	0x0000 00E3 – 0x0000 00E3
SYSEN_TYPE	RW	8	0x0000 00E4 – 0x0000 00E4
SYSEN_REMAP	RW	8	0x0000 00E5 – 0x0000 00E5
HFCLKOUT_DEV_GRP	RW	8	0x0000 00E6 – 0x0000 00E6
HFCLKOUT_TYPE	RW	8	0x0000 00E7 – 0x0000 00E7
HFCLKOUT_REMAP	RW	8	0x0000 00E8 – 0x0000 00E8
32KCLKOUT_DEV_GRP	RW	8	0x0000 00E9 – 0x0000 00E9
32KCLKOUT_TYPE	RW	8	0x0000 00EA – 0x0000 00EA
32KCLKOUT_REMAP	RW	8	0x0000 00EB – 0x0000 00EB
TRITON_RESET_DEV_GRP	RW	8	0x0000 00EC – 0x0000 00EC
TRITON_RESET_TYPE	RW	8	0x0000 00ED – 0x0000 00ED

Table 2-6. PM_RECEIVER Register Summary for SECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
TRITON_RESET_REMAP	RW	8	0x0000 00EE – 0x0000 00EE
MAINREF_DEV_GRP	RW	8	0x0000 00EF – 0x0000 00EF
MAINREF_TYPE	RW	8	0x0000 00F0 – 0x0000 00F0
MAINREF_REMAP	RW	8	0x0000 00F1 – 0x0000 00F1

Table 2-7. PM_RECEIVER Register Summary for UNSECURE Mode Active

Register Name	Type	Register Width (Bits)	Physical Address
SC_CONFIG	RW	8	0x0000 005B – 0x0000 005B
SC_DETECT1	RW	8	0x0000 005C – 0x0000 005C
SC_DETECT2	RW	8	0x0000 005D – 0x0000 005D
WATCHDOG_CFG	RW	8	0x0000 005E – 0x0000 005E
IT_CHECK_CFG	RW	8	0x0000 005F – 0x0000 005F
VIBRATOR_CFG	RW	8	0x0000 0060 – 0x0000 0060
DCDC_GLOBAL_CFG	RW	8	0x0000 0061 – 0x0000 0061
VDD1_TRIM1	RW	8	0x0000 0062 – 0x0000 0062
VDD1_TRIM2	RW	8	0x0000 0063 – 0x0000 0063
VDD2_TRIM1	RW	8	0x0000 0064 – 0x0000 0064
VDD2_TRIM2	RW	8	0x0000 0065 – 0x0000 0065
VIO_TRIM1	RW	8	0x0000 0066 – 0x0000 0066
VIO_TRIM2	RW	8	0x0000 0067 – 0x0000 0067
MISC_CFG	RW	8	0x0000 0068 – 0x0000 0068
LS_TST_A	RW	8	0x0000 0069 – 0x0000 0069
LS_TST_B	RW	8	0x0000 006A – 0x0000 006A
LS_TST_C	RW	8	0x0000 006B – 0x0000 006B
LS_TST_D	RW	8	0x0000 006C – 0x0000 006C
BB_CFG	RW	8	0x0000 006D – 0x0000 006D
MISC_TST	RW	8	0x0000 006E – 0x0000 006E
TRIM1	RW	8	0x0000 006F – 0x0000 006F
TRIM2	RW	8	0x0000 0070 – 0x0000 0070
DCDC_TIMEOUT	RW	8	0x0000 0071 – 0x0000 0071
VAUX2_DEV_GRP	RW	8	0x0000 0076 – 0x0000 0076
VAUX2_TYPE	RW	8	0x0000 0077 – 0x0000 0077
VAUX2_REMAP	RW	8	0x0000 0078 – 0x0000 0078
VAUX2_DEDICATED	RW	8	0x0000 0079 – 0x0000 0079
VMMC1_DEV_GRP	RW	8	0x0000 0082 – 0x0000 0082
VMMC1_TYPE	RW	8	0x0000 0083 – 0x0000 0083
VMMC1_REMAP	RW	8	0x0000 0084 – 0x0000 0084
VMMC1_DEDICATED	RW	8	0x0000 0085 – 0x0000 0085
VPLL1_DEV_GRP	RW	8	0x0000 008A – 0x0000 008A
VPLL1_TYPE	RW	8	0x0000 008B – 0x0000 008B
VPLL1_REMAP	RW	8	0x0000 008C – 0x0000 008C
VPLL1_DEDICATED	RW	8	0x0000 008D – 0x0000 008D
VDAC_DEV_GRP	RW	8	0x0000 0096 – 0x0000 0096
VDAC_TYPE	RW	8	0x0000 0097 – 0x0000 0097
VDAC_REMAP	RW	8	0x0000 0098 – 0x0000 0098
VDAC_DEDICATED	RW	8	0x0000 0099 – 0x0000 0099
VINTANA1_DEV_GRP	RW	8	0x0000 009A – 0x0000 009A

Table 2-7. PM_RECEIVER Register Summary for UNSECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
VINTANA1_TYPE	RW	8	0x0000 009B – 0x0000 009B
VINTANA1_REMAP	RW	8	0x0000 009C – 0x0000 009C
VINTANA1_DEDICATED	RW	8	0x0000 009D – 0x0000 009D
VINTANA2_DEV_GRP	RW	8	0x0000 009E – 0x0000 009E
VINTANA2_TYPE	RW	8	0x0000 009F – 0x0000 009F
VINTANA2_REMAP	RW	8	0x0000 00A0 – 0x0000 00A0
VINTANA2_DEDICATED	RW	8	0x0000 00A1 – 0x0000 00A1
VINTDIG_DEV_GRP	RW	8	0x0000 00A2 – 0x0000 00A2
VINTDIG_TYPE	RW	8	0x0000 00A3 – 0x0000 00A3
VINTDIG_REMAP	RW	8	0x0000 00A4 – 0x0000 00A4
VINTDIG_DEDICATED	RW	8	0x0000 00A5 – 0x0000 00A5
VIO_DEV_GRP	RW	8	0x0000 00A6 – 0x0000 00A6
VIO_TYPE	RW	8	0x0000 00A7 – 0x0000 00A7
VIO_REMAP	RW	8	0x0000 00A8 – 0x0000 00A8
VIO_CFG	RW	8	0x0000 00A9 – 0x0000 00A9
VIO_MISC_CFG	RW	8	0x0000 00AA – 0x0000 00AA
VIO_TEST1	RW	8	0x0000 00AB – 0x0000 00AB
VIO_TEST2	RW	8	0x0000 00AC – 0x0000 00AC
VIO_OSC	RW	8	0x0000 00AD – 0x0000 00AD
VIO_RESERVED	RW	8	0x0000 00AE – 0x0000 00AE
VIO_VSEL	RW	8	0x0000 00AF – 0x0000 00AF
VDD1_DEV_GRP	RW	8	0x0000 00B0 – 0x0000 00B0
VDD1_TYPE	RW	8	0x0000 00B1 – 0x0000 00B1
VDD1_REMAP	RW	8	0x0000 00B2 – 0x0000 00B2
VDD1_CFG	RW	8	0x0000 00B3 – 0x0000 00B3
VDD1_MISC_CFG	RW	8	0x0000 00B4 – 0x0000 00B4
VDD1_TEST1	RW	8	0x0000 00B5 – 0x0000 00B5
VDD1_TEST2	RW	8	0x0000 00B6 – 0x0000 00B6
VDD1_OSC	RW	8	0x0000 00B7 – 0x0000 00B7
VDD1_RESERVED	RW	8	0x0000 00B8 – 0x0000 00B8
VDD1_VSEL	RW	8	0x0000 00B9 – 0x0000 00B9
VDD1_VMODE_CFG	RW	8	0x0000 00BA – 0x0000 00BA
VDD1_VFLOOR	RW	8	0x0000 00BB – 0x0000 00BB
VDD1_VROOF	RW	8	0x0000 00BC – 0x0000 00BC
VDD1_STEP	RW	8	0x0000 00BD – 0x0000 00BD
VDD2_DEV_GRP	RW	8	0x0000 00BE – 0x0000 00BE
VDD2_TYPE	RW	8	0x0000 00BF – 0x0000 00BF
VDD2_REMAP	RW	8	0x0000 00C0 – 0x0000 00C0
VDD2_CFG	RW	8	0x0000 00C1 – 0x0000 00C1
VDD2_MISC_CFG	RW	8	0x0000 00C2 – 0x0000 00C2
VDD2_TEST1	RW	8	0x0000 00C3 – 0x0000 00C3
VDD2_TEST2	RW	8	0x0000 00C4 – 0x0000 00C4
VDD2_OSC	RW	8	0x0000 00C5 – 0x0000 00C5
VDD2_RESERVED	RW	8	0x0000 00C6 – 0x0000 00C6
VDD2_VSEL	RW	8	0x0000 00C7 – 0x0000 00C7
VDD2_VMODE_CFG	RW	8	0x0000 00C8 – 0x0000 00C8
VDD2_VFLOOR	RW	8	0x0000 00C9 – 0x0000 00C9

Table 2-7. PM_RECEIVER Register Summary for UNSECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
VDD2_VROOF	RW	8	0x0000 00CA – 0x0000 00CA
VDD2_STEP	RW	8	0x0000 00CB – 0x0000 00CB
VUSB1V5_DEV_GRP	RW	8	0x0000 00CC – 0x0000 00CC
VUSB1V5_TYPE	RW	8	0x0000 00CD – 0x0000 00CD
VUSB1V5_REMAP	RW	8	0x0000 00CE – 0x0000 00CE
VUSB1V8_DEV_GRP	RW	8	0x0000 00CF – 0x0000 00CF
VUSB1V8_TYPE	RW	8	0x0000 00D0 – 0x0000 00D0
VUSB1V8_REMAP	RW	8	0x0000 00D1 – 0x0000 00D1
VUSB3V1_DEV_GRP	RW	8	0x0000 00D2 – 0x0000 00D2
VUSB3V1_TYPE	RW	8	0x0000 00D3 – 0x0000 00D3
VUSB3V1_REMAP	RW	8	0x0000 00D4 – 0x0000 00D4
VUSBCP_DEV_GRP	RW	8	0x0000 00D5 – 0x0000 00D5
VUSBCP_TYPE	RW	8	0x0000 00D6 – 0x0000 00D6
VUSBCP_REMAP	RW	8	0x0000 00D7 – 0x0000 00D7
VUSB_DEDICATED1	RW	8	0x0000 00D8 – 0x0000 00D8
VUSB_DEDICATED2	RW	8	0x0000 00D9 – 0x0000 00D9
REGEN_DEV_GRP	RW	8	0x0000 00DA – 0x0000 00DA
REGEN_TYPE	RW	8	0x0000 00DB – 0x0000 00DB
REGEN_REMAP	RW	8	0x0000 00DC – 0x0000 00DC
NRESPWRON_DEV_GRP	RW	8	0x0000 00DD – 0x0000 00DD
NRESPWRON_TYPE	RW	8	0x0000 00DE – 0x0000 00DE
NRESPWRON_REMAP	RW	8	0x0000 00DF – 0x0000 00DF
CLKEN_DEV_GRP	RW	8	0x0000 00E0 – 0x0000 00E0
CLKEN_TYPE	RW	8	0x0000 00E1 – 0x0000 00E1
CLKEN_REMAP	RW	8	0x0000 00E2 – 0x0000 00E2
SYSEN_DEV_GRP	RW	8	0x0000 00E3 – 0x0000 00E3
SYSEN_TYPE	RW	8	0x0000 00E4 – 0x0000 00E4
SYSEN_REMAP	RW	8	0x0000 00E5 – 0x0000 00E5
HFCLKOUT_DEV_GRP	RW	8	0x0000 00E6 – 0x0000 00E6
HFCLKOUT_TYPE	RW	8	0x0000 00E7 – 0x0000 00E7
HFCLKOUT_REMAP	RW	8	0x0000 00E8 – 0x0000 00E8
32KCLKOUT_DEV_GRP	RW	8	0x0000 00E9 – 0x0000 00E9
32KCLKOUT_TYPE	RW	8	0x0000 00EA – 0x0000 00EA
32KCLKOUT_REMAP	RW	8	0x0000 00EB – 0x0000 00EB
TRITON_RESET_DEV_GRP	RW	8	0x0000 00EC – 0x0000 00EC
TRITON_RESET_TYPE	RW	8	0x0000 00ED – 0x0000 00ED
TRITON_RESET_REMAP	RW	8	0x0000 00EE – 0x0000 00EE
MAINREF_DEV_GRP	RW	8	0x0000 00EF – 0x0000 00EF
MAINREF_TYPE	RW	8	0x0000 00F0 – 0x0000 00F0
MAINREF_REMAP	RW	8	0x0000 00F1 – 0x0000 00F1

Condition: P(MSecure) = 0

Table 2-8. RTC Register Summary for SECURE Mode Active

Register Name	Type	Register Width (Bits)	Physical Address
SECONDS_REG	R	8	0x0000 001C
MINUTES_REG	R	8	0x0000 001D
HOURS_REG	R	8	0x0000 001E

Table 2-8. RTC Register Summary for SECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
DAYS_REG	R	8	0x0000 001F
MONTHS_REG	R	8	0x0000 0020
YEARS_REG	R	8	0x0000 0021
WEEKS_REG	R	8	0x0000 0022
ALARM_SECONDS_REG	RW	8	0x0000 0023
ALARM_MINUTES_REG	RW	8	0x0000 0024
ALARM_HOURS_REG	RW	8	0x0000 0025
ALARM_DAYS_REG	RW	8	0x0000 0026
ALARM_MONTHS_REG	RW	8	0x0000 0027
ALARM_YEARS_REG	RW	8	0x0000 0028
RTC_CTRL_REG	R	8	0x0000 0029
RTC_STATUS_REG	RW	8	0x0000 002A
RTC_INTERRUPTS_REG	RW	8	0x0000 002B
RTC_COMP_LSB_REG	R	8	0x0000 002C
RTC_COMP_MSB_REG	R	8	0x0000 002D

Condition: P(MSecure) = 1

Table 2-9. RTC Register Summary for UNSECURE Mode Active

Register Name	Type	Register Width (Bits)	Physical Address
SECONDS_REG	RW	8	0x0000 001C
MINUTES_REG	RW	8	0x0000 001D
HOURS_REG	RW	8	0x0000 001E
DAYS_REG	RW	8	0x0000 001F
MONTHS_REG	RW	8	0x0000 0020
YEARS_REG	RW	8	0x0000 0021
WEEKS_REG	RW	8	0x0000 0022
ALARM_SECONDS_REG	RW	8	0x0000 0023
ALARM_MINUTES_REG	RW	8	0x0000 0024
ALARM_HOURS_REG	RW	8	0x0000 0025
ALARM_DAYS_REG	RW	8	0x0000 0026
ALARM_MONTHS_REG	RW	8	0x0000 0027
ALARM_YEARS_REG	RW	8	0x0000 0028
RTC_CTRL_REG	RW	8	0x0000 0029
RTC_STATUS_REG	RW	8	0x0000 002A
RTC_INTERRUPTS_REG	RW	8	0x0000 002B
RTC_COMP_LSB_REG	RW	8	0x0000 002C
RTC_COMP_MSB_REG	RW	8	0x0000 002D

2.6.1.1.4 SECURED_REG

Table 2-10. SECURED_REG Register Summary for SECURE Mode Active

Register Name	Type	Register Width (Bits)	Physical Address
SECURED_REG_A	R	8	0x0000 0000
SECURED_REG_B	R	8	0x0000 0001
SECURED_REG_C	R	8	0x0000 0002
SECURED_REG_D	R	8	0x0000 0003

Table 2-10. SECURED_REG Register Summary for SECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
SECURED_REG_E	R	8	0x0000 0004
SECURED_REG_F	R	8	0x0000 0005
SECURED_REG_G	R	8	0x0000 0006
SECURED_REG_H	R	8	0x0000 0007
SECURED_REG_I	R	8	0x0000 0008
SECURED_REG_J	R	8	0x0000 0009
SECURED_REG_K	R	8	0x0000 000A
SECURED_REG_L	R	8	0x0000 000B
SECURED_REG_M	R	8	0x0000 000C
SECURED_REG_N	R	8	0x0000 000D
SECURED_REG_O	R	8	0x0000 000E
SECURED_REG_P	R	8	0x0000 000F
SECURED_REG_Q	R	8	0x0000 0010
SECURED_REG_R	R	8	0x0000 0011
SECURED_REG_S	R	8	0x0000 0012
SECURED_REG_U	R	8	0x0000 0013

Table 2-11. SECURED_REG Register Summary for UNSECURE Mode Active

Register Name	Type	Register Width (Bits)	Physical Address
SECURED_REG_A	RW	8	0x0000 0000
SECURED_REG_B	RW	8	0x0000 0001
SECURED_REG_C	RW	8	0x0000 0002
SECURED_REG_D	RW	8	0x0000 0003
SECURED_REG_E	RW	8	0x0000 0004
SECURED_REG_F	RW	8	0x0000 0005
SECURED_REG_G	RW	8	0x0000 0006
SECURED_REG_H	RW	8	0x0000 0007
SECURED_REG_I	RW	8	0x0000 0008
SECURED_REG_J	RW	8	0x0000 0009
SECURED_REG_K	RW	8	0x0000 000A
SECURED_REG_L	RW	8	0x0000 000B
SECURED_REG_M	RW	8	0x0000 000C
SECURED_REG_N	RW	8	0x0000 000D
SECURED_REG_O	RW	8	0x0000 000E
SECURED_REG_P	RW	8	0x0000 000F
SECURED_REG_Q	RW	8	0x0000 0010
SECURED_REG_R	RW	8	0x0000 0011
SECURED_REG_S	RW	8	0x0000 0012
SECURED_REG_U	RW	8	0x0000 0013

2.6.1.2 Address Group — 4a Hex

2.6.1.2.1 Interrupts

Table 2-12. Interrupt Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
BCIISR1A	RW	8	0x0000 00B9
BCIISR2A	RW	8	0x0000 00BA
BCIIMR1A	RW	8	0x0000 00BB
BCIIMR2A	RW	8	0x0000 00BC
BCIISR1B	RW	8	0x0000 00BD
BCIISR2B	RW	8	0x0000 00BE
BCIIMR1B	RW	8	0x0000 00BF
BCIIMR2B	RW	8	0x0000 00C0
BCISIR1	RW	8	0x0000 00C1
BCISIR2	RW	8	0x0000 00C2
BCIEDR1	RW	8	0x0000 00C3
BCIEDR2	RW	8	0x0000 00C4
BCIEDR3	RW	8	0x0000 00C5
BCISIHCTRL	RW	8	0x0000 00C6

2.6.1.2.2 MADC

Table 2-13. MADC Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
CTRL1	RW	8	0x0000 0000
CTRL2	RW	8	0x0000 0001
RTSELECT_LSB	RW	8	0x0000 0002
RTSELECT_MSB	RW	8	0x0000 0003
RTAVERAGE_LSB	RW	8	0x0000 0004
RTAVERAGE_MSB	RW	8	0x0000 0005
SW1SELECT_LSB	RW	8	0x0000 0006
SW1SELECT_MSB	RW	8	0x0000 0007
SW1AVERAGE_LSB	RW	8	0x0000 0008
SW1AVERAGE_MSB	RW	8	0x0000 0009
SW2SELECT_LSB	RW	8	0x0000 000A
SW2SELECT_MSB	RW	8	0x0000 000B
SW2AVERAGE_LSB	RW	8	0x0000 000C
SW2AVERAGE_MSB	RW	8	0x0000 000D
BCI_USBAVERAGE	RW	8	0x0000 000E
ACQUISITION	RW	8	0x0000 000F
USBREF_LSB	RW	8	0x0000 0010
USBREF_MSB	RW	8	0x0000 0011
CTRL_SW1	RW	8	0x0000 0012
CTRL_SW2	RW	8	0x0000 0013
MADC_TEST	RW	8	0x0000 0014
GP_MADC_TEST1	RW	8	0x0000 0015
GP_MADC_TEST2	RW	8	0x0000 0016
RTCH0_LSB	RW	8	0x0000 0017
RTCH0_MSB	RW	8	0x0000 0018
RTCH1_LSB	RW	8	0x0000 0019
RTCH1_MSB	RW	8	0x0000 001A
RTCH2_LSB	RW	8	0x0000 001B

Table 2-13. MADC Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address
RTCH2_MSB	RW	8	0x0000 001C
RTCH3_LSB	RW	8	0x0000 001D
RTCH3_MSB	RW	8	0x0000 001E
RTCH4_LSB	RW	8	0x0000 001F
RTCH4_MSB	RW	8	0x0000 0020
RTCH5_LSB	RW	8	0x0000 0021
RTCH5_MSB	RW	8	0x0000 0022
RTCH6_LSB	RW	8	0x0000 0023
RTCH6_MSB	RW	8	0x0000 0024
RTCH7_LSB	RW	8	0x0000 0025
RTCH7_MSB	RW	8	0x0000 0026
RTCH8_LSB	RW	8	0x0000 0027
RTCH8_MSB	RW	8	0x0000 0028
RTCH9_LSB	RW	8	0x0000 0029
RTCH9_MSB	RW	8	0x0000 002A
RTCH10_LSB	RW	8	0x0000 002B
RTCH10_MSB	RW	8	0x0000 002C
RTCH11_LSB	RW	8	0x0000 002D
RTCH11_MSB	RW	8	0x0000 002E
RTCH12_LSB	RW	8	0x0000 002F
RTCH12_MSB	RW	8	0x0000 0030
RTCH13_LSB	RW	8	0x0000 0031
RTCH13_MSB	RW	8	0x0000 0032
RTCH14_LSB	RW	8	0x0000 0033
RTCH14_MSB	RW	8	0x0000 0034
RTCH15_LSB	RW	8	0x0000 0035
RTCH15_MSB	RW	8	0x0000 0036
GPCH0_LSB	RW	8	0x0000 0037
GPCH0_MSB	RW	8	0x0000 0038
GPCH1_LSB	RW	8	0x0000 0039
GPCH1_MSB	RW	8	0x0000 003A
GPCH2_LSB	RW	8	0x0000 003B
GPCH2_MSB	RW	8	0x0000 003C
GPCH3_LSB	RW	8	0x0000 003D
GPCH3_MSB	RW	8	0x0000 003E
GPCH4_LSB	RW	8	0x0000 003F
GPCH4_MSB	RW	8	0x0000 0040
GPCH5_LSB	RW	8	0x0000 0041
GPCH5_MSB	RW	8	0x0000 0042
GPCH6_LSB	RW	8	0x0000 0043
GPCH6_MSB	RW	8	0x0000 0044
GPCH7_LSB	RW	8	0x0000 0045
GPCH7_MSB	RW	8	0x0000 0046
GPCH8_LSB	RW	8	0x0000 0047
GPCH8_MSB	RW	8	0x0000 0048
GPCH9_LSB	RW	8	0x0000 0049
GPCH9_MSB	RW	8	0x0000 004A

Table 2-13. MADC Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address
GPCH10_LSB	RW	8	0x0000 004B
GPCH10_MSB	RW	8	0x0000 004C
GPCH11_LSB	RW	8	0x0000 004D
GPCH11_MSB	RW	8	0x0000 004E
GPCH12_LSB	RW	8	0x0000 004F
GPCH12_MSB	RW	8	0x0000 0050
GPCH13_LSB	RW	8	0x0000 0051
GPCH13_MSB	RW	8	0x0000 0052
GPCH14_LSB	RW	8	0x0000 0053
GPCH14_MSB	RW	8	0x0000 0054
GPCH15_LSB	RW	8	0x0000 0055
GPCH15_MSB	RW	8	0x0000 0056
MADC_ISR1	RW	8	0x0000 0061
MADC_IMR1	RW	8	0x0000 0062
MADC_ISR2	RW	8	0x0000 0063
MADC_IMR2	RW	8	0x0000 0064
MADC_SIR	RW	8	0x0000 0065
MADC_EDR	RW	8	0x0000 0066
MADC_SIH_CTRL	RW	8	0x0000 0067

2.6.1.2.3 PWM0

Table 2-14. PWM0 Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
PWM0ON	RW	8	0x0000 00F8
PWM0OFF	RW	8	0x0000 00F9

Table 2-15. PWM0ON

Address Offset	0x00		
Physical Address	0x0000 00F8	**Instance**	AUX_SCpwmPWM0
Description	Controls the ON time of the PWM0 and allows selecting the number of clock cycles in the PWM0 period: 128 (default value: bit at 0) or 64 (bit at 1)		
Type	RW		

7	6	5	4	3	2	1	0
INT_PWM_LENGTH0	PWM0ON6	PWM0ON5	PWM0ON4	PWM0ON3	PWM0ON2	PWM0ON1	PWM0ON0

Bits	Field Name	Description	Type	Reset
7	INT_PWM_LENGTH0	Allows selection of the number of clock cycles in the PWM0 period: 128 (default value: bit at 0) or 64 (bit at 1)	RW	0
6	PWM0ON6	DATA6	RW	0
5	PWM0ON5	DATA5	RW	0

Bits	Field Name	Description	Type	Reset
4	PWM0ON4	DATA4	RW	0
3	PWM0ON3	DATA3	RW	0
2	PWM0ON2	DATA2	RW	0
1	PWM0ON1	DATA1	RW	0
0	PWM0ON0	DATA0	RW	0

Table 2-16. PWM0OFF

Address Offset	0x01		
Physical Address	0x0000 00F9	**Instance**	AUX_SCpwmPWM0
Description	Controls the OFF time of the PWM0		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	PWM0OFF6	PWM0OFF5	PWM0OFF4	PWM0OFF3	PWM0OFF2	PWM0OFF1	PWM0OFF0

Bits	Field Name	Description	Type	Reset
7	Reserved	Not used	R	0
6	PWM0OFF6	DATA6	RW	0
5	PWM0OFF5	DATA5	RW	0
4	PWM0OFF4	DATA4	RW	0
3	PWM0OFF3	DATA3	RW	0
2	PWM0OFF2	DATA2	RW	0
1	PWM0OFF1	DATA1	RW	0
0	PWM0OFF0	DATA0	RW	0

2.6.1.2.4 PWM1

Table 2-17. PWM1 Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
PWM1ON	RW	8	0x0000 00FB
PWM1OFF	RW	8	0x0000 00FC

Table 2-18. PWM1ON

Address Offset	0x00		
Physical Address	0x0000 00FB	**Instance**	AUX_SCpwmPWM1
Description	Controls the ON time of the PWM1 and allows selecting the number of clock cycles in the PWM1 period: 128 (default value: bit at 0) or 64 (bit at 1)		
Type	RW		

7	6	5	4	3	2	1	0
INT_PWM_LENGTH1	PWM1ON6	PWM1ON5	PWM1ON4	PWM1ON3	PWM1ON2	PWM1ON1	PWM1ON0

Bits	Field Name	Description	Type	Reset
7	INT_PWM_LENGTH1	Allows selection of the number of clock cycles in the PWM1 period: 128 (default value: bit at 0) or 64 (bit at 1)	RW	0
6	PWM1ON6	DATA6	RW	0
5	PWM1ON5	DATA5	RW	0
4	PWM1ON4	DATA4	RW	0
3	PWM1ON3	DATA3	RW	0
2	PWM1ON2	DATA2	RW	0
1	PWM1ON1	DATA1	RW	0
0	PWM1ON0	DATA0	RW	0

Table 2-19. PWM1OFF

Address Offset	0x01		
Physical Address	0x0000 00FC	**Instance**	AUX_SCpwmPWM1
Description	Controls the OFF time of the PWM1		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	PWM1ONFF6	PWM1OFF5	PWM1OFF4	PWM1OFF3	PWM1OFF2	PWM1OFF1	PWM1OFF0

Bits	Field Name	Description	Type	Reset
7	Reserved	Not used	R	0
6	PWM1OFF6	DATA6	RW	0
5	PWM1OFF5	DATA5	RW	0
4	PWM1OFF4	DATA4	RW	0
3	PWM1OFF3	DATA3	RW	0
2	PWM1OFF2	DATA2	RW	0

Bits	Field Name	Description	Type	Reset
1	PWM1OFF1	DATA1	RW	0
0	PWM1OFF0	DATA0		

2.6.1.2.5 LED

Table 2-20. LED Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
LEDEN	RW	8	0x0000 00EE

2.6.1.2.6 PWMA

Table 2-21. PWMA Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
PWMAON	RW	8	0x0000 00EF
PWMAOFF	RW	8	0x0000 00F0

2.6.1.2.7 PWMB

Table 2-22. PWMB Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
PWMBON	RW	8	0x0000 00F1
PWMBOFF	RW	8	0x0000 00F2

2.6.1.2.8 KEYPAD

Table 2-23. KEYPAD Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
KEYP_CTRL_REG	RW	8	0x0000 00D2
KEY_DEB_REG	RW	8	0x0000 00D3
LONG_KEY_REG1	RW	8	0x0000 00D4
LK_PTV_REG	RW	8	0x0000 00D5
TIME_OUT_REG1	RW	8	0x0000 00D6
TIME_OUT_REG2	RW	8	0x0000 00D7
KBC_REG	RW	8	0x0000 00D8
KBR_REG	R	8	0x0000 00D9
KEYP_SMS	R	8	0x0000 00DA
FULL_CODE_7_0	R	8	0x0000 00DB
FULL_CODE_15_8	R	8	0x0000 00DC
FULL_CODE_23_16	R	8	0x0000 00DD
FULL_CODE_31_24	R	8	0x0000 00DE
FULL_CODE_39_32	R	8	0x0000 00DF
FULL_CODE_47_40	R	8	0x0000 00E0
FULL_CODE_55_48	R	8	0x0000 00E1
FULL_CODE_63_56	R	8	0x0000 00E2
KEYP_ISR1	RW	8	0x0000 00E3
KEYP_IMR1	RW	8	0x0000 00E4
KEYP_ISR2	RW	8	0x0000 00E5

Table 2-23. KEYPAD Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address
KEYP_IMR2	RW	8	0x0000 00E6
KEYP_SIR	RW	8	0x0000 00E7
KEYP_EDR	RW	8	0x0000 00E8
KEYP_SIH_CTRL	RW	8	0x0000 00E9

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2.6.2.1 USB

Table 2-24. USB Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
VENDOR_ID_LO	R	8	0x0000 0000
VENDOR_ID_HI	R	8	0x0000 0001
PRODUCT_ID_LO	R	8	0x0000 0002
PRODUCT_ID_HI	R	8	0x0000 0003
FUNC_CTRL	RW	8	0x0000 0004
FUNC_CTRL_SET	RW	8	0x0000 0005
FUNC_CTRL_CLR	RW	8	0x0000 0006
IFC_CTRL	RW	8	0x0000 0007
IFC_CTRL_SET	RW	8	0x0000 0008
IFC_CTRL_CLR	RW	8	0x0000 0009
OTG_CTRL	RW	8	0x0000 000A
OTG_CTRL_SET	RW	8	0x0000 000B
OTG_CTRL_CLR	RW	8	0x0000 000C
USB_INT_EN_RISE	RW	8	0x0000 000D
USB_INT_EN_RISE_SET	RW	8	0x0000 000E
USB_INT_EN_RISE_CLR	RW	8	0x0000 000F
USB_INT_EN_FALL	RW	8	0x0000 0010
USB_INT_EN_FALL_SET	RW	8	0x0000 0011
USB_INT_EN_FALL_CLR	RW	8	0x0000 0012
USB_INT_STS	R	8	0x0000 0013
USB_INT_LATCH	R	8	0x0000 0014
DEBUG	R	8	0x0000 0015
SCRATCH_REG	RW	8	0x0000 0016
SCRATCH_REG_SET	RW	8	0x0000 0017
SCRATCH_REG_CLR	RW	8	0x0000 0018
CARKIT_CTRL_SET	RW	8	0x0000 001A
CARKIT_CTRL	RW	8	0x0000 0019
CARKIT_CTRL_CLR	RW	8	0x0000 001B
CARKIT_INT_DELAY	RW	8	0x0000 001C
CARKIT_INT_EN	RW	8	0x0000 001D
CARKIT_INT_EN_SET	RW	8	0x0000 001E
CARKIT_INT_EN_CLR	RW	8	0x0000 001F
CARKIT_INT_STS	R	8	0x0000 0020
CARKIT_INT_LATCH	R	8	0x0000 0021
CARKIT_PLS_CTRL	RW	8	0x0000 0022
CARKIT_PLS_CTRL_SET	RW	8	0x0000 0023

Table 2-24. USB Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address
CARKIT_PLS_CTRL_CLR	RW	8	0x0000 0024
TRANS_POS_WIDTH	RW	8	0x0000 0025
TRANS_NEG_WIDTH	RW	8	0x0000 0026
RCV_PLTY_RECOVERY	RW	8	0x0000 0027
OTHER_FUNC_CTRL	RW	8	0x0000 0080
OTHER_FUNC_CTRL_SET	RW	8	0x0000 0081
OTHER_FUNC_CTRL_CLR	RW	8	0x0000 0082
OTHER_IFC_CTRL	RW	8	0x0000 0083
OTHER_IFC_CTRL_SET	RW	8	0x0000 0084
OTHER_IFC_CTRL_CLR	RW	8	0x0000 0085
OTHER_INT_EN_RISE	RW	8	0x0000 0086
OTHER_INT_EN_RISE_SET	RW	8	0x0000 0087
OTHER_INT_EN_RISE_CLR	RW	8	0x0000 0088
OTHER_INT_EN_FALL	RW	8	0x0000 0089
OTHER_INT_EN_FALL_SET	RW	8	0x0000 008A
OTHER_INT_EN_FALL_CLR	RW	8	0x0000 008B
OTHER_INT_STS	R	8	0x0000 008C
OTHER_INT_LATCH	R	8	0x0000 008D
ID_INT_EN_RISE	RW	8	0x0000 008E
ID_INT_EN_RISE_SET	RW	8	0x0000 008F
ID_INT_EN_RISE_CLR	RW	8	0x0000 0090
ID_INT_EN_FALL	RW	8	0x0000 0091
ID_INT_EN_FALL_SET	RW	8	0x0000 0092
ID_INT_EN_FALL_CLR	RW	8	0x0000 0093
ID_INT_STS	RW	8	0x0000 0094
ID_INT_LATCH	R	8	0x0000 0095
ID_STATUS	R	8	0x0000 0096
CARKIT_SM_1_INT_EN	RW	8	0x0000 0097
CARKIT_SM_1_INT_EN_SET	RW	8	0x0000 0098
CARKIT_SM_1_INT_EN_CLR	RW	8	0x0000 0099
CARKIT_SM_1_INT_STS	RW	8	0x0000 009A
CARKIT_SM_1_INT_LATCH	R	8	0x0000 009B
CARKIT_SM_2_INT_EN	RW	8	0x0000 009C
CARKIT_SM_2_INT_EN_SET	RW	8	0x0000 009D
CARKIT_SM_2_INT_EN_CLR	RW	8	0x0000 009E
CARKIT_SM_2_INT_STS	RW	8	0x0000 009F
CARKIT_SM_2_INT_LATCH	R	8	0x0000 00A0
CARKIT_SM_CTRL	RW	8	0x0000 00A1
CARKIT_SM_CTRL_SET	RW	8	0x0000 00A2
CARKIT_SM_CTRL_CLR	RW	8	0x0000 00A3
CARKIT_SM_CMD	RW	8	0x0000 00A4
CARKIT_SM_CMD_SET	RW	8	0x0000 00A5
CARKIT_SM_CMD_CLR	RW	8	0x0000 00A6
CARKIT_SM_CMD_STS	RW	8	0x0000 00A7
CARKIT_SM_STATUS	RW	8	0x0000 00A8
CARKIT_SM_NEXT_STATUS	R	8	0x0000 00A9
CARKIT_SM_ERR_STATUS	R	8	0x0000 00AA

Table 2-24. USB Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address
CARKIT_SM_CTRL_STATE	RW	8	0x0000 00AB
POWER_CTRL	RW	8	0x0000 00AC
POWER_CTRL_SET	RW	8	0x0000 00AD
POWER_CTRL_CLR	RW	8	0x0000 00AE
OTHER_IFC_CTRL2	RW	8	0x0000 00AF
OTHER_IFC_CTRL2_SET	RW	8	0x0000 00B0
OTHER_IFC_CTRL2_CLR	RW	8	0x0000 00B1
REG_CTRL_EN	RW	8	0x0000 00B2
REG_CTRL_EN_SET	RW	8	0x0000 00B3
REG_CTRL_EN_CLR	RW	8	0x0000 00B4
REG_CTRL_ERROR	R	8	0x0000 00B5
OTHER_FUNC_CTRL2	RW	8	0x0000 00B8
OTHER_FUNC_CTRL2_SET	RW	8	0x0000 00B9
OTHER_FUNC_CTRL2_CLR	RW	8	0x0000 00BA
CARKIT_ANA_CTRL	RW	8	0x0000 00BB
CARKIT_ANA_CTRL_SET	RW	8	0x0000 00BC
CARKIT_ANA_CTRL_CLR	RW	8	0x0000 00BD
VBUS_DEBOUNCE	RW	8	0x0000 00C0
ID_DEBOUNCE	RW	8	0x0000 00C1
TPH_DP_CON_MIN	RW	8	0x0000 00C2
TPH_DP_CON_MAX	RW	8	0x0000 00C3
TCR_DP_CON_MIN	RW	8	0x0000 00C4
TCR_DP_CON_MAX	RW	8	0x0000 00C5
TPH_DP_PD_SHORT	RW	8	0x0000 00C6
TPH_CMD_DLY	RW	8	0x0000 00C7
TPH_DET_RST	RW	8	0x0000 00C8
TPH_AUD_BIAS	RW	8	0x0000 00C9
TCR_UART_DET_MIN	RW	8	0x0000 00CA
TCR_UART_DET_MAX	RW	8	0x0000 00CB
TPH_ID_INT_PW	RW	8	0x0000 00CD
TACC_ID_INT_WAIT	RW	8	0x0000 00CE
TACC_ID_INT_PW	RW	8	0x0000 00CF
TPH_CMD_WAIT	RW	8	0x0000 00D0
TPH_ACK_WAIT	RW	8	0x0000 00D1
TPH_DP_DISC_DET	RW	8	0x0000 00D2
VBAT_TIMER	RW	8	0x0000 00D3
CARKIT_4W_DEBUG	R	8	0x0000 00E0
CARKIT_5W_DEBUG	R	8	0x0000 00E1
CARKIT_5W_DEBUG	R	8	0x0000 00E1
TEST_CTRL_CLR	RW	8	0x0000 00EB
TEST_CARKIT_SET	RW	8	0x0000 00EC
TEST_CARKIT_CLR	RW	8	0x0000 00ED
TEST_POWER_SET	RW	8	0x0000 00EE
TEST_POWER_CLR	RW	8	0x0000 00EF
TEST_ULPI	RW	8	0x0000 00F0
TXVR_EN_TEST_SET	RW	8	0x0000 00F2
TXVR_EN_TEST_CLR	RW	8	0x0000 00F3

Table 2-24. USB Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address
VBUS_EN_TEST	RW	8	0x0000 00F4
ID_EN_TEST	RW	8	0x0000 00F5
PSM_EN_TEST_SET	RW	8	0x0000 00F6
PSM_EN_TEST_CLR	RW	8	0x0000 00F7
PHY_TRIM_CTRL	RW	8	0x0000 00FC
PHY_PWR_CTRL	RW	8	0x0000 00FD
PHY_CLK_CTRL	RW	8	0x0000 00FE
PHY_CLK_CTRL_STS	RW	8	0x0000 00FF

2.6.3 Address Group – 49 Hex

2.6.3.1 AUDIO_VOICE

Table 2-25. AUDIO_VOICE Register Summary (TPS65930 Only)

Register Name	Type	Register Width (Bits)	Physical Address
codec_MODE	RW	8	0x0000 0001
OPTION	RW	8	0x0000 0002
MICBIAS_CTL	RW	8	0x0000 0004
ANAMICL	RW	8	0x0000 0005
ANAMICR	RW	8	0x0000 0006
AVADC_CTL	RW	8	0x0000 0007
ADCMICSEL	RW	8	0x0000 0008
DIGMIXING	RW	8	0x0000 0009
ATXL1PGA	RW	8	0x0000 000A
ATXR1PGA	RW	8	0x0000 000B
AVTXL2PGA	RW	8	0x0000 000C
AVTXR2PGA	RW	8	0x0000 000D
AUDIO_IF	RW	8	0x0000 000E
VOICE_IF	RW	8	0x0000 000F
ARXR1PGA	RW	8	0x0000 0010
ARXL1PGA	RW	8	0x0000 0011
ARXR2PGA	RW	8	0x0000 0012
ARXL2PGA	RW	8	0x0000 0013
VRXPGA	RW	8	0x0000 0014
VSTPGA	RW	8	0x0000 0015
VRX2ARXPGA	RW	8	0x0000 0016
AVDAC_CTL	RW	8	0x0000 0017
ARX2VTXPGA	RW	8	0x0000 0018
ARXL1_APGA_CTL	RW	8	0x0000 0019
ARXR1_APGA_CTL	RW	8	0x0000 001A
ARXL2_APGA_CTL	RW	8	0x0000 001B
ARXR2_APGA_CTL	RW	8	0x0000 001C
ATX2ARXPGA	RW	8	0x0000 001D
BT_IF	RW	8	0x0000 001E
BTPGA	RW	8	0x0000 001F
BTSTPGA	RW	8	0x0000 0020
EAR_CTL	RW	8	0x0000 0021

Table 2-25. AUDIO_VOICE Register Summary (TPS65930 Only) (continued)

Register Name	Type	Register Width (Bits)	Physical Address
HS_SEL	RW	8	0x0000 0022
HS_GAIN_SET	RW	8	0x0000 0023
HS_POPN_SET	RW	8	0x0000 0024
PREDL_CTL	RW	8	0x0000 0025
PREDR_CTL	RW	8	0x0000 0026
PRECKL_CTL	RW	8	0x0000 0027
PRECKR_CTL	RW	8	0x0000 0028
HFL_CTL	RW	8	0x0000 0029
HFR_CTL	RW	8	0x0000 002A
ALC_CTL	RW	8	0x0000 002B
ALC_SET1	RW	8	0x0000 002C
ALC_SET2	RW	8	0x0000 002D
BOOST_CTL	RW	8	0x0000 002E
SOFTVOL_CTL	RW	8	0x0000 002F
DTMF_FREQSEL	RW	8	0x0000 0030
DTMF_TONEXT1H	RW	8	0x0000 0031
DTMF_TONEXT1L	RW	8	0x0000 0032
DTMF_TONEXT2H	RW	8	0x0000 0033
DTMF_TONEXT2L	RW	8	0x0000 0034
DTMF_TONOFF	RW	8	0x0000 0035
DTMF_WANONOFF	RW	8	0x0000 0036
I2S_RX_SCRAMBLE_H	RW	8	0x0000 0037
I2S_RX_SCRAMBLE_M	RW	8	0x0000 0038
I2S_RX_SCRAMBLE_L	RW	8	0x0000 0039
APLL_CTL	RW	8	0x0000 003A
DTMF_CTL	RW	8	0x0000 003B
DTMF_PGA_CTL2	RW	8	0x0000 003C
DTMF_PGA_CTL1	RW	8	0x0000 003D
MISC_SET_1	RW	8	0x0000 003E
PCMBTMUX	RW	8	0x0000 003F
RX_PATH_SEL	RW	8	0x0000 0043
VDL_APGA_CTL	RW	8	0x0000 0044
VIBRA_CTL	RW	8	0x0000 0045
VIBRA_SET	RW	8	0x0000 0046
ANAMIC_GAIN	RW	8	0x0000 0048
MISC_SET_2	RW	8	0x0000 0049

2.6.3.2 General-Purpose Input/Output (GPIO)

Table 2-26. GPIO Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
GPIODATAIN1	R	8	0x0000 0098
GPIODATAIN2	R	8	0x0000 0099
GPIODATAIN3	R	8	0x0000 009A
GPIODATADIR1	RW	8	0x0000 009B
GPIODATADIR2	RW	8	0x0000 009C
GPIODATADIR3	RW	8	0x0000 009D

Table 2-26. GPIO Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address
GPIODATAOUT1	RW	8	0x0000 009E
GPIODATAOUT2	RW	8	0x0000 009F
GPIODATAOUT3	RW	8	0x0000 00A0
CLEARGPIODATAOUT1	RW	8	0x0000 00A1
CLEARGPIODATAOUT2	RW	8	0x0000 00A2
CLEARGPIODATAOUT3	RW	8	0x0000 00A3
SETGPIODATAOUT1	RW	8	0x0000 00A4
SETGPIODATAOUT2	RW	8	0x0000 00A5
SETGPIODATAOUT3	RW	8	0x0000 00A6
GPIO_DEBEN1	RW	8	0x0000 00A7
GPIO_DEBEN1	RW	8	0x0000 00A7
GPIO_DEBEN3	RW	8	0x0000 00A9
GPIO_CTRL	RW	8	0x0000 00AA
GPIOPUPDCTR1	RW	8	0x0000 00AB
GPIOPUPDCTR2	RW	8	0x0000 00AC
GPIOPUPDCTR3	RW	8	0x0000 00AD
GPIOPUPDCTR4	RW	8	0x0000 00AE
GPIOPUPDCTR5	RW	8	0x0000 00AF
GPIO_TEST	RW	8	0x0000 00B0
GPIO_ISR1A	RW	8	0x0000 00B1
GPIO_ISR2A	RW	8	0x0000 00B2
GPIO_ISR3A	RW	8	0x0000 00B3
GPIO_IMR1A	RW	8	0x0000 00B4
GPIO_IMR2A	RW	8	0x0000 00B5
GPIO_IMR3A	RW	8	0x0000 00B6
GPIO_ISR1B	RW	8	0x0000 00B7
GPIO_ISR2B	RW	8	0x0000 00B8
GPIO_ISR3B	RW	8	0x0000 00B9
GPIO_IMR1B	RW	8	0x0000 00BA
GPIO_IMR2B	RW	8	0x0000 00BB
GPIO_IMR3B	RW	8	0x0000 00BC
GPIO_SIR1	RW	8	0x0000 00BD
GPIO_SIR2	RW	8	0x0000 00BE
GPIO_SIR3	RW	8	0x0000 00BF
GPIO_EDR1	RW	8	0x0000 00C0
GPIO_EDR2	RW	8	0x0000 00C1
GPIO_EDR3	RW	8	0x0000 00C2
GPIO_EDR4	RW	8	0x0000 00C3
GPIO_EDR5	RW	8	0x0000 00C4
GPIO_SIH_CTRL	RW	8	0x0000 00C5

2.6.3.3 Interface Bit Register (INTBR)

Table 2-27. INTBR Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
IDCODE_7_0	R	8	0x0000 0085
IDCODE_15_8	R	8	0x0000 0086

Table 2-27. INTBR Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address
IDCODE_23_16	R	8	0x0000 0087
IDCODE_31_24	R	8	0x0000 0088
DIEID_7_0	R	8	0x0000 0089
DIEID_15_8	R	8	0x0000 008A
DIEID_23_16	R	8	0x0000 008B
DIEID_31_24	R	8	0x0000 008C
DIEID_39_32	R	8	0x0000 008D
DIEID_47_40	R	8	0x0000 008E
DIEID_55_48	R	8	0x0000 008F
DIEID_63_56	R	8	0x0000 0090
GPBR1	RW	8	0x0000 0091
PMBR1	RW	8	0x0000 0092
PMBR2	RW	8	0x0000 0093
GPPUPDCTR1	RW	8	0x0000 0094
GPPUPDCTR2	RW	8	0x0000 0095
GPPUPDCTR3	RW	8	0x0000 0096
UNLOCK_TEST_REG	RW	8	0x0000 0097

NOTE: Access to the following registers is protected:

- IDCODE_7_0
- IDCODE_15_8
- IDCODE_23_16
- IDCODE_31_24
- DIEID_7_0
- DIEID_15_8
- DIEID_23_16
- DIEID_31_24
- DIEID_39_32
- DIEID_47_40
- DIEID_55_48
- DIEID_63_56

To read these registers, the UNLOCK_TEST_REG register must first be written with 0x49.

Table 2-28. GPPUPDCTR1

Address Offset	0x0F		
Physical Address	0x0000 0094	**Instance**	INT_SCINTBR
Description	This register is the generic pullup/pulldown control register for the I^2C pad (SmartReflex I^2C and T2 internal common register I^2C buses). By default, the external PU resistor should be connected. But because a 3KΩ±30% resistor is available inside the pad, this can be connected, as the default is VMODE2/POWEROK2 on the I2C_SR line. Pad muxing is controlled by the power module register. The default value is pullup. See the device data manual for more information about the use of the pullups.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED	SR_I2C_SDA_CTRL_PU	RESERVED	SR_I2C_SCL_CTRL_PU	RESERVED	I2C_SDA_CTRL_PU	RESERVED	I2C_SCL_CTRL_PU

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved for spare	RW	0
6	SR_I2C_SDA_CTRL_PU		RW	1
		0x0: Pullup is disabled.		
		0x1: Pullup is enabled.		
5	Reserved	Reserved for spare	RW	0
4	SR_I2C_SCL_CTRL_PU		RW	1
		0x0: Pullup is disabled.		
		0x1: Pullup is enabled.		
3	Reserved	Reserved for spare	RW	0
2	I2C_SDA_CTRL_PU		RW	1
		0x0: Pullup is disabled.		
		0x1: Pullup is enabled.		
1	Reserved	Reserved for spare	RW	0
0	I2C_SCL_CTRL_PU		RW	1
		0x0: Pullup is disabled.		
		0x1: Pullup is enabled.		

2.6.3.4 Primary Interrupt Handler (PIH)

Table 2-29. PIH Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
PIH_ISR_P1	RW	8	0x0000 0081
PIH_ISR_P2	RW	8	0x0000 0082
PIH_SIR	RW	8	0x0000 0083

2.6.3.5 Test

Table 2-30. Test Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
AUDIO_TEST_CTL	RW	8	0x0000 004C
INT_TEST_CTL	RW	8	0x0000 004D
DAC_ADC_TEST_CTL	RW	8	0x0000 004E
RXTX_TRIM_IB	RW	8	0x0000 004F
CLD_CONTROL	RW	8	0x0000 0050
CLD_MODE_TIMING	RW	8	0x0000 0051
CLD_TRIM_RAMP	RW	8	0x0000 0052
CLD_TESTV_CTL	RW	8	0x0000 0053
APLL_TEST_CTL	RW	8	0x0000 0054
APLL_TEST_DIV	RW	8	0x0000 0055
APLL_TEST_CTL2	RW	8	0x0000 0056
APLL_TEST_CUR	RW	8	0x0000 0057
DIGMIC_BIAS1_CTL	RW	8	0x0000 0058
DIGMIC_BIAS2_CTL	RW	8	0x0000 0059
RX_OFFSET_VOICE	R	8	0x0000 005A
RX_OFFSET_AL1	R	8	0x0000 005B
RX_OFFSET_AR1	R	8	0x0000 005C
RX_OFFSET_AL2	R	8	x0000 005D
RX_OFFSET_AR2	R	8	0x0000 005E
OFFSET1	R	8	0x0000 005F
OFFSET2	R	8	0x0000 0060

2.6.4 Address Group - 12 Hex (SMARTREFLEX_REG)

Table 2-31. SMARTREFLEX_REG Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
VDD1_SR_CONTROL	RW	8	0x0000 0000
VDD2_SR_CONTROL	RW	8	0x0000 0001

Clocks

This chapter describes the clocks of the device integrated power-management/audio coder/decoder (codec) device.

Topic **Page**

3.1 Device Clocks Overview

The devices use several clocks, including many in the submodules that enable specific features. This chapter describes the clock sources from which all other clocks derive their synchronization. Specialized clock circuits, such as those used in the audio and universal serial bus (USB) subchips, are discussed in the appropriate TRM chapters.

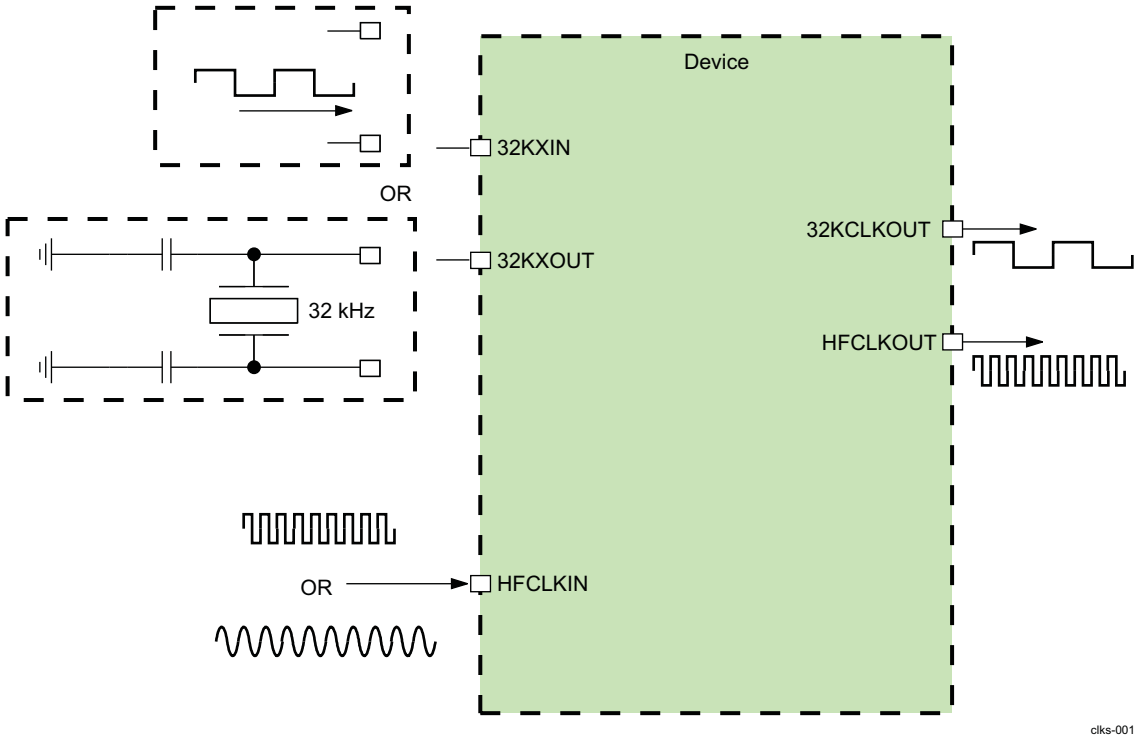
3.1.1 Oscillators Versus Clocks

In this TRM, the difference between oscillators and clocks is negligible. An oscillator is a source of sinusoidal signals used with analog circuitry; a clock provides square-waves, as used in digital logic. Both terms mean a source of an alternating signal having controlled frequency and amplitude variations that fall within specified limits.

3.1.2 Clock Sources

The device has two sources of high-stability clock signals: the external high-frequency clock (HFCLKIN) input and an onboard 32-kHz oscillator (an external 32-kHz signal can be injected). Figure 3-1 shows these options.

Figure 3-1. Clock Sources



3.1.2.1 External HFCLKIN

The device derives its overall synchronization from the externally supplied clock signal, HFCLKIN.

Table 3-1 lists the frequencies that the device can accept for HFCLKIN. In some applications, 26 MHz is preferred, because certain features of the device audio section are not available without it (for more information, see Chapter 13, *Audio*).

When 26 MHz is used for HFCLKIN, it must come from the same system clock that supplies the audio codec.

Table 3-1 lists the external HFCLKIN clock frequencies.

Table 3-1. External HFCLKIN Clock Frequencies

Clock Type	Frequency (MHz)
Digital	19.2, 26, 38.4
Sine	19.2, 26, 38.4

When HFCLKIN is present, the 32-kHz crystal oscillator and the three 3-MHz resistance-capacitive (RC) oscillators in the device are synchronized with it (see Section 3.4.4, *3-MHz RC Oscillators*).

3.1.2.2 32-kHz Clock

The device 32-kHz clock (32.768 kHz) circuit can function with an externally supplied digital signal or a quartz crystal. The 32-kHz clock drives the real-time clock (RTC), which is used by the device for various functions.

3.1.2.3 RTC

The RTC generates and maintains time and provides alarm-clock functions that include the following:

- Time information (seconds/minutes/hours) directly in binary-coded decimal (BCD) code
- Calendar information (day/month/year/day of the week) directly in BCD code, up to the year 2099
- Interrupt generation, periodically (1 second/1 minute/1 hour/1 day) or at a precise time (alarm function)
- 30-second time correction

3.2 Clock Environment

3.2.1 Clock Request—HFCLKOUT

When an external device requires a clock signal other than 32 kHz from the device, it must set the CLKREQ pin to 1. A rising edge on the CLKREQ pin leads to a SLEEP-to-ACTIVE transition on P3. When this transition occurs, the resources activated depend on the sequence programmed in the power-management sequencing memory (for more information, see *Section 5.4.9.2, SLEEP ON and SLEEP OFF Transitions*, in Chapter 5, *Resets and Power Management*). The SLEEP OFF sequence must be configured to set the CLKEN signal to 1 to notify the system clock provider of the clock request and start a timer. When the timer expires, the device opens a gated clock, the timer automatically reloads the defined value, and a high-frequency output clock signal is available through the HFCLKOUT pin. nSLEEP1 can be used in the same way if CLKEN and HFCLKOUT are linked to P1/P2. The output drive of the HFCLKOUT pin is programmable for two capacitive loads (10 pF or 40 pF); it should be set to 40 pF by default.

3.2.2 32KCLKOUT

Regardless of whether the device 32-kHz oscillator circuit runs directly from a crystal or from an external 32-kHz signal, the device buffers the resulting 32-kHz signal and provides it as 32KCLKOUT, which can be provided externally to the application processor or other devices. The default mode of the 32KCLKOUT signal is active, but it can be disabled.

3.2.3 External 32-kHz Slave Mode Operation

- In master mode:

  When the device oscillator is connected to an external 32.768-kHz crystal through the 32KXIN/32KXOUT balls, 32KCLK is available when the device power-on reset (POR) is released.

  When the device oscillator is connected to an external digital 32.768-kHz clock through 32KXIN input, the device POR is released only when the external digital clock is available. Software can enable the oscillator mode after the first start.

- In slave mode:

  When the device is configured in slave mode (operates under the control of an external controller), the internal 32-kHz oscillator circuitry is bypassed and an external 32-kHz signal is required.

3.2.4 Setting and Enabling the RTC

The 32.768-kHz clock drives the RTC embedded in the device. The RTC is not enabled by default; the host processor must set the correct date and time to enable the RTC.

3.3 Clock Integration

3.3.1 Device Internal Clock Distribution

The device receives an external HFCLKIN signal and uses it to synchronize or generate the clocks required to operate the device subsystems. Figure 3-2 and Figure 3-3 are overviews of clock distribution in the device.

Figure 3-2. Device Internal Clock Distribution–Clock Sources and Controls

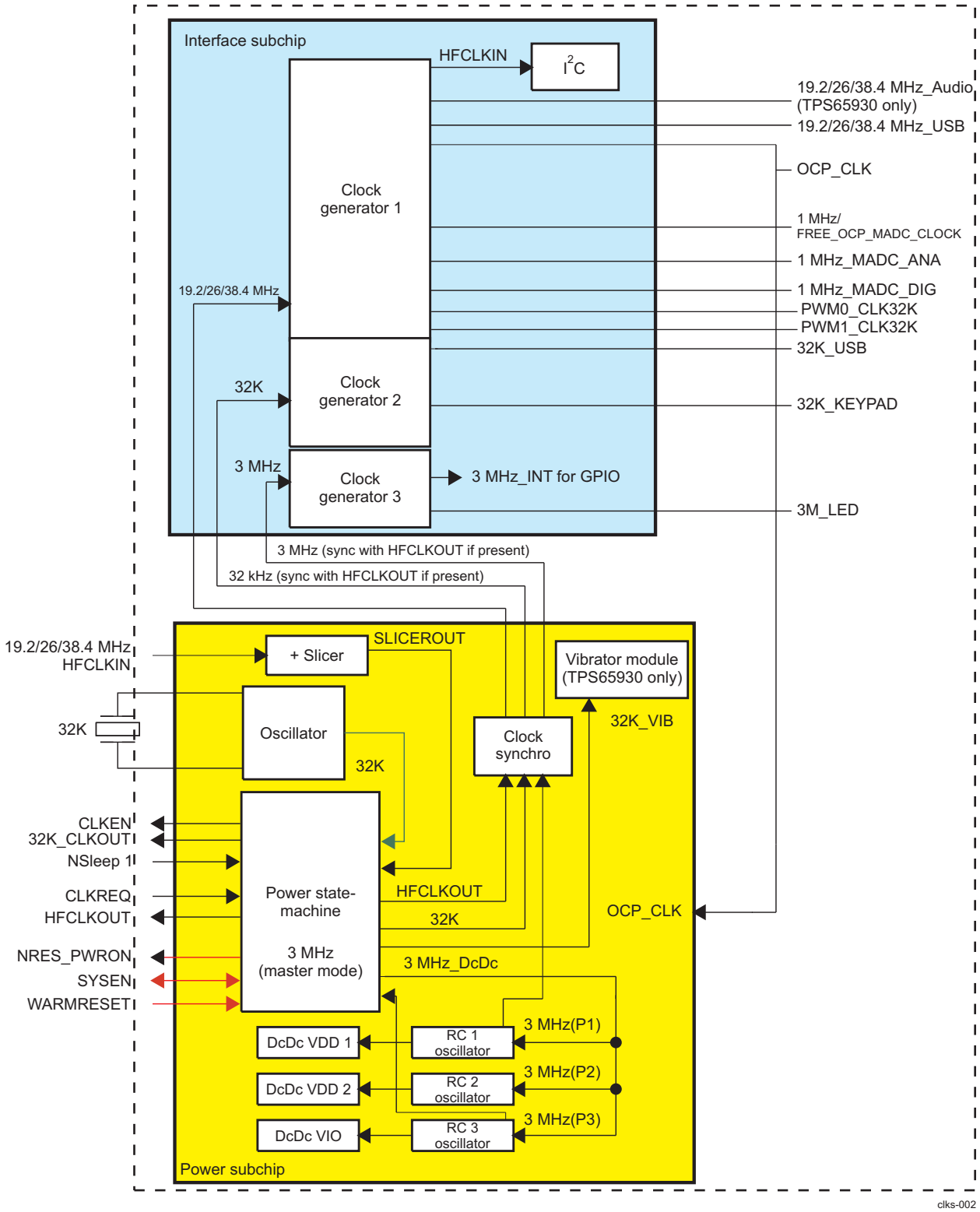
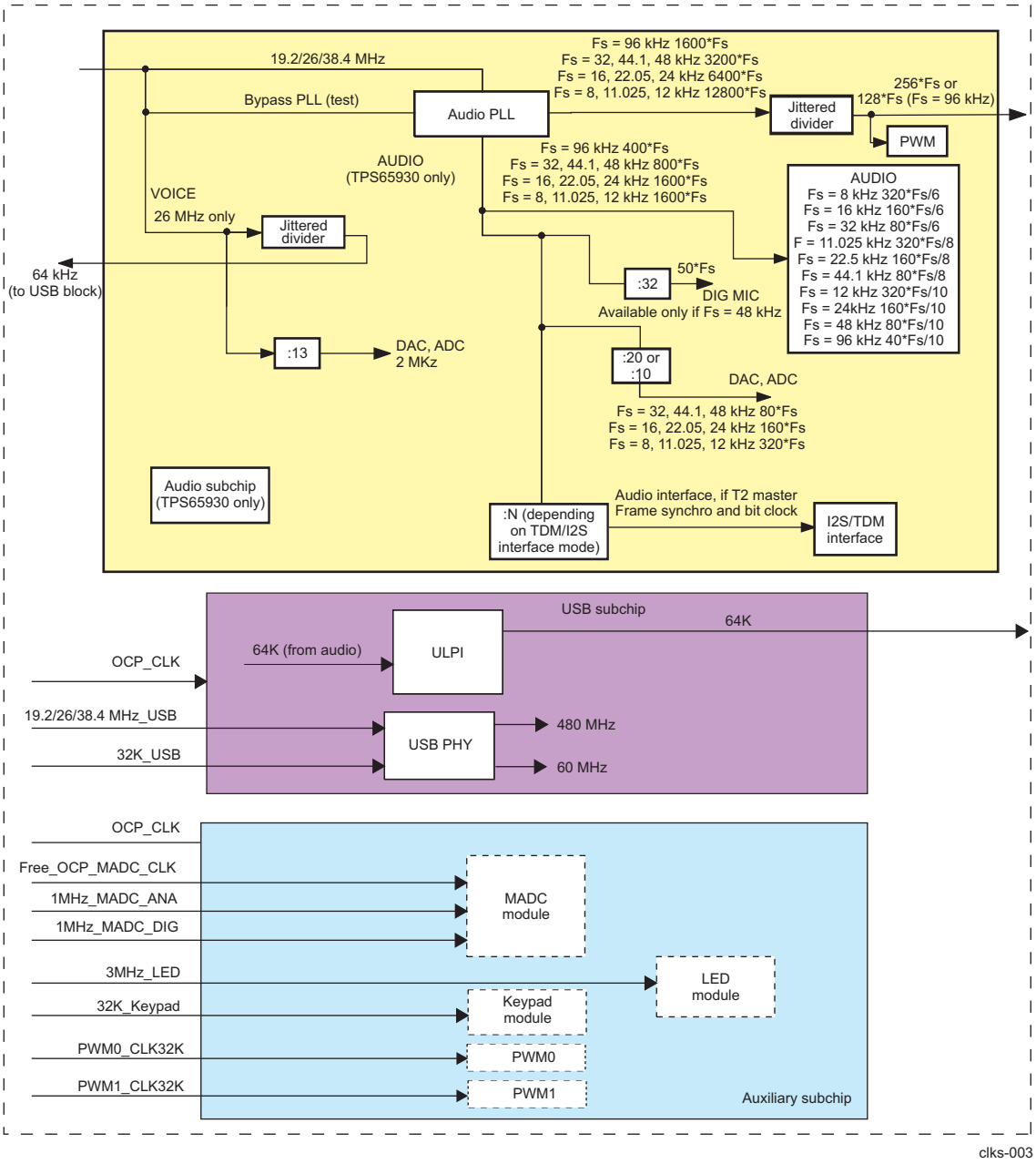


Figure 3-3. Device Clock Distribution–Clock Recipients



3.3.2 Clock Controls and Signals

The device clock resources provide a series of clock signals to the subchips:

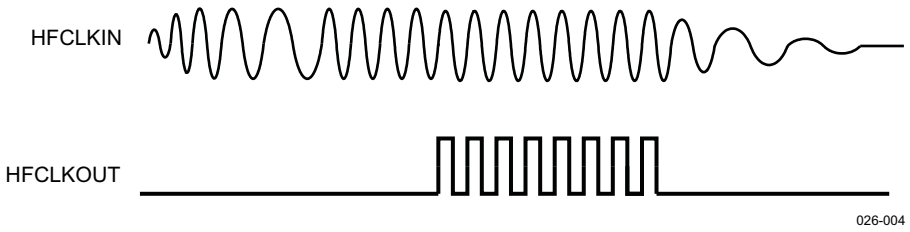
- Equalities:
  - MCLK = System clock = HFCLK
  - Open-core protocol (OCP) clock = 1/2 system clock
  - MCLK_FREQ = Signal identifying the system clock frequency (used by audio and USB)
- Monitoring analog-to-digital converter (ADC) (MADC):
  - MADC_CLK1M: 1-MHz digital clock
  - MADC_CLK1M_ANA: 1-MHz analog clock
  - MADC_CLKFREE1M: Always available 1-MHz clock; not gated

  - MADC_CLKOCP: OCP interface gated clock
  - MADC_CLKFREEOCP: Always available OCP clock; not gated
- LED:
  - LED_CLK32K_3M_Req: 3-MHz clock request
  - LED_CLK_3MHz: 3-MHz digital clock
  - OCP_CLK: OCP interface gated clock
- PWM0 and PWM1 generators:
  - PWM0_CLK32K (for PWM0): 32-kHz clock
  - PWM1_CLK32K (for PWM1): 32-kHz clock
- Keypad/keyboard controller:
  - KEYP_CLK32K: 32-kHz digital clock
  - OCP_CLK: OCP clock
- Audio subchip (TPS65930 only):
  - AUDIO_MCLK: System clock (MCLK_FREQ identifies the frequency)
- USB
  - USB_MCLK_Req: System clock request
  - USB_MCLK: System clock (MCLK_FREQ identifies the frequency)
  - USB_CLK32K: 32-kHz clock
  - USB_CLK1M: 1-MHz clock
  - OCP_CLK: OCP interface clock

3.3.2.1 HFCLKIN

Figure 3-4 shows the behavior of HFCLKOUT (the filtered derivation of HFCLKIN).

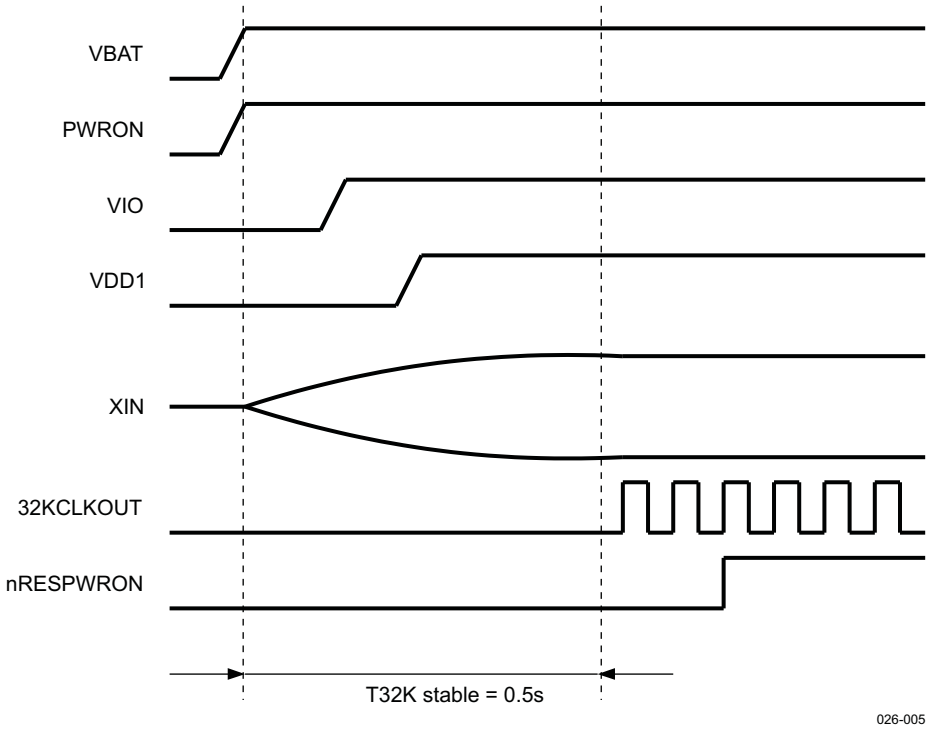
Figure 3-4. HFCLKOUT



3.3.2.2 32-kHz Oscillator Stabilization

When the 32-kHz oscillator starts, a short transition period occurs. During that period, the frequency is not stable, and the signal must not be used until it reaches equilibrium. Figure 3-5 shows the startup sequence.

Figure 3-5. 32-kHz Oscillator Stabilization



3.4 Clock Functional Description

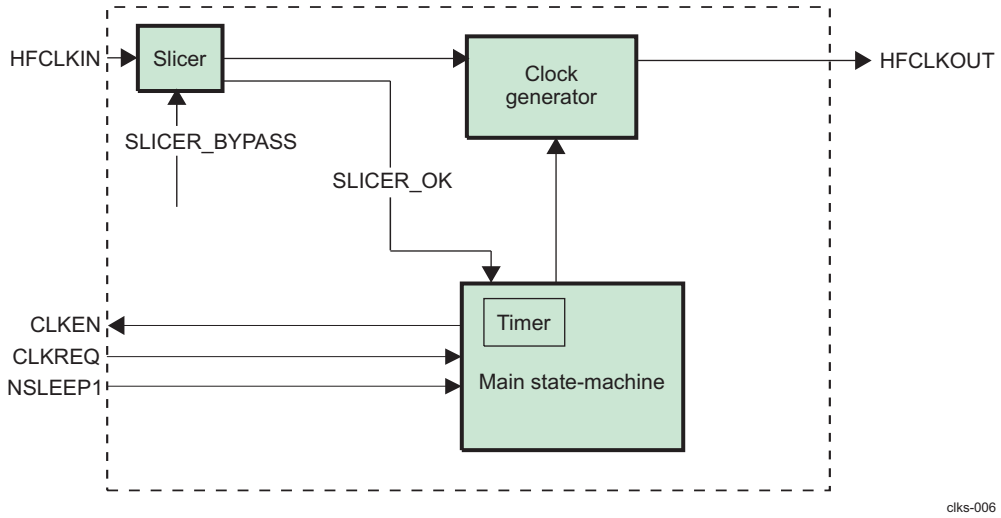
3.4.1 External HFCLKIN

The HFCLKIN signal for the device is provided from an external source.

When the device enters an active state, the external host processor must immediately indicate the HFCLKIN frequency (19.2, 26, or 38.4 MHz) by setting the CFG_BOOT[1:0] HFCLK_FREQ bit field (see Table 3-10). HFCLK_FREQ has a default of not programmed, and in that condition, the USB subsection does not work, the three DC/DC switching supplies (VIO, VDD1, and VDD2) operate from their free-running 3-MHz (RC) oscillators, and the PWR registers are accessed at a default 1.5-MB rate (see Section 3.4.1.2, *PWR Registers Clock Select*). HFCLK_FREQ must be set by the host processor during the initial power-up sequence.

Figure 3-6 is a block diagram of the high-frequency clock circuitry.

Figure 3-6. External HFCLKIN



When HFCLKIN is a sinusoidal signal, the slicer converts it to a square-wave suitable for use with digital logic. The clock generator consists of gating circuitry that ensures a stable signal. The main state-machine, working with the CLKREQ, SLEEP, and CLKEN signals, controls the clock generator and signals to clock users that HFCLK is stable.

3.4.1.1 Clock Slicer

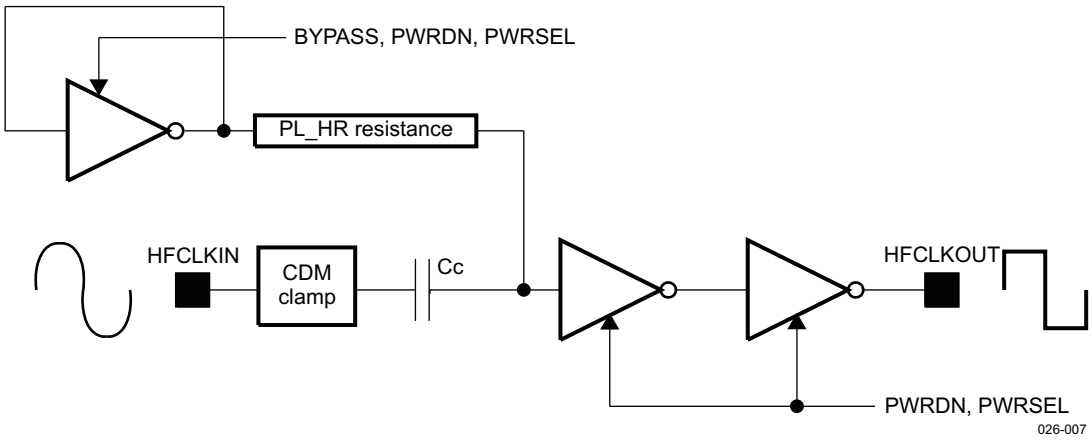
The clock slicer transforms the clock input signal into a squared clock signal used internally by the device and as an external output. The input signal can be one of the following:

- Sinusoid signal for the slicer mode
- Square clock signal for the bypass mode

For more information about HFCLKIN input signal amplitude, see the device data manual.

Figure 3-7 shows the clock slicer design.

Figure 3-7. Clock Slicer Block Diagram



When a digital external clock is supplied, the slicer can be disabled.

3.4.1.2 PWR Register Clock Select

When the external HF clock signal is 19.2 MHz, a problem can occur in accessing the registers in the power subchip, depending on the clock rate used to access the registers. The situation is the result of a near-integer relationship between the access frequency of the power register and one-half the frequency of the system clock, HFCLK (19.2 MHz).

To prevent this problem, two clock rates are used, depending on the frequency of the HF clock. When the external HF clock is 26 or 38.4 MHz, the power subchip registers are accessed using a 3-MHz clock; when the external HF clock is 19.2 MHz, the registers are accessed at half that frequency (1/2 of 3 MHz = 1.5 MHz).

When power is first applied to the device, the external HF clock frequency is unknown (HFCLK_FREQ has not been set by the host processor). To ensure that the power subchip registers can be accessed, the default register access frequency is 1.5 MHz.

When the host processor executes its software, it must immediately assign the HF clock frequency being sent to the device by setting the CFG_BOOT1:0] HFCLK_FREQ bit field (see Table 3-10). When the HFCLK_FREQ bit field is set, an automatic feature controlled by the BACKUP_MISC_CFG[1] PWR_CLK_MAN bit (see Table 3-11) operates. Unless the PWR_CLK_MAN bit is disabled (discussed in the next paragraph), the clock frequency used to access the register in the power subchip follows the rules that have been described; the power registers are accessed at a 3-MHz rate if the HF clock is 26 or 38.4 MHz; otherwise, a 1.5-MHz frequency is used. Not setting the HFCLK_FREQ bit field is treated as though the bit field is set for a 19.2-MHz HF clock; the power registers are accessed using a 1.5-MHz clock. Not setting the HFCLK_FREQ bit field also causes other problems; see the explanation for the CFG_BOOT register in Table 3-10.

When power is first applied to the device, its defaults for accessing the power subchip registers are as described, but when the host processor accesses these registers, it is possible to disable the automatic setting of the power register access frequency by turning off the PWR_CLK_MAN bit (changing it from its default value of 1 to 0). If the PWR_CLK_MAN bit is disabled, the power registers are accessed using a 1.5-MHz or a 3-MHz frequency, depending on the value set in the BACKUP_MISC_CFG[0] PWR_CLK_FREQ bit (see Table 3-11).

3.4.1.3 MADC Clock Select

A method is required to provide a clock to the MADC section. A default clock is provided based on the assumption that HFCLKIN (the externally supplied HF clock) is 26 MHz (this is a desirable frequency because it provides capabilities in the audio subsection that are not otherwise available).

The GPBR1[4] DEFAULT_MADC_CLK_EN bit (see Table 3-12) controls the default estimate that the HFCLKIN signal is 26 MHz. The default value of the DEFAULT_MADC_CLK_EN bit is 1, and in that condition the MADC subsection is provided a clock based on the assumption that HFCLKIN is 26 MHz. If

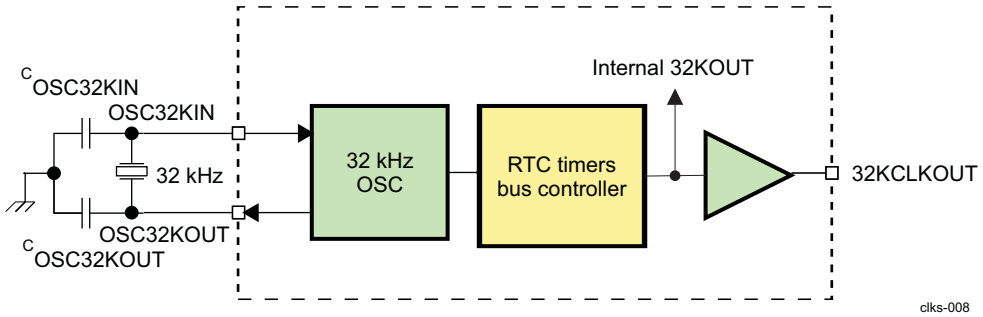
left at its default value (1), the DEFAULT_MADC_CLK_EN bit overrides the value the host processor sets in the CFG_BOOT[1:0] HFCLK_FREQ bit field for the clock sent to the MADC. If the HFCLKIN signal is not 26 MHz, DEFAULT_MADC_CLK_EN must be disabled (set to 0) by the host processor during the initial power-up sequence; therefore, the determination of the MADC clock frequency is based on the HFCLK_FREQ bit setting. If the DEFAULT_MADC_CLK_EN bit is to be disabled, it must be done before setting the HFCLK_FREQ bit field.

3.4.2 32-kHz Clock

The 32-kHz clock drives the RTC circuitry. When the external HFCLKIN signal is available, the 32-kHz oscillator is synchronized with it. If HFCLKIN is not available but the device is powered, the 32-kHz oscillator is synchronized with the 3-MHz RC oscillators.

Figure 3-8 is a block diagram of the 32-kHz clock.

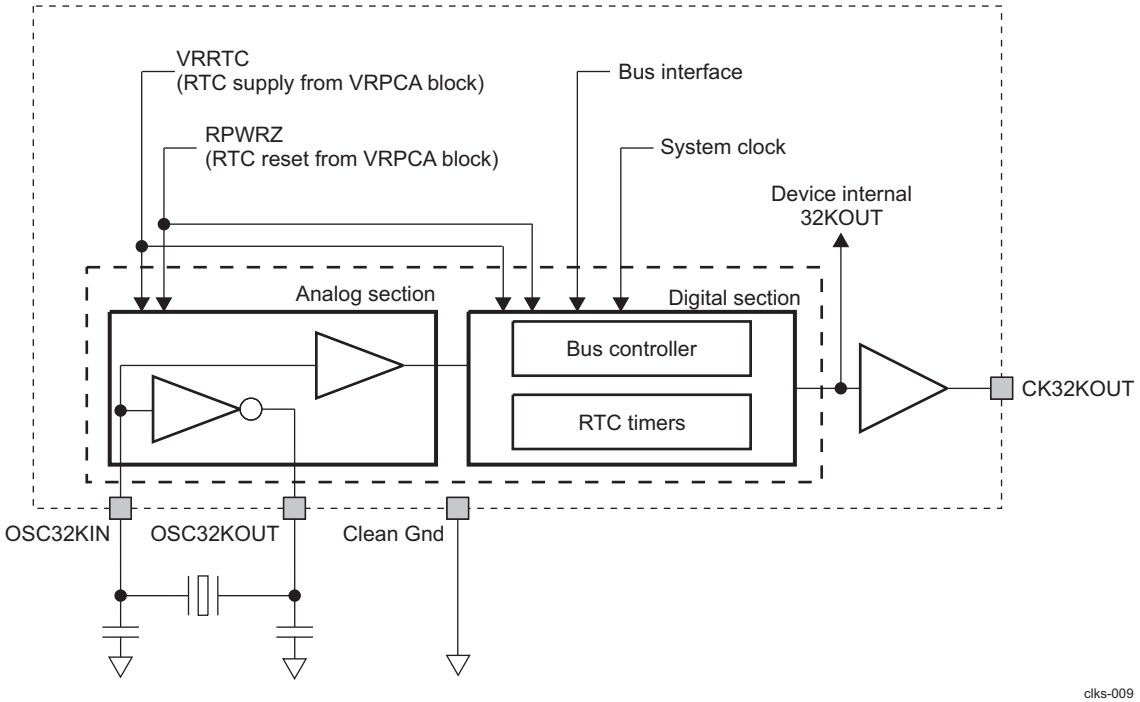
Figure 3-8. 32-kHz Clock



3.4.3 RTC

The RTC, which is driven by the 32-kHz oscillator, provides alarm and timekeeping functions (see Figure 3-9).

Figure 3-9. RTC



3.4.3.1 RTC Digital Section

3.4.3.1.1 Overview

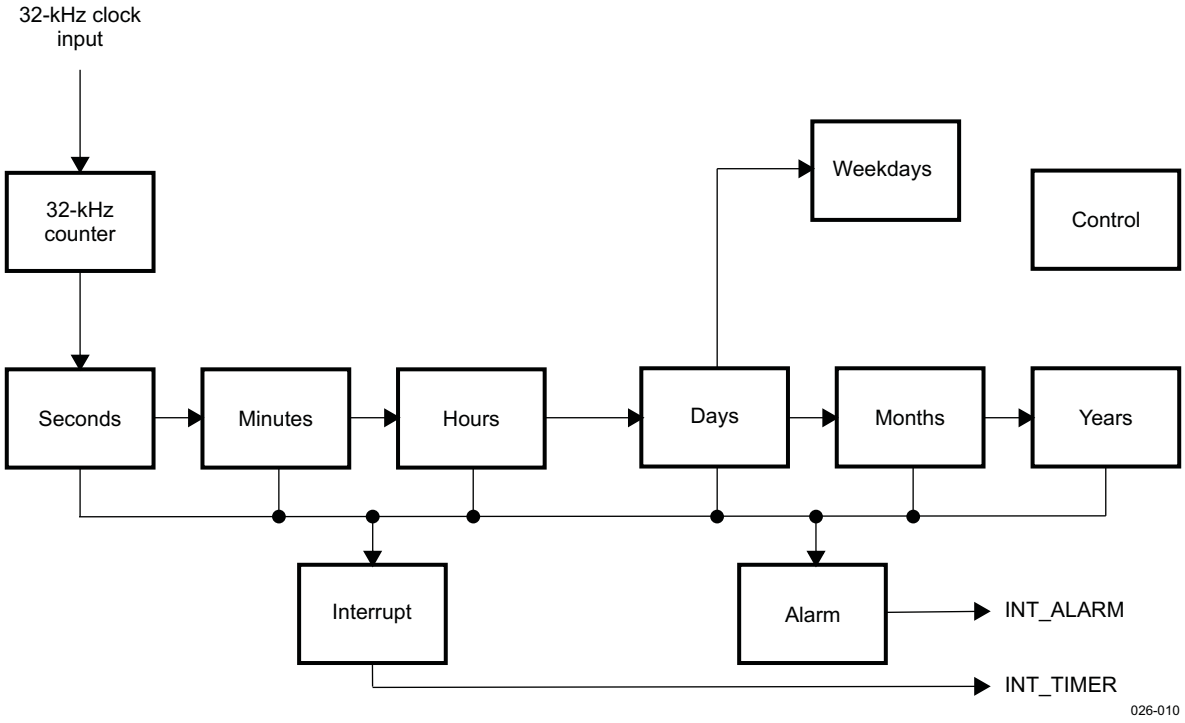
The RTC performs the following basic functions:

- Time information (seconds/minutes/hours) directly in BCD code
- Calendar information (day/month/year/day of the week) directly in BCD code up to the year 2099
- Interrupt generation periodically (1 second/1 minute/1 hour/1 day) or at a precise time (alarm function)
- 30-second time correction

3.4.3.1.2 Block Diagram

Figure 3-10 is a block diagram of the RTC digital section.

Figure 3-10. RTC Digital Section Block Diagram



3.4.3.1.3 Register Descriptions

All time and calendar information is available in dedicated BCD time-and-calendar (TC) registers, as follows:

- YEARS_REG register: Year data ranges from 00 to 99:
  - Leap year: Year divisible by 4 (2000, 2004, 2008, 2012, ...)
  - Common year: Other years
- MONTHS_REG register: Month data ranges from 01 to 12.
- DAYS_REG register: Day value ranges from:
  - 1 to 31 when months are 1, 3, 5, 7, 8, 10, 12
  - 1 to 30 when months are 4, 6, 9, 11
  - 1 to 29 when month is 2 and year is a leap year
  - 1 to 28 when month is 2 and year is a common year
- WEEKS_REG register: Week value ranges from 0 to 6.
- HOURS_REG register: Hour value ranges from 00 to 23 in 24-hour mode, and from 1 to 12 in AM/PM mode.

- MINUTES_REG register: Minutes value ranges from 0 to 59.
- SECONDS_REG register: Seconds value ranges from 0 to 59.

3.4.3.1.4 Setting Time and Calendar Information

Modifying TC registers

To modify the current time, an external processor writes a new time into the TC registers. The TC registers can be written to without stopping the RTC.

The external processor can stop the RTC by writing 0 to the RTC_CTRL_REG[0] STOP_RTC bit, update the TC register values, and then restart the RTC by setting the STOP_RTC bit to 1. TC registers are secured registers.

Rounding Seconds

Time in the RTC can be rounded to the nearest minute by setting the RTC_CTRL_REG[1] ROUND_30S bit to 1. TC register values are set to the closest minute during the next second. The ROUND_30S bit is automatically cleared when rounding is performed.

Examples:

- If the current time is 10H 59M 45S, setting the ROUND_30S bit to 1 changes the time (the next second) to 11H 00M 00S.
- If the current time is 10H 59M 29S, setting the ROUND_30S bit to 1 changes the time (the next second) to 10H 59M 00S.

3.4.3.1.5 Managing Interrupts

The RTC can generate two interrupts: a timer interrupt (INT_TIMER) and an alarm interrupt (INT_ALARM).

INT_TIMER

The RTC_INTERRUPTS_REG[2] INT_TIMER bit can be selected to trigger every second, minute, hour, or day by setting it to 1. When the timer interrupt function triggers an interrupt, the external processor can examine bits [2:5] in the RTC_STATUS_REG register to determine which IT_TIMER setting caused the interrupt. (If the external processor knows the IT_TIMER setting, checking bits [2:5] is not required.)

Setting the RTC_INTERRUPTS_REG register to shorter time increments results in an interrupt also being generated when longer time intervals are reached (see Table 3-2).

Table 3-2. INT_TIMER

RTC_INTERRUPTS_REG[1:0] RTC_STATUS_REG[5:2]	3	2	1	0
1D_EVENT	1	0/1 See (1).	0/1 See (1).	0/1 See (1).
1H_EVENT	1	1	0/1 See (1).	0/1 See (1).
1M_EVENT	1	1	1	0/1 See (1).
1S_EVENT	1	1	1	1

(1) Set to 1 when this event is concurrent with the programmed periodical period

Examples:

- When an interrupt every second is selected (bits [1:0] of the RTC_ INTERRUPTS_REG register are set to 0 and 0, respectively), an alignment synchronized with the second and with the minute occurs every 60 interrupts.
- When an interrupt every hour is selected (bits [1:0] of RTC_ INTERRUPTS_REG are set to 2 and 0, respectively), an alignment synchronized with the hour and with the day occurs every 24 interrupts.

INT_ALARM

INT_ALARM can be generated when the time set in the TC ALARM registers (of the same number and configuration as the TC registers) is the same as in the TC registers. INT_ALARM is generated if the RTC_INTERRUPTS_REG[3] IT_ALARM bit is set. This interrupt is low-level sensitive. The RTC_STATUS_REG[6] ALARM bit indicates that INT_ALARM occurred. The alarm interrupt is disabled by writing 1 to the RTC_STATUS_REG[6] ALARM bit.

3.4.3.1.6 32-kHz Oscillator Drift Compensation

A compensation mechanism accounts for inaccuracy in the 32-kHz oscillator. In the compensation procedure, the external processor calculates the drift of the 32-kHz oscillator and then loads the compensation registers (RTC_COMP_LSB_REG and RTC_COMP_MSB_REG) with the drift compensation value calculated during the measurement. If the RTC_CTRL_REG[2] AUTO_COMP bit is enabled, the COMP_REG value (in twos complement) is added to the RTC 32-kHz counter each hour and 1 second. When COMP_REG is added to the RTC 32-kHz counter, the duration of the current second becomes [(32768 – COMP_REG)/32768] seconds; therefore, it is possible to compensate the RTC with 1/32768-second time unit accuracy each hour.

The steps described are an outline of the required calibration process. This discussion does not include details about the requirement to provide an accurate external frequency reference and suitable software on the external processor to perform the calibration procedure. Table 3-3 shows the distribution of responsibilities between the RTC and the external processor for drift compensation.

Table 3-3. Task Distribution Between External Processor and RTC for Drift Compensation

External Processor	RTC
Measure the 32-kHz oscillator drift.	
Calculate the drift compensation for 1 hour.	
	Every hour, drift compensation value is added to the RTC 32-kHz counter.

3.4.3.2 RTC Registers

This section lists the registers used by the RTC.

Example:

The time is 10H 54M 36S PM (PM_AM mode is set), the 5th of September, 1997 (HOURS_REG is 9 because it starts at 0).

TC register values:

SECONDS_REG	0x36
MINUTES_REG	0x54
HOURS_REG	0x90
DAYS_REG	0x05
MONTHS_REG	0x09
YEARS_REG	0x97

- TC registers, secured with the Msecure pad:
  - SECONDS_REG
  - MINUTES_REG
  - HOURS_REG
  - DAYS_REG
  - MONTHS_REG
  - YEARS_REG
  - WEEKS_REG
- TC alarm registers:
  - ALARM_SECONDS_REG
  - ALARM_MINUTES_REG

  - ALARM_HOURS_REG
  - ALARM_DAYS_REG
  - ALARM_MONTHS_REG
  - ALARM_YEARS_REG
- General register:
  - RTC_CTRL_REG
- RTC_INTERRUPTS_REG
- RTC_STATUS_REG

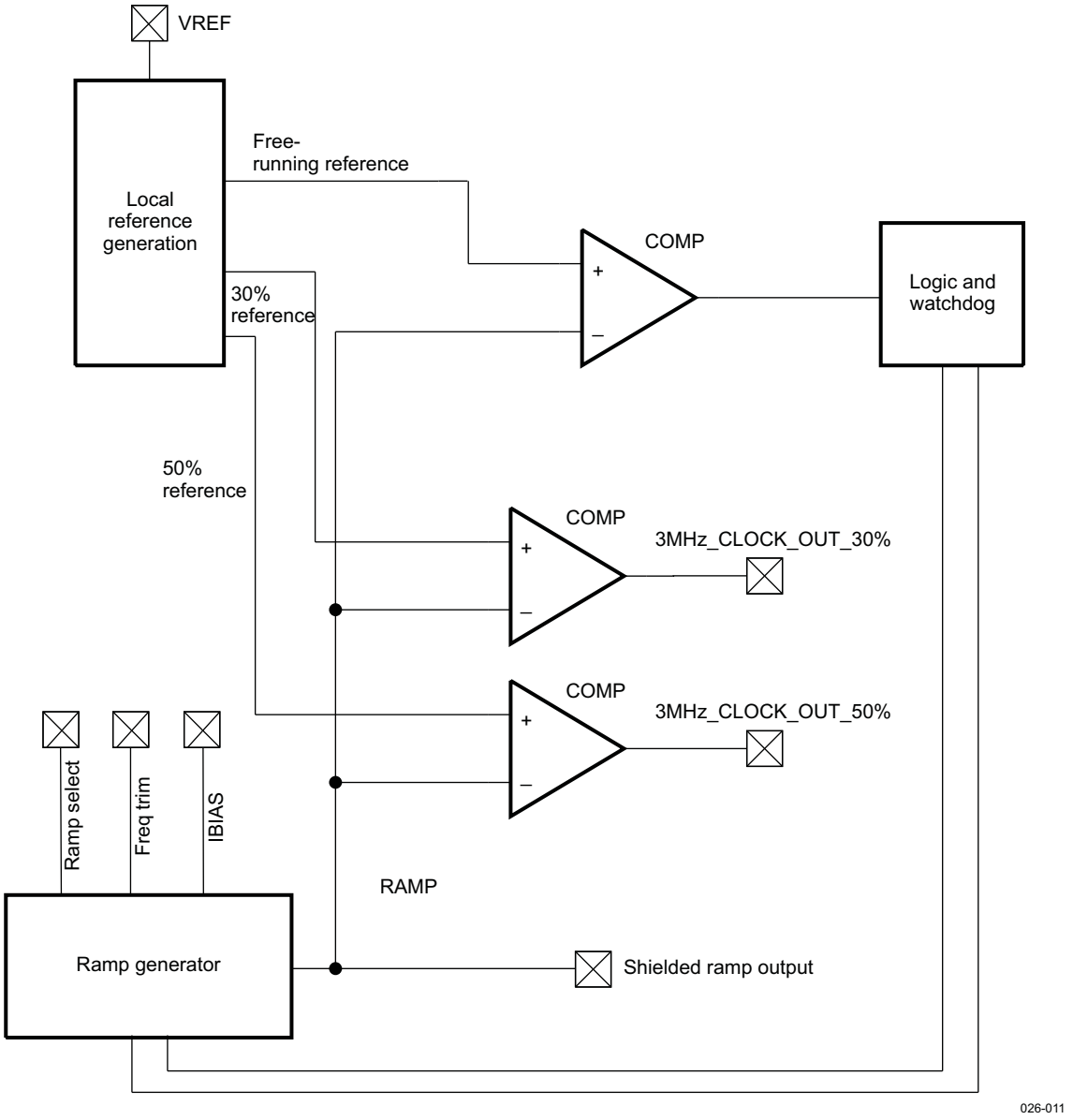
  The alarm interrupt is low until an external processor writes 1 to the ALARM bit of the RTC_STATUS_REG register. POWER_UP is set by a reset and cleared by writing 1 to it.
- Compensation registers:
  - RTC_COMP_MSB_REG
  - RTC_COMP_LSB_REG

3.4.4 3-MHz RC Oscillators

The device has three internal RC oscillators that free-run at roughly 3 MHz. These oscillators do not have external appearances and are used to clock internal switching regulators. If the external HFCLKIN signal is not present, the 32-kHz oscillator synchronizes with the RC oscillators, if they are operating. If the HFCLKIN signal is present, the 32-kHz oscillator must be synchronized with it, and the RC oscillators must be idled. Figure 3-11 shows the RC oscillators.

The RC oscillators drive the switching regulators for VDD1, VDD2, and VIO. To minimize noise on these power buses, it is desirable to operate the oscillators in a particular phase relationship. This implementation method will be provided in a chapter addendum.

Figure 3-11. Ramp Generator Block Diagram



The following registers are connected to the 3-MHz RC oscillators:

- VIO_OSC
- VDD1_OSC
- VDD2_OSC

3.5 Clock Programming Models

3.5.1 Clock Generator Startup Example

After a valid main battery insertion, the device is in WAIT-ON state. All low-dropout (LDO) regulators are disabled, except VRRTC, which provides the power supply to the 32-kHz internal oscillator.

When the device power-management system recognizes a valid switch-on condition, the power sources are powered up, the power domain is stable, and the 32-kHz and interface clock (3-MHz RC oscillator) are enabled and ready for use.

When the system clock (the externally provided HFCLKIN signal) is available, the clock frequency control backup register must be programmed. The clock generator receives this information from the power subchip to configure its outputs.

When this process completes, the device is ready to deliver clocks to the peripherals when a valid clock request is made.

3.5.2 Setting an Alarm With the RTC

- Preconditions:

  The RTC is set to the correct time and is running.
- Process:
  1. The external processor loads the desired values into the alarm TC registers.
  2. To activate the alarm, the external processor sets the RTC_INTERRUPTS_REG[3] IT_ALARM bit to 1.
  3. When the values in the alarm TC registers match the values in the TC registers, an interrupt is generated.

3.5.3 Responding to an Alarm Interrupt

- Preconditions:

  Because the external processor sets the mode, it must know whether the RTC has interrupts configured for timer interrupt or alarm interrupt. The status of RTC interrupt generation can be confirmed by reading the RTC_INTERRUPTS_REG[2] IT_TIMER and RTC_INTERRUPTS_REG[3] IT_ALARM bits.
- Process:

  If RTC interrupt generation is configured for IT_ALARM, when the external processor detects the interrupt, it recognizes that the RTC reached the alarm time previously set.

  If RTC interrupt generation is configured for IT_TIMER, the external processor must read the RTC_STATUS_REG[5:2] event timer bits to determine which bits are set. If there is uncertainty about the time interval selected, the external processor can read the RTC_INTERRUPTS_REG[1:0] EVERY bit field. After the timer bits are read, they must be reset by writing 0 to them; this prepares them to be triggered during the next interrupt.

3.6 Clock Register Manual

In Table 3-4 through Table 3-20, in registers that contain multiple types of information, clock-related entries are highlighted. Registers that clearly pertain to clocks do not contain highlighting.

NOTE: Use of the names Triton and Triton 2 is a direct reference to the device, indicating that the source information is from the TI product-development organization.

3.6.1 Register Access

The device internal registers are accessed through the inter-integrated circuit (I^2C™) bus.

For more information, see Chapter 2, *Control Interface*.

Table 3-4. PWR_ISR1

Address Offset	0x00		
Physical Address	0x0000 002E	**Instance**	POWERINT
Description	This interrupt status ISR1 register determines which input event triggered the interrupt line int1_n request.		
Type	RW		

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	RESERVED	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset
7	SC_DETECT		RW	0
6	MBCHG		RW	0
5	RESERVED		RW	0
4	HOT_DIE		RW	0
3	RTC_IT		RW	0
2	USB_PRES		RW	0
1	CHG_PRES		RW	0
0	PWRON	Because the PWRON signal is active low, this signal is inverted.	RW	0

Table 3-5. PWR_IMR1

Address Offset	0x01		
Physical Address	0x0000 002F	**Instance**	POWERINT
Description	This interrupt mask IMR1 register lets the user mask the expected transition event from generating an interrupt request on _int1_n.		
Type	RW		

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	RESERVED	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset
7	SC_DETECT	0: Bit unmasked 1: Bit masked	RW	0
6	MBCHG	0: Bit unmasked 1: Bit masked	RW	0
5	RESERVED		RW	0
4	HOT_DIE	0: Bit unmasked 1: Bit masked	RW	0
3	RTC_IT	0: Bit unmasked 1: Bit masked	RW	0

Bits	Field Name	Description	Type	Reset
2	USB_PRES	0: Bit unmasked 1: Bit masked	RW	0
1	CHG_PRES	0: Bit unmasked 1: Bit masked	RW	0
0	PWRON	0: Bit unmasked 1: Bit masked	RW	0

Table 3-6. PWR_ISR2

Address Offset	0x02		
Physical Address	0x0000 0030	**Instance**	POWERINT
Description	This interrupt status ISR2 register determines which input event triggered the interrupt line int2_n request.		
Type	RW		

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	RESERVED	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset
7	SC_DETECT		RW	0
6	MBCHG		RW	0
5	RESERVED		RW	0
4	HOT_DIE		RW	0
3	RTC_IT		RW	0
2	USB_PRES		RW	0
1	CHG_PRES		RW	0
0	PWRON	Because the PWRON signal is active low, this signal is inverted.	RW	0

Table 3-7. PWR_IMR2

Address Offset	0x03		
Physical Address	0x0000 0031	**Instance**	POWERINT
Description	This interrupt mask IMR2 register lets the user mask the expected transition event from generating an interrupt request on _int2_n.		
Type	RW		

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	RESERVED	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset
7	SC_DETECT	0: Bit unmasked 1: Bit masked	RW	0
6	MBCHG	0: Bit unmasked 1: Bit masked	RW	0
5	RESERVED		RW	0
4	HOT_DIE	0: Bit unmasked 1: Bit masked	RW	0
3	RTC_IT	0: Bit unmasked 1: Bit masked	RW	0
2	USB_PRES	0: Bit unmasked 1: Bit masked	RW	0
1	CHG_PRES	0: Bit unmasked 1: Bit masked	RW	0
0	PWRON	0: Bit unmasked 1: Bit masked	RW	0

Table 3-8. PWR_SIR

Address Offset	0x04		
Physical Address	0x0000 0032	**Instance**	POWERINT
Description	For testing, this software interrupt PWR_SIR register allows generation of an interrupt event on the int1_n or int2_n request line by writing 1 to the targeted SIR bit in a specific test mode. This register is protected by the Triton2 global test key (to unlock this key, write B6 at address 97 in the interfaces).		
Type	RW		

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	RESERVED	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset
7	SC_DETECT		RW	0
6	MBCHG		RW	0
5	RESERVED		RW	0
4	HOT_DIE		RW	0
3	RTC_IT		RW	0
2	USB_PRES		RW	0
1	CHG_PRES		RW	0
0	PWRON		RW	0

Table 3-9. PWR_EDR1

Address Offset	0x05		
Physical Address	0x0000 0033	**Instance**	POWERINT
Description	Power edge detection register 1 for PWRON, charger presence, USB presence, and RTC IT (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
RTC_IT_RISING	RTC_IT_FALLING	USB_PRES_RISING	USB_PRES_FALLING	CHG_PRES_RISINGG	CHG_PRES_FALLING	PWRON_RISING	PWRON_FALLING

Bits	Field Name	Description	Type	Reset
7	RTC_IT_RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	1
6	RTC_IT_FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled	RW	1
5	USB_PRES_ RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	1
4	USB_PRES_ FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled	RW	1
3	CHG_PRES_ RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	1
2	CHG_PRES_ FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled	RW	1
1	PWRON_RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	1

Bits	Field Name	Description	Type	Reset
0	PWRON_FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled	RW	1

Table 3-10. CFG_BOOT

Address Offset	0x05−0x05 in 0xE byte increments		
Physical Address	0x0000 003B−0x0000 003B	**Instance**	POWERPM_MASTER
Description	Boot configuration register (backup domain) Write-protected with the KEY_CFG register		
Type	RW		

7	6	5	4	3	2	1	0
CK32K_LOWPWR_EN	BOOT_CFG			HIGH_PERF_SQ	SLICER_BYPASS	HFCLK_FREQ	

Bits	Field Name	Description	Type	Reset
7	CK32K_LOWPWR_EN	0: The 32-kHz oscillator never goes to low-power mode. 1: The 32-kHz oscillator goes to low-power mode if the main battery voltage is low.	RW	0
6:4	BOOT_CFG	BOOT_CFG = (TEST, RESET, BOOT1, BOOT0)	R	0x0
3	HIGH_PERF_SQ	0: Slicer not in high-performance mode 1: Slicer in high-performance mode	RW	1
2	SLICER_BYPASS	0: Slicer not bypassed 1: Slicer bypassed	RW	0
1:0	HFCLK_FREQ	00: Not programmed 01: 19.2 MHz 10: 26 MHz 11: 38.4 MHz The software should program this register during the boot sequence. If this register remains at 00, three events occur: • The internal clock_OK from the slicer is tied to 1. • The DC/DCs cannot use the divided HF clock (they remain on their internal oscillator). • The main clock generator cannot provide the clock to the MADC and the USB.	RW	0x0

Table 3-11. BACKUP_MISC_CFG

Address Offset	0x0C−0x0C in 0xE byte increments		
Physical Address	0x0000 0042−0x0000 0042	**Instance**	POWERPM_MASTER
Description	Write-protected with the KEY_CFG (backup domain)		
Type	R		

7	6	5	4	3	2	1	0
RESERVED						PWR_CLK_MAN	PWR_CLK_FREQ

Bits	Field Name	Description	Type	Reset
7:2	Reserved		R	0x00
1	PWR_CLK_MAN	0: Automatic mode If the HF frequency is set to at least 26 MHz, the power internal clock is set to 3 MHz. If the HF frequency is less than 26 MHz, the power internal clock is set to 1.5 MHz. 1: Manual mode The PWR_CLK_FREQ bit selects the power internal clock frequency.	RW	0
R0	PWR_CLK_FREQ	If PWR_CLK_MAN equals 0: No action If PWR_CLK_MAN equals 1: 0: The power internal clock is set to 3 MHz. 1: The power internal clock is set to 1.5 MHz.	RW	0

Table 3-12. GPBR1

Address Offset	0x0C		
Physical Address	0x0000 0091	**Instance**	INT_SCINTBR
Description	General-purpose bank register. This register includes the PWM0/PWM1 clock-gating feature, PWM enable features (Triton2 PWM spec), and the MADC default clock switch-off bit (the MADC clock is enabled by default). Three other fields are dedicated to the HFCLK/3-MHz software MADC clock switching if the VBAT monitoring function is required in sleep mode.		
Type	RW		

7	6	5	4	3	2	1	0
MADC_HFCLK_EN	MADC_3MHZ_EN	BAT_MON_EN	DEFAULT_MADC_CLK_EN	PWM1_ENABLE	PWM0_ENABLE	PWM1_CLK_ENABLE	PWM0_CLK_ENABLE

Bits	Field Name	Description	Type	Reset
7	MADC_HFCLK_EN	When set to 1 (default), the MADC 1-MHz clock divider based on the HFCLK (26 MHz) clock (not available in sleep mode) is switched on. When 0, the MADC 1-MHz clock divider based on HFCLK is switched off.	RW	1
6	MADC_3MHZ_EN	When set to 1, the MADC 1-MHz clock divider based on the 3-MHz clock (available even when T2 is in sleep mode) is switched on. When 0 (default), the MADC 1-MHz clock divider based on the 3-MHz clock is switched off.	RW	0
5	VBAT_MON_EN	When set to 1, the VBAT monitoring function is enabled in sleep mode; that is, if enabled (MADC_3MHZ_EN = 1), the MADC 1-MHz clock based on the 3-MHz clock divider is connected to MADC. When 0 (default), the feature is not enabled in sleep mode.	RW	0
4	DEFAULT_MADC_CLK_EN	When this bit is 1 (default), the MADC clock is on and equals HFCLK divided by 26. If HFCLK is 26 MHz, the MADC clock is 1 MHz. If HFCLK is not 26 MHz (38.4 MHz or 19.2 MHz), the MADC frequency is 38.4/26 = 1.47 MHz or 19.2/26 = 7.36 MHz. When this bit is cleared, the MADC clock is based on the HFCLK frequency value in the HFCLK _FREQ bit in the CFG_BOOT register; that is, no MADC clock is generated when HFCLK_FREQ is 00 (default).	RW	1

Bits	Field Name	Description	Type	Reset
		When this bit is set, any mechanism of clock gating regarding the MADC clock request is bypassed; that is, power consumption is greater when MADC_DEFAULT_CLK_EN is cleared, because the clock is always provided to MADC, even if it is not requested.		
3	PWM1_ENABLE	0x0: PWM1 output is disabled (see PWM spec). 0x1: PWM1 output is enabled (see PWM spec).	RW	0
2	PWM0_ENABLE	0x0: PWM0 output is disabled (see PWM spec). 0x1: PWM1 output is enabled (see PWM spec).	RW	0
1	PWM1_CLK_ENABLE	0x0: PWM1 clock is disabled. 0x1: PWM1 clock is enabled.	RW	0
0	PWM0_CLK_ENABLE	0x0: PWM0 clock is disabled. 0x1: PWM0 clock is enabled.	RW	0

Table 3-13. SHUNDAN

Address Offset	0x06−0x06 in 0xE byte increments		
Physical Address	0x0000 003C−0x0000 003C	**Instance**	POWERPM_MASTER
Description			
Type	RW		

7	6	5	4	3	2	1	0
Reserved		CNT					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:0	CNT	When VBAT is low, count up to 2 seconds using a 32-kHz clock (32.768 kHz/1024). The default value of this register is 0x3F after the first main battery insertion. The maximum value is 0x3E. This register can be set back to 0x00 by software.	RW	0x3F

Table 3-14. CFG_PWRANA2

Address Offset	0x09−0x09 in 0xE byte increments		
Physical Address	0x0000 003F−0x0000 003F	**Instance**	POWERPM_MASTER
Description	Configuration for PWRANA2 voltage regulator (backup domain)		
	All bits protected with the KEY_TST except VRRTC_SLEEP		
Type	RW		

7	6	5	4	3	2	1	0
VRRTC_DISABLE	VRRTC_SLEEP	VRRTC_TRIEN	VRRTC_TRIM		LOJIT1_LOWV	LOJIT0_LOWV	LOJIT0_LOWV

Bits	Field Name	Description	Type	Reset
7	VRRTC_DISABLE	0: Functional mode 1: VRRTC LDO is in off mode when it should be in active mode. Protected with KEY_TST.	RW	0
6	VRRTC_SLEEP	0: VRRTC LDO in normal functional mode 1: VRRTC LDO in sleep mode for less power consumption	RW	0

Bits	Field Name	Description	Type	Reset
5	VRRTC_TRIEN	0: Functional mode 1: Regulator output is high-impedance. Protected with KEY_TST. Protected with KEY_TST.	RW	0
4:3	VRRTC_TRIM	2 trim bits. Protected with KEY_TST.	RW	0x1
2	LOJIT1_LOWV	Protected with KEY_TST If it is used in functional mode, the user must lock back the KEY_TST immediately after register write.	RW	1
1	LOJIT0_LOWV	If LOJIT0 and LOJT1 are low, the 32-kHz oscillator is in high-jitter mode. In all other cases, the 32-kHz oscillator is in low-jitter mode. Protected with KEY_TST If it is used in functional mode, the user must lock back the KEY_TST immediately after register write.	RW	1
0	BYP_32KHZ_LOWV	Protected with KEY_TST This bit reset value is 1 in slave and test modes.	RW	0

Table 3-15. WATCHDOG_CFG

Address Offset	0x03−0x03 in 0x17 byte increments		
Physical Address	0x0000 005E−0x0000 005E	**Instance**	POWERPM_RECEIVER
Description	Watchdog configuration register (VRRTC domain) This watchdog can stop or restart the system when there is a software or hardware issue. The counter is set to a value (1 to 30 seconds) and if the software does not write back a value on the counter or disable the counter (by writing 0 on the watchdog), the system is reset after the specified delay. If the STARTON_SWBUG bit of the CFG_P1_TRANSITION or CFG_P2_TRANSITION or CFG_P3_TRANSITION register is set to 1, the system restarts automatically.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved				WATCHDOG			

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:0	WATCHDOG	00000: Watchdog disabled 00001: Triton goes to WAIT-ON state. 00010: Triton goes to WAIT-ON state in 1 second. 00011: Triton goes to WAIT-ON state in 2 seconds. 00100: Triton goes to WAIT-ON state in 3 seconds. When 11110: Triton goes in WAIT-ON state in 29 seconds. When 11111: Triton goes in WAIT-ON state in 30 seconds. This register is updated every second: Watchdog <= Watchdog – 1 every second. Reset when signal triton_reset_na is low (WAIT-ON state).	RW	0x00

Table 3-16. DC/DC_GLOBAL_CFG

Address Offset	0x06−0x06 in 0x17 byte increments		
Physical Address	0x0000 0061−0x0000 0061	**Instance**	POWERPM_RECEIVER
Description	DC/DC voltage regulator configuration register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
CARD_DETECT_2_LEVEL	CARD_DETECT_1_LEVEL	REGEN_PU_DISABLE	SYSEN_PU_DISABLE	SMARTREFLEX_ENABLE	CARD_DETECT_CFG	CLK_32K_DEGATE	CLK_HF_DEGATE

Bits	Field Name	Description	Type	Reset
7	CARD_DETECT_2_LEVEL	0: CD2 is active high. Card presence detected at high level. 1: CD2 is active low. Card presence detected at low level.	RW	0
6	CARD_DETECT_1_LEVEL	0: CD1 is active high. Card presence detected at high level. 1: CD1 is active low. Card presence detected at low level.	RW	0
5	REGEN_PU_DISABLE	0: REGEN pullup enabled when the open-drain is not driven 1: REGEN pullup never enabled	RW	0
4	SYSEN_PU_DISABLE	0: SYSTEN pullup enabled when the open-drain is not driven 1: SYSEN pullup not enabled	RW	0
3	SMARTREFLEX_ENABLE	0: SmartReflex is disabled. 1: SmartReflex is enabled. By default, pads used by SmartReflex and Vmode are assigned to Vmode. They are assigned to the SmartReflex I2S bus only when SMARTREFLEX_ ENABLE is high.	RW	0
2	CARD_DETECT_CFG	0: The SIM card is plugged in on GPIO1/INT1 (CD2). 1: The MMC2 card is plugged in on GPIO1/INT1 (CD2).	RW	0
1	CLK_32K_DEGATE	0: clk32kout gating is controlled by the PMC STM (default). 1: clk32kout gating is disabled. Write access to these bits only in secure mode (MSECURE pad = 1) These bits are sync reset to 0 when NRESPWRON is driven low (usual PMC_RESET async reset).	RW	0
0	CLK_HF_DEGATE	0: clkhfout gating is controlled by the PMC STM (default). Clken is controlled by the PMC STM. 1: clkhfout gating is disabled. Clken is tied to 1. Write access to these bits only in secure mode (MSECURE pad = 1) These bits are sync reset to 0 when NRESPWRON is driven low (usual PMC_RESET async reset).	RW	0

Table 3-17. MISC_CFG

Address Offset	0x0D−0x0D in 0x17 byte increments		
Physical Address	0x0000 0068−0x0000 0068	**Instance**	POWERPM_RECEIVER
Description	VRRTC domain		
Type	RW		

7	6	5	4	3	2	1	0
TEMP_SEL		VINTANA2_SWITCH_AUTO	CLK_HF_DRV	RFID_EN_PU_DISABLE	RFID_EN	CLKEN2_CFG	CLKEN2_ENABLE

Bits	Field Name	Description	Type	Reset
7:6	TEMP_SEL	Hot-die interrupt temperature selection	RW	0x0
5	VINTANA2_SWITCH_AUTO	0: The switch from 2.75 V to 2.5 V, if battery voltage is below 3.0 V, is manual. 1: Automatic switch enabled	RW	0
4	CLK_HF_DRV	This bit selects the output drive of the HFCLKOUT pin. 0: Output drive for a 10-pF capacity load 1: Output drive for a 40-pF capacity load	RW	1
3	RFID_EN_PU_DISABLE	0: RFID_EN pullup enabled when the open-drain is not driven 1: RFID_EN pullup never enabled (Was CLK_32K_DRV; no longer used)	RW	0
2	RFID_EN	0: RFID_EN pad is set to 0. 1: RFID_EN pad is set to 1.	RW	0
1	CLKEN2_CFG	0: The CLKEN clock enable is output on CLKEN2. 1: CLKEN2 pad is a GPIO.	RW	1
0	CLKEN2_ENABLE	If CLKEN2_CFG = 1: 0: CLKEN2 = 0 1: CLKEN2 = 1 If CLKEN2_CFG = 0: No action	RW	0

Table 3-18. VIO_OSC

Address Offset	0x52−0x52 in 0x26 byte increments		
Physical Address	0x0000 00AD−0x0000 00AD	**Instance**	POWERPM_RECEIVER
Description	VRRTC domain		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			OVLAP_SEL			SH_RAMP_SWITCH	

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0
4:2	OVLAP_SEL	If expected OSC OVLAP_SEL is 000, reg value must be 110. If expected OSC OVLAP_SEL is 001, reg value must be 111. If expected OSC OVLAP_SEL is 010, reg value must be 100. If expected OSC OVLAP_SEL is 011, reg value must be 101. If expected OSC OVLAP_SEL is 100, reg value must be 010. If expected OSC OVLAP_SEL is 101, reg value must be 011. If expected OSC OVLAP_SEL is 110, reg value must be 000. If expected OSC OVLAP_SEL is 111, reg value must be 001.	RW	0x0
1:0	SH_RAMP_SWITCH		RW	0x0

Table 3-19. VDD1_OSC

Address Offset	0x5C−0x5C in 0x26 byte increments		
Physical Address	0x0000 00B7−0x0000 00B7	**Instance**	POWERPM_RECEIVER
Description			
Type	RW		

7	6	5	4	3	2	1	0
Reserved		CKIN_EN	OVLAP_SEL			SH_RAMP_SWITCH	

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0
5	CKIN_EN	If expected OSC OVLAP_SEL is 000, reg value must be 110. If expected OSC OVLAP_SEL is 001, reg value must be 111. If expected OSC OVLAP_SEL is 010, reg value must be 100. If expected OSC OVLAP_SEL is 011, reg value must be 101. If expected OSC OVLAP_SEL is 100, reg value must be 010. If expected OSC OVLAP_SEL is 101, reg value must be 011. If expected OSC OVLAP_SEL is 110, reg value must be 000. If expected OSC OVLAP_SEL is 111, reg value must be 001.	RW	0
42	OVLAP_SEL		RW	0x0
1:0	SH_RAMP_ SWITCH		RW	0x0

Table 3-20. VDD2_OSC

Address Offset	0x6A−0x6A in 0x26 byte increments		
Physical Address	0x0000 00C5−0x0000 00C5	**Instance**	POWERPM_RECEIVER
Description			
Type	RW		

7	6	5	4	3	2	1	0
Reserved		CKIN_EN	OVLAP_SEL			SH_RAMP_SWITCH	

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0
5	CKIN_EN	If expected OSC OVLAP_SEL is 000, reg value must be 110. If expected OSC OVLAP_SEL is 001, reg value must be 111. If expected OSC OVLAP_SEL is 010, reg value must be 100. If expected OSC OVLAP_SEL is 011, reg value must be 101. If expected OSC OVLAP_SEL is 100, reg value must be 010. If expected OSC OVLAP_SEL is 101, reg value must be 011. If expected OSC OVLAP_SEL is 110, reg value must be 000. If expected OSC OVLAP_SEL is 111, reg value must be 001.	RW	0
4:2	OVLAP_SEL		RW	0x0
1:0	SH_RAMP_ SWITCH		RW	0x0

3.6.2 RTC

This section provides information about the RTC module instance in the device and describes the individual registers.

The RTC module has multiple modes. Table 3-21 lists the register accesses for the modes.

Table 3-22 summarizes the RTC modes.

Table 3-23 and Table 3-24 summarize the RTC registers for secure mode and unsecure mode, respectively.

Table 3-25 through Table 3-43 describe the individual registers.

Table 3-21. RTC Mode Overview

Address Offset	Registers			
	Secure		Unsecure	
	READ	WRITE	READ	WRITE
0x00	SECONDS_REG	–	SECONDS_REG	SECONDS_REG
0x01	MINUTES_REG	–	MINUTES_REG	MINUTES_REG
0x02	HOURS_REG	–	HOURS_REG	HOURS_REG

Table 3-21. RTC Mode Overview (continued)

Address Offset	Registers			
	Secure		Unsecure	
	READ	WRITE	READ	WRITE
0x03	DAYS_REG	–	DAYS_REG	DAYS_REG
0x04	MONTHS_REG	–	MONTHS_REG	MONTHS_REG
0x05	YEARS_REG	–	YEARS_REG	YEARS_REG
0x06	WEEKS_REG	–	WEEKS_REG	WEEKS_REG
0x07	ALARM_SECONDS_ REG	ALARM_SECONDS_ REG	ALARM_SECONDS_ REG	ALARM_SECONDS_ REG
0x08	ALARM_MINUTES_ REG	ALARM_MINUTES_ REG	ALARM_MINUTES_ REG	ALARM_MINUTES_ REG
0x09	ALARM_HOURS_ REG	ALARM_HOURS_ REG	ALARM_HOURS_ REG	ALARM_HOURS_ REG
0x0A	ALARM_DAYS_REG	ALARM_DAYS_REG	ALARM_DAYS_REG	ALARM_DAYS_REG
0x0B	ALARM_MONTHS_ REG	ALARM_MONTHS_ REG	ALARM_MONTHS_ REG	ALARM_MONTHS_ REG
0x0C	ALARM_YEARS_REG	ALARM_YEARS_REG	ALARM_YEARS_REG	ALARM_YEARS_REG
0x0D	RTC_CTRL_REG		RTC_CTRL_REG	RTC_CTRL_REG
0x0E	RTC_STATUS_REG	RTC_STATUS_REG	RTC_STATUS_REG	RTC_STATUS_REG
0x0F	RTC_INTERRUPTS_ REG	RTC_INTERRUPTS_ REG	RTC_INTERRUPTS_ REG	RTC_INTERRUPTS_ REG
0x10	RTC_COMP_LSB_ REG	–	RTC_COMP_LSB_ REG	RTC_COMP_LSB_ REG
0x11	RTC_COMP_MSB_ REG	–	RTC_COMP_MSB_ REG	RTC_COMP_MSB_ REG

Table 3-22. RTC Mode Summary

Mode Name	Condition
SECURE	P(MSecure)=0
UNSECURE	P(MSecure)=1

3.6.2.1 Condition: P(MSecure) = 0

Table 3-23. RTC Register Summary for SECURE Mode

Register Name	Type	Register Width (Bits)	Physical Address
SECONDS_REG	R	8	0x0000 001C
MINUTES_REG	R	8	0x0000 001D
HOURS_REG	R	8	0x0000 001E
DAYS_REG	R	8	0x0000 001F
MONTHS_REG	R	8	0x0000 0020
YEARS_REG	R	8	0x0000 0021
WEEKS_REG	R	8	0x0000 0022
ALARM_SECONDS_REG	RW	8	0x0000 0023
ALARM_MINUTES_REG	RW	8	0x0000 0024
ALARM_HOURS_REG	RW	8	0x0000 0025
ALARM_DAYS_REG	RW	8	0x0000 0026
ALARM_MONTHS_REG	RW	8	0x0000 0027
ALARM_YEARS_REG	RW	8	0x0000 0028
RTC_CTRL_REG	R	8	0x0000 0029
RTC_STATUS_REG	RW	8	0x0000 002A
RTC_INTERRUPTS_REG	RW	8	0x0000 002B
RTC_COMP_LSB_REG	R	8	0x0000 002C
RTC_COMP_MSB_REG	R	8	0x0000 002D

3.6.2.2 Condition: P(MSecure) = 1

Table 3-24. RTC Register Summary for UNSECURE Mode

Register Name	Type	Register Width (Bits)	Physical Address
SECONDS_REG	RW	8	0x0000 001C
MINUTES_REG	RW	8	0x0000 001D
HOURS_REG	RW	8	0x0000 001E
DAYS_REG	RW	8	0x0000 001F
MONTHS_REG	RW	8	0x0000 0020
YEARS_REG	RW	8	0x0000 0021
WEEKS_REG	RW	8	0x0000 0022
ALARM_SECONDS_REG	RW	8	0x0000 0023
ALARM_MINUTES_REG	RW	8	0x0000 0024
ALARM_HOURS_REG	RW	8	0x0000 0025
ALARM_DAYS_REG	RW	8	0x0000 0026
ALARM_MONTHS_REG	RW	8	0x0000 0027
ALARM_YEARS_REG	RW	8	0x0000 0028
RTC_CTRL_REG	RW	8	0x0000 0029
RTC_STATUS_REG	RW	8	0x0000 002A
RTC_INTERRUPTS_REG	RW	8	0x0000 002B
RTC_COMP_LSB_REG	RW	8	0x0000 002C
RTC_COMP_MSB_REG	RW	8	0x0000 002D

Table 3-25. SECONDS_REG

Address Offset	0x00		
Physical Address	0x0000 001C	**Instance**	POWERRTC
Description			
Type	See Table 3-21.		

7	6	5	4	3	22	1	0
Reserved	SEC1			SEC0			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:4	SEC1	Second digit of seconds. Range is 0 to 5.	RW	0x0
3:0	SEC0	First digit of seconds. Range is 0 to 9.	RW	0x0

Table 3-26. MINUTES_REG

Address Offset	0x01		
Physical Address	0x0000 001D	**Instance**	POWERRTC
Description			
Type	See Table 3-21.		

7	6	5	4	3	2	1	0
Reserved	MIN1			MIN0			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:4	MIN1	Second digit of minutes. Range is 0 to 5.	RW	0x0
3:0	MIN0	First digit of minutes. Range is 0 to 9.	RW	0x0

Table 3-27. HOURS_REG

Address Offset	0x02		
Physical Address	0x0000 001E	**Instance**	POWERRTC
Description			
Type	See Table 3-21.		

7	6	5	4	3	2	1	0
PM_NAM	Reserved	HOUR1		HOUR0			

Bits	Field Name	Description	Type	Reset
7	PM_NAM	Used only in PM_AM mode (otherwise, 0) 0: AM 1: PM	RW	0
6	Reserved		R	0
5:4	HOUR1	Second digit of hours. Range is 0 to 2.	RW	0x0
3:0	HOUR0	First digit of hours. Range is 0 to 9.	RW	0x0

Table 3-28. DAYS_REG

Address Offset	0x03		
Physical Address	0x0000 001F	**Instance**	POWERRTC
Description			
Type	See Table 3-21.		

7	6	5	4	3	2	1	0
Reserved		DAY1		DAY0			

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:4	DAY1	Second digit of days. Range is 0 to 3.	RW	0x0
3:0	DAY0	First digit of days. Range is 0 to 9.	RW	0x1

Table 3-29. MONTHS_REG

Address Offset	0x04		
Physical Address	0x0000 0020	**Instance**	POWERRTC
Description	Usual notation is taken for month value: 01: January 02: February .... 12: December		
Type	See Table 3-21.		

7	6	5	4	3	2	1	0
Reserved			MONTH1	MONTH0			

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4	MONTH1	Second digit of months. Range is 0 to 1.	RW	0
3:0	MONTH0	First digit of months. Range is 0 to 9.	RW	0x1

Table 3-30. YEARS_REG

Address Offset	0x05		
Physical Address	0x0000 0021	**Instance**	POWERRTC
Description			
Type	See Table 3-21.		

7	6	5	4	3	2	1	0
YEAR1				YEAR0			

Bits	Field Name	Description	Type	Reset
7:4	YEAR1	Second digit of years. Range is 0 to 9.	RW	0x0
3:0	YEAR0	First digit of years. Range is 0 to 9.	RW	0x0

Table 3-31. WEEKS_REG

Address Offset	0x06		
Physical Address	0x0000 0022	**Instance**	POWERRTC
Description			
Type	See Table 3-21.		

7	6	5	4	3	2	1	0
Reserved						WEEK	

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RW	0x00
2:0	WEEK	First digit of days in a week. Range is 0 to 6.	RW	0x0

Table 3-32. ALARM_SECONDS_REG

Address Offset	0x07		
Physical Address	0x0000 0023	**Instance**	POWERRTC
Description			
Type	RW		

7	6	5	4	3	2	1	0
Reserved	ALARM_SEC1			ALARM_SEC0			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:4	ALARM_SEC1	Second digit of seconds. Range is 0 to 5.	RW	0x0
3:0	ALARM_SEC0	First digit of seconds. Range is 0 to 9.	RW	0x0

Table 3-33. ALARM_MINUTES_REG

Address Offset	0x08		
Physical Address	0x0000 0024	**Instance**	POWERRTC
Description			
Type	RW		

7	6	5	4	3	2	1	0
Reserved	ALARM_MIN1			ALARM_MIN0			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:4	ALARM_MIN1	Second digit of minutes. Range is 0 to 5.	RW	0x0
3:0	ALARM_MIN0	First digit of minutes. Range is 0 to 9.	RW	0x0

Table 3-34. ALARM_HOURS_REG

Address Offset	0x09		
Physical Address	0x0000 0025	**Instance**	POWERRTC
Description			
Type	RW		

7	6	5	4	3	2	1	0
ALARM_PM_NAM	Reserved	ALARM_HOUR1		ALARM_HOUR0			

Bits	Field Name	Description	Type	Reset
7	ALARM_PM_NAM	Used only in PM_AM mode (otherwise, 0) 0: AM 1: PM	RW	0
6	Reserved		R	0
5:4	ALARM_HOUR1	Second digit of hours. Range is 0 to 2.	RW	0x0
3:0	ALARM_HOUR0	First digit of hours. Range is 0 to 9.	RW	0x0

Table 3-35. ALARM_DAYS_REG

Address Offset	0x0A		
Physical Address	0x0000 0026	**Instance**	POWERRTC
Description			
Type	RW		

7	6	5	4	3	2	1	0
Reserved		ALARM_DAY1		ALARM_DAY0			

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:4	ALARM_DAY1	Second digit of days. Range is 0 to 3.	RW	0x0
3:0	ALARM_DAY0	First digit of days. Range is 0 to 9.	RW	0x1

Table 3-36. ALARM_MONTHS_REG

Address Offset	0x0B		
Physical Address	0x0000 0027	**Instance**	POWERRTC
Description			
Type	RW		

7	6	5	4	3	2	1	0
Reserved			ALARM_MONTH1	ALARM_MONTH0			

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4	ALARM_MONTH1	Second digit of months. Range is 0 to 1.	RW	0
3:0	ALARM_MONTH0	First digit of months. Range is 0 to 9.	RW	0x1

Table 3-37. ALARM_YEARS_REG

Address Offset	0x0C		
Physical Address	0x0000 0028	**Instance**	POWERRTC
Description			
Type	RW		

7	6	5	4	3	2	1	0
ALARM_YEAR1				ALARM_YEAR0			

Bits	Field Name	Description	Type	Reset
7:4	ALARM_YEAR1	Second digit of years. Range is 0 to 9.	RW	0x0
3:0	ALARM_YEAR0	First digit of years. Range is 0 to 9.	RW	0x0

Table 3-38. RTC_CTRL_REG

Address Offset	0x0D		
Physical Address	0x0000 0029	**Instance**	POWERRTC
Description	SET_32_counter must be used only when the RTC is frozen. The ROUND_30S bit is a toggle bit; the host processor can only write 1, and the RTC clears it. If the host processor sets the ROUND_30S bit and then reads it, the host processor reads 1 until rounding to the closest minute is performed at the next second. MODE_12_24: It is possible to switch between the two modes at any time without disturbing the RTC; read or write is always performed with the current mode. The GET_TIME bit is a toggle bit; the host processor can only write 1, and the RTC clears it. If the host processor sets the GET_TIME bit and then reads it, the host processor reads 0 (backup domain).		
Type	See Table 3-21.		

7	6	5	4	3	2	1	0
Reserved	GET_TIME	SET_32_COUNTER	TEST_MODE	MODE_12_24	AUTO_COMP	ROUND_30S	STOP_RTC

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	GET_TIME	0: No action 1: When 1 is written, internal TC register values are stored in latches. When the ALARM_SECONDS_REG, ALARM_MINUTES_REG, ... registers are read, these latched values are read. (For more information, see the Description of this register.)	RW	0
5	SET_32_COUNTER	0: No action 1: Set the 32-kHz counter with comp_reg value. (For more information, see the Description of this register.)	R	0x0
4	TEST_MODE	0: Functional mode 1: Test mode (Autocompensation is enabled when the 32-kHz counter reaches its end.)	R	0x0
3	MODE_12_24	0: 24-hour mode (For more information, see the Description of this register.) 1: 12-hour mode (PM/AM mode)	R	0x0
2	AUTO_COMP	0: No autocompensation 1: Autocompensation enabled	R	0x0
1	ROUND_30S	0: No update 1: When 1 is written, the time is rounded to the closest minute. (For more information, see the Description of this register.)	R	0x0
0	STOP_RTC	0: RTC is frozen. 1: RTC is running.	R	0x0

Table 3-39. RTC_STATUS_REG

Address Offset	0x0E		
Physical Address	0x0000 002A	**Instance**	POWERRTC
Description	The alarm interrupt is low until the host processor writes 1 in the ALARM bit of the RTC_STATUS_REG register. POWER_UP is set by a reset and is cleared by writing 1 in this bit (backup domain).		
Type	RW		

7	6	5	4	3	2	1	0
POWER_UP	ALARM	1D_EVENT	1H_EVENT	1M_EVENT	1S_EVENT	RUN	Reserved

Bits	Field Name	Description	Type	Reset
7	POWER_UP	A reset occurred.	RW	1
6	ALARM	An alarm interrupt was generated.	RW	0
5	1D_EVENT	One day occurred.	R	0
4	1H_EVENT	One hour occurred.	R	0
3	1M_EVENT	One minute occurred.	R	0
2	1S_EVENT	One second occurred.	R	0
1	RUN	0: RTC is frozen. 1: RTC is running.	R	0
0	Reserved		R	0

Table 3-40. RTC_INTERRUPTS_REG

Address Offset	0x0F		
Physical Address	0x0000 002B	**Instance**	POWERRTC
Description			
Type	RW		

7	6	5	4	3	2	1	0
Reserved				IT_ALARM	IT_TIMER	EVERY	

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RW	0x0
3	IT_ALARM	Enable one interrupt when the alarm value is reached (TC ALARM registers) by the TC registers.	RW	0
2	IT_TIMER	Enable periodic interrupt. 0: Interrupt disabled 1: Interrupt enabled	RW	0
1:0	EVERY	Interrupt period 0: Every second 1: Every minute 2: Every hour 3: Every day	RW	0x0

Table 3-41. RTC_COMP_LSB_REG

Address Offset	0x10		
Physical Address	0x0000 002C	**Instance**	POWERRTC
Description	This register must be written in twos complement. This means that to add one 32-kHz oscillator period every hour, the host processor must write FFFF into RTC_COMP_MSB_REG and RTC_COMP_LSB_REG. To remove one 32-kHz oscillator period every hour, the host processor must write 0001 into RTC_COMP_MSB_REG and RTC_COMP_LSB_REG. The 7FFF value is forbidden.		
Type	See Table 3-21.		

7	6	5	4	3	2	1	0
RTC_COMP_LSB							

Bits	Field Name	Description	Type	Reset
7:0	RTC_COMP_LSB	Number of 32-kHz periods to be added to the 32-kHz counter every hour	RW	0x00

Table 3-42. RTC_COMP_MSB_REG

Address Offset	0x11		
Physical Address	0x0000 002D	**Instance**	POWERRTC
Description			
Type	See Table 3-21.		

7	6	5	4	3	2	1	0
RTC_COMP_MSB							

Bits	Field Name	Description	Type	Reset
7:0	RTC_COMP_MSB	Number of 32-kHz periods to be added into the 32-kHz counter every hour	RW	0x00

Table 3-43. CLD_TRIM_RAMP

Address Offset	0x06		
Physical Address	0x0000 0052	**Instance**	AUDIO_SCTEST
Description	Class D: Ramp trimming control register. There is a correlation between CLD_RAMP_FREQ and CLD_RAMP_TRIM. Ex: Clock frequency = 400 kHz → Res_ramp = 15K, I_ramp_unit = 9.7 μA Clock frequency = 320 kHz → Res_ramp = 16.875K, I_ramp_unit = 8.9 μA Clock frequency = 600 kHz → Res_ramp = 9.375K, I_ramp_unit = 13.3 μA		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	CLD_RAMP_FREQ			CLD_RAMP_TRIM			

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6:4	CLD_RAMP_FREQ	Trim bits used in the ramp generator to trim the amplitude of the ramp (which must be related to the frequency) The amplitude is defined by Res_ramp and I_ramp_unit: 0x0: Res_ramp = 15 kΩ (Freq = 400 kHz) 0x1: Res_ramp = 11.25 kΩ 0×2: Res_ramp = 11.25 kΩ 0x3: Res_ramp = 7.5 kΩ 0x4: Res_ramp = 16.875 kΩ (320 kHz) 0x5: Res_ramp = 13.125 kΩ 0x6: Res_ramp = 13.125 kΩ 0x7: Res_ramp = 9.375 kΩ (600 kHz)	RW	0x0
3:0	CLD_RAMP_TRIM	Trim bits used in the ramp generator to control the current (thermometer code) 0x0: I_ramp_unit = 8.9 μA 0x1: I_ramp_unit = 9.7 μA 0x3: I_ramp_unit = 10.6 μA 0x7: I_ramp_unit = 11.8 μA 0xF: I_ramp_unit = 13.3 μA	RW	0x3

Interrupts

This chapter describes the interrupts used in the integrated power-management/audio coder/decoder (codec) device.

Topic **Page**

4.1 Interrupt Handler Overview

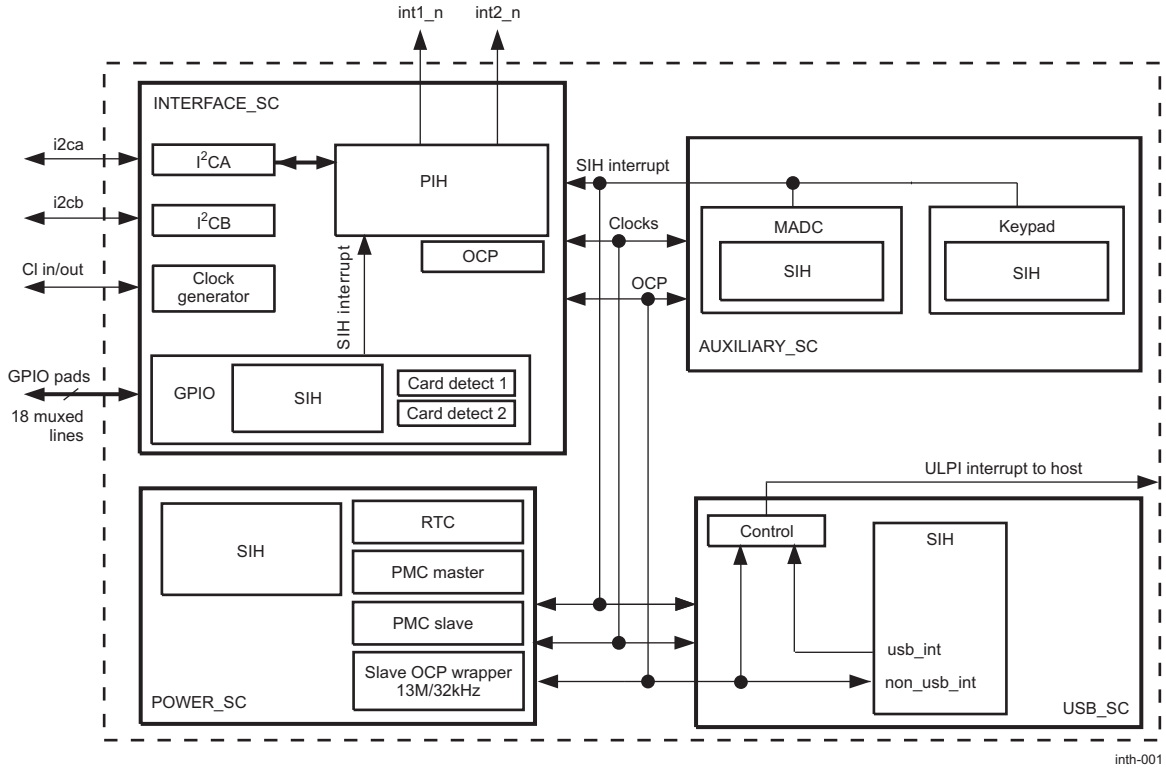
The device power integrated circuit (IC) integrates five modules (also called subchips):

- INTERFACE_SC
- AUDIO_SC (TPS65930 only)
- AUXILIARY_SC
- USB_SC
- POWER_SC

The INTERFACE_SC interfaces with the other subchips. Each subchip except the AUDIO_SC has at least one interrupt handler, the secondary interrupt handler (SIH), that communicates with the primary interrupt handler (PIH) in the INTERFACE_SC. The AUXILIARY_SC includes two SIHs (for monitoring analog-to-digital control [MADC]) and a keypad. The USB_SC includes the UTIM+ low pin interface (ULPI) port, in addition to the SIH, for interrupts. If the ULPI port is selected for interrupts, the ULPI data bus is a direct interrupt line to the host.

Figure 4-1 is a top-level block diagram of the interrupt handler blocks.

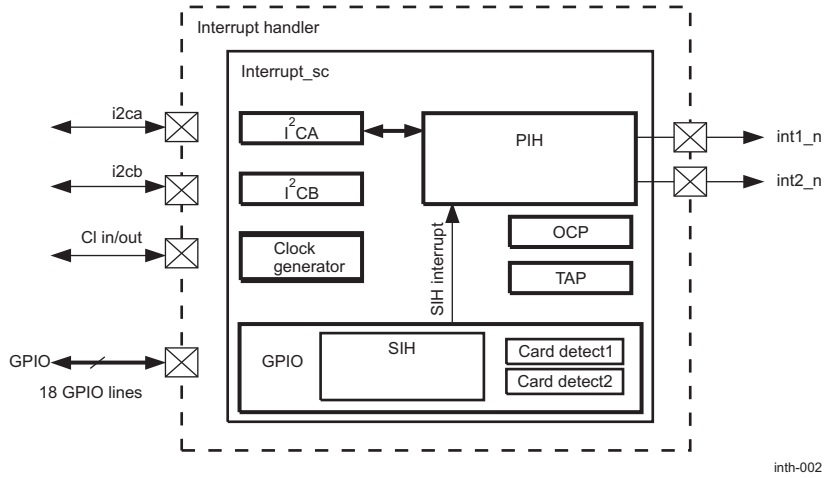
Figure 4-1. Device Subchip Block Diagram



4.2 Interrupt Handler Environment

Figure 4-2 shows the interrupt handler connections to external devices.

Figure 4-2. Interrupts To and From External Devices



An output pin (int1_n) is available to send an interrupt to an external host. All device interrupt sources can be directed to interrupt line 1 (INT1). Each interrupt source can be redirected to interrupt pins int1_n. The selection is made through an interrupt mask register (IMR).

Because the silicon carries over the design of the TPS65950, which has access to two interrupt status lines, the PIH consists of two configuration registers:

- PIH_ISR_P1: Interrupt status register for INT1
- PIH_ISR_P2: Interrupt status register for INT2 (not available)

NOTE: Because only INT1 is available to the TPS65930 and TPS65920, it must be selected for all applications.

These registers store the SIH block generating the current interrupt, and tell the host which subsystem ISR (SIH_ISR) to read for interrupt details.

The SIH consists of four configuration registers:

- ISR (ISR1 and ISR2): Interrupt status register. Indicates which input event triggered the interrupt request
- IMR (IMR1 and IMR2): Interrupt mask register: Allows masking of the expected transition event from generating an interrupt request on INT1 and INT2. Input events that can trigger interrupts are described in Section 4.6, *Register Manual*, for each SIH block.
- EDR (EDR1 and EDR2): Edge-detection register: Enable or disable falling-edge or rising-edge detection. Section 4.6, *Register Manual*, shows the fields and values used for edge detection.
- SIH_CTRL: SIH control register: Enable or disable features like pending interrupts, exclusivity, and clear-on-read (COR). These features are explained in Section 4.4.1, *Interrupt Processing*, and Section 4.4.2, *Register Read Write Features*.

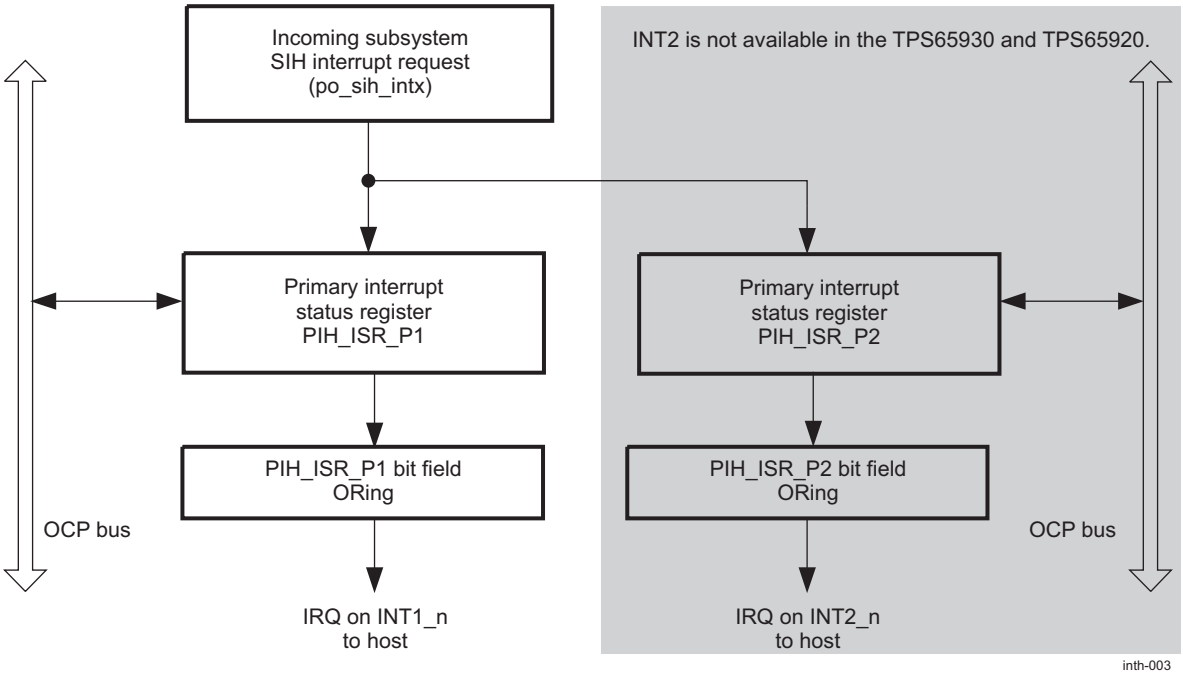
4.3 Interrupt Handler Integration

This section describes interrupt handlers in the device. Each module in the device, except the AUDIO_SC module (TPS65930 only), has an SIH that communicates with the PIH. The function of each SIH is the same in each subchip and is explained once.

4.3.1 PIH and SIH Block Diagram

Figure 4-3 and Figure 4-4 are block diagrams of the PIH and the SIH, respectively.

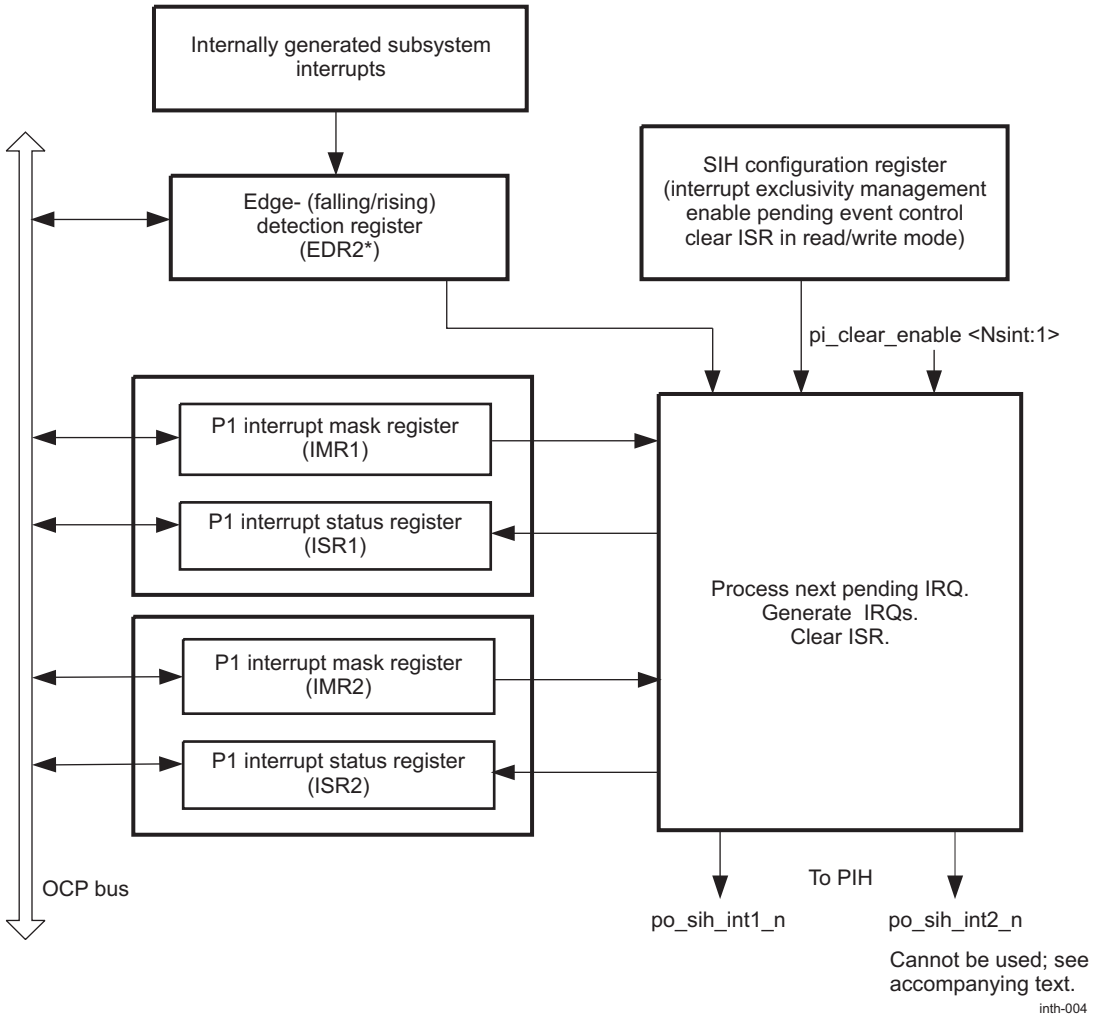
Figure 4-3. PIH Block Diagram



The PIH receives interrupts from the SIH of the other subchips. There can be six external interrupt request sources to the INTERFACE_SC subchip. The PIH has two interrupt status registers (PIH_ISR_P1 and PIH_ISR_P2) and if both were available, they would tell an external host processor which subchip to read for the SIH_ISR register values. Because the TPS65930 and TPS65920 offer access only to INT1, only PIH_ISR_P1 is used.

If a status register field of the PIH is set, an active low interrupt is generated and sent to the host.

Figure 4-4. SIH Block Diagram



There are two identical interrupt-generation modules in the SIH. Each interrupt-generation module processes synchronous interrupt requests from the general-purpose input/output (GPIO), MADC, keypad, power, and universal serial bus (USB) modules. Each interrupt-generation module controls its own synchronous interrupt request line and its own interrupt mask register (IMRx) and interrupt status register (ISRx).

NOTE: Because INT2 is not available in the TPS65930 and TPS65920, it cannot be used. Its description is included to explain why registers are available to control INT2 (the design comes from the TPS65950 and in that device, INT2 is available. For all applications using the TPS65930 and TPS65920, INT1 must be selected.

4.3.2 Interrupt Requests

The device can handle six interrupts in the PIH coming from the GPIO, USB, MADC, keypad, and power (PWR) modules, and several in the SIH. Table 4-1 lists the SIH interrupts for the device. Depending on the mask bits, these interrupts can generate an external interrupt signal on INT1 and/or INT2 outputs (when using the TPS65930 and TPS65920, always select INT1).

Table 4-1. Device External Interrupt Sources

PIH	SIH
Power management	RTC alarm event
	RTC periodic event
	VBUS D+/D– detection
	Hot-die condition detection
	Power on (PWRON) detection
	PWROK time-out DCDC1
	PWROK time-out DCDC2
	VINTANA2 short-circuit detect
	VMMC1 short-circuit detect
	VAUX2 short-circuit detect
	VIO short-circuit detect
	VDD2 short-circuit detect
	VDD1 short-circuit detect
MADC	MADC end of conversion (start analog-to-digital converter [ADC])
	MADC end of conversion (software processor 1 [SW1])
	MADC end of conversion (software processor 2 [SW2])
	MADC USB (VBAT to VUSB supply change)
GPIOs	GPIO[0…17] interrupts
Keypad	Keypad time-out
	Key pressed
	Long key pressed
USB	DISCONNECTED
	CARKIT
	USB_OTG_B
	USB_HOST
	PH_ACC
	PSM_ERROR
	PH_NO_ACK
	PHONE_UART
	CARDP
	STOP_PLS_MISS
	IDGND
	SESSEND
	SESSVALID
	VBUSVALID
	HOSTDISCONNECT
	CARINTDET
	ULPI_I2C_CONFLICT_ERROR
	VB_SESS_VLD
	DM_HI
	DP_HI
	ABNORMAL_STRESS
	ID_FLOAT
	ID_RES_440K
	ID_RES_200K
	ID_RES_100K

When configured as inputs, GPIOs can generate interrupts that can be directed to the INT1 and/or INT2 signals, depending on the register configuration (GPIO_SIH_IMRx). With the TPS65930 and TPS65920, INT1 must always be selected. When an interrupt event is an input to the SIH, there are two ways to clear it:

- Clear on read: The interrupt is cleared when the associated interrupt register is read.
- Clear on write: The interrupt is cleared by writing to the ISR when the <module>_SIH_CTRL[2] COR bit is set to 1.

4.3.3 Clocking and Power Management

The clock source for the PIH and the SIH in the interface subchip is the 3-MHz clock. The clock source for the other SIHs is the functional clock for that module. All subchip interrupt handlers are powered by a digital power domain of 1.5 V.

4.4 Functional Description

This section is an overview of how the interrupt handler is implemented and how outputs are generated. The following description is relevant to the generation of INT1.

The INT1 pin alerts the host processor of any event that occurs on the device. The host processor can then poll the ISR through the general-purpose (GP) inter-integrated circuit (I^2C™) to identify the responsible event. The detected events are configurable with an IMR.

The interrupt handler has the following main features:

- Auto-acknowledgment mechanism through the status register read/clear/release process
- Less wiring density at the digital top level by removing the ACK signal
- One I^2C access required to determine the interrupt subsystem source
- Ability of a pending event (which can arrive during software latency) to generate an interrupt to the host or disable the plug/unplug feature
- SIH interrupt exclusivity management between the two host processors

The interrupt handler has the following limitations:

- No wake-up interrupts from subsystem modules in OFF state that can turn the device to ACTIVE state
- No interrupt masking from the PIH
- An interrupt generated by the SIH/PIH mechanism must be used by a host with low-level sensitive interrupt detection capability.
- No priority management of interrupts

An interrupt is generated (active low) when a bit field of the PIH status register(s) is set.

4.4.1 Interrupt Processing

4.4.1.1 Input Selection

The interrupt handler supports edge-sensitive incoming interrupt detection. The SIH asserts an interrupt, maintaining it until software handles it. The interrupt is cleared using the clear-on-write or clear-on-read feature (see Section 4.4.2, *Register Read and Write Features*).

4.4.1.2 Masking

Detection of an incoming interrupt can be enabled or disabled by the IMR register <module>_IMR. The IMR lets the user mask the expected transition at the end of a sequence from generating an interrupt request on the INT1 line.

4.4.1.3 Edge Detection

Each module of the interrupt handler has an edge-detection register (EDR), <module>_EDR. The corresponding bits in this register define the edge expected to trigger an incoming interrupt request. The detection can be performed on the rising edge or falling edge or both edges.

4.4.1.4 Exclusivity Management

When exclusivity is enabled (by default), any nonmasked interrupts are transmitted to the INT1_n line. When this feature is disabled, a nonmasked interrupt is transmitted on both interrupt lines (INT1_n and INT2_n), but only INT1_n should be used with the TPS65930 and TPS65920. Exclusivity can be enabled and disabled by writing 1 or 0 to the <module>_SIH_CTRL[0] EXCLEN bit (for example, the EXCLEN bit in the GPIO_SIH_CTRL register).

NOTE: Because only INT1_n is available in the TPS65930 and TPS65920, exclusivity has no function. It is described so that the user will know why it is a programmable feature (the design comes from the TPS65950, where INT1 and INT2 are available, and exclusivity is functional.

4.4.2 Register Read and Write Features

A SIH status register can be cleared two ways, depending on the state of the configuration register, <module>_SIH_CTR:

- Clear-on-read: The status register is cleared when its content is read by the open-core protocol (OCP) bus.
- Clear-on-write: The status register is not automatically cleared on a read access, but on a status write operation.

4.4.2.1 Clear-On-Read

The status register is cleared when its contents are read by the OCP bus. The COR feature is enabled by programming the <module>_ SIH_CTRL[2]) COR bit to 0. In this mode, the status register is cleared when an OCP read occurs. When the status register is read by OCP, a clearing pulse is generated to clear each bit of the status register.

NOTE: To clear the interrupt using the COR feature, read the PWRON bit twice.

NOTE: When the user presses and releases the PWRON button, a first and a second interrupt, respectively, are sent. If the first interrupt is not clear before the PWRON button is released, the PENDDIS bit is set to 0 by default. Two COR actions must then be performed to clear both interrupts.

4.4.2.2 Clear-On-Write

By default, writing 1 to a bit position in the ISR clears the corresponding status bit, while writing 0 leaves the status bit unaffected. This lets software decide when any ISR active field must be cleared, and which interrupt line can be released. The clear-on-write feature is enabled by programming the COR bit to 1. This mechanism allows locking of the COR feature until the last data register associated with the interrupt event is read. In case of plug/unplug detection (for example, from GPIO,), or an interrupt event not associated with data registers, the COR access can be used and the status register cleared when an OCP read occurs.

4.4.2.3 Software Latency

The <module>_SIH_CTRL register enables or disables buffering for a pending event. The <module>_SIH_CTRL[1] PENDDIS bit disables a pending interrupt if written with 1. If PENDDIS is written with 0, pending event buffering is enabled. When two events occur on one interrupt line before the status register is read, the second event is buffered and treated later. A third event that occurs before status read is lost.

4.4.3 USB Interrupts

The device power-management device mechanism for supporting interrupts from the USB_SC differs from that of other subchips. A brief explanation is given in this section. For details, see Chapter 14, *USB*.

The USB_SC receives two types of interrupts:

- USB interrupts:
  - HOSTDISCONNECT
  - VBUSVALID
  - SESSVALID
  - SESSEND
  - IDGND
- Non-USB interrupts (all other interrupts)

The USB_SC module signals interrupts through two interfaces:

- ULPI port

Interrupts signaled at the ULPI port are directed toward the ULPI parallel bus ULPI_DATA[7:0] or the ULPI_DATA[3] line, depending on the register configuration. In USB serial or carkit mode, the ULPI_DATA[3] port is used. In USB synchronous mode, the ULPI_DATA[7:0] port is used and the interrupt is sent as an RX command.

- INT1 line

  The interrupt USB_SIH_INT1_n on the INT1 port from the SIH is routed to the PIH in the INTERFACE_SC module. PIH interrupts are connected to the host.

The ULPI interface allows communication between the USB physical layer transceiver (PHY) and the OTG/host/peripheral controller (link). If the link is in synchronous mode, an interrupt event causes the PHY to send a RX CMD byte to the link. If the link is not in synchronous mode, an interrupt event causes the PHY to assert the interrupt signal. This interrupt signal is multiplexed on the ULPI_DATA[3] or ULPI_DATA[2] line, according to the selected mode (ULPI or CEA2011 protocol), or signaled on the USB_SIH_INT1 line (ALT_INT_REROUTE = 1). When the link detects that the interrupt signal is asserted, it wakes up the clock (if powered down) and then reads the interrupt latch or interrupt status registers to determine the source of the interrupt.

Three interrupt registers support interrupt generation:

- Interrupt enable (*_INT_EN_*)

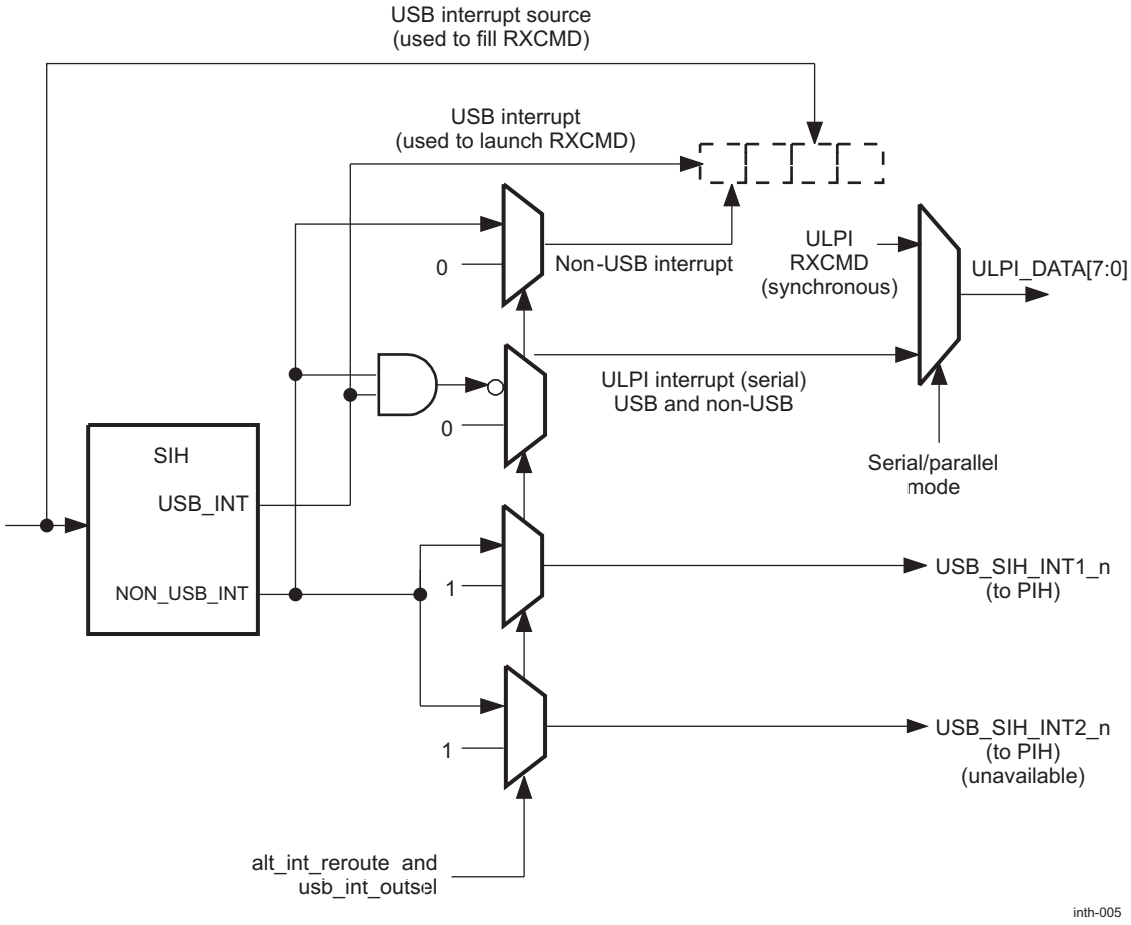
  The interrupt enable register enables the indication of an event when the corresponding signal changes. It acts as a mask event when set low. Depending on the source, interrupts can be enabled on rising (low-to-high transition), falling (high-to-low transition), or when a specified condition is met.
- Interrupt status (*_INT_STS)

  The interrupt status register (read-only) indicates the current value of the interrupt source signal.
- Interrupt latch (*_INT_LATCH)

  The bits in the interrupt latch register are set when a nonmask event occurs on the corresponding signal. This is a read-only register that is cleared automatically on a read access.

Figure 4-5 shows USB interrupt routing.

Figure 4-5. USB Interrupt Routing



4.4.4 Primary Interrupt Handler ISR Mapping

Table 4-2 shows how the bits in PIH_ISR_P1 and PIH_ISR_P2 are mapped to SIH modules in the subchips.

Table 4-2. Register Mapping

	PIH_ISR_P1 and PIH_ISR_P2 Bit Field Mapping							
	ISR7	**ISR6**	**ISR5**	**ISR4**	**ISR3**	**ISR2**	**ISR1**	**ISR0**
T2 subsystems	NA(1)	NA	PWR	USB	MADC	BCI	Keypad	GPIO

(1) NA = not attributed

4.5 Programming Model

4.5.1 Enabling Interrupts

1. Writing 0 to the correct interrupt bit field in the IMR unmasks the interrupt. Two IMRs correspond to INT1 and INT2, the two interrupts for the device. INT2 is not available.
2. Based on the signal transition trigger, the user writes 0 or 1 to the corresponding bit field of the EDR. Writing 1 to the bit field enables falling- or rising-edge detection; writing 0 to the bit field disables falling- or rising-edge detection.
3. Writing 0 to the PENDDIS bit in the SIH_CTRL register enables a pending interrupt event, and writing 1 disables a pending interrupt event. Writing 0 to the EXCLEN bit in this register disables exclusivity; writing 1 enables exclusivity. Writing 0 to the COR bit clears the ISR on a read access; writing 1 to this

bit clears the ISR on a write access.

4.5.2 Servicing Interrupts

1. If the field of the ISR is 1, the SIH asserts the subsystem interrupt request line going to the PIH interrupt line and updates the corresponding PIH_ISR_P1 register. The PIH_ISR register stores this information about the interrupt source in its register fields.
2. The status register of the PIH asserts low the output interrupt line INT1 to the host.
3. When the host recognizes the interrupt, it starts the interrupt routine.
4. The host processor reads the PIH_ISR register to determine the interrupt source. This information points to one of the subsystem SIH modules. Reading the PIH_ISR register does not clear the interrupt.
5. The host processor reads the corresponding SIH_ISR register to determine which event caused the interrupt.
6. Based on the setting of the COR bit, the SIH_ISR bits are cleared. If the COR bit is 0, the SIH_ISR bit is cleared on a read access. If it is 1, it is cleared on a write access.
7. SIH releases the IRQ line going to the PIH. PIH releases the interrupt line (INT1 or INT2).

4.5.3 Disabling Interrupts

Writing 1 to the correct interrupt bit field in the IMR masks the interrupt.

4.6 Register Manual

This section summarizes the registers used to configure interrupts.

4.6.1 Instance Summary

Table 4-3 shows the base address and address space for the INT_SC module instances.

Table 4-3. Instance Summary

Module Name	Base Address	Size
PIH	0x0000 0080	4 bytes
INTERRUPTS (BCI)	0x0000 00B9	14 bytes
GPIO	0x0000 0098	46 bytes
KEYPAD	0x0000 00D2	24 bytes
MADC	0x0000 0000	104 bytes
INT (Power)	0x0000 002E	8 bytes
USB	0x0000 0000	256 bytes

4.6.2 PIH

This section provides information about the interrupt registers in the PIH module instance in the device. Table 4-4 is the PIH register summary. The registers in the module instance are described separately in Table 4-5 through Table 4-7.

Table 4-4. PIH Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
PIH_ISR_P1	RW	8	0x0000 0081
PIH_ISR_P2	RW	8	0x0000 0082
PIH_SIR	RW	8	0x0000 0083

Table 4-5. PIH_ISR_P1

Address Offset	0x01		
Physical Address	0x0000 0081	**Instance**	INT_SCPIH
Description	This register stores the currently active block number (in hexadecimal) generating the current interrupt. Reading this register does not clear any bits, but tells the host which subsystem SIH_ISRx register to read.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
PIH_ISR7	PIH_ISR6	PIH_ISR5	PIH_ISR4	PIH_ISR3	PIH_ISR2	PIH_ISR1	PIH_ISR0

Bits	Field Name	Description	Type	Reset
7	PIH_ISR7	Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
6	PIH_ISR6	Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
5	PIH_ISR5	Power-management-dedicated interrupt line status Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
4	PIH_ISR4	USB-dedicated interrupt line status Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
3	PIH_ISR3	MADC-dedicated interrupt line status Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
2	PIH_ISR2	BCI-dedicated interrupt line status Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
1	PIH_ISR1	Keypad-dedicated interrupt line status Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
0	PIH_ISR0	GPIO-dedicated interrupt line status Read 0x0: No interrupt set 0x1: Interrupt set	RW	0

Table 4-6. PIH_ISR_P2

Address Offset	0x02		
Physical Address	0x0000 0082	**Instance**	INT_SCPIH
Description	This register stores the active block number (in hexadecimal) generating the current interrupt. Reading this register does not clear any bits, but tells the host which subsystem SIH_ISRx register to read.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
PIH_ISR7	PIH_ISR6	PIH_ISR5	PIH_ISR4	PIH_ISR3	PIH_ISR2	PIH_ISR1	PIH_ISR0

Bits	Field Name	Description	Type	Reset
7	PIH_ISR7	Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
6	PIH_ISR6	Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
5	PIH_ISR5	Power-management-dedicated interrupt line status Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
4	PIH_ISR4	USB-dedicated interrupt line status Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
3	PIH_ISR3	MADC-dedicated interrupt line status Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
2	PIH_ISR2	BCI-dedicated interrupt line status Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
1	PIH_ISR1	Keypad-dedicated interrupt line status Read 0x0: No interrupt set 0x1: Interrupt set	RW	0
0	PIH_ISR0	GPIO-dedicated interrupt line status Read 0x0: No interrupt set 0x1: Interrupt set	RW	0

Table 4-7. PIH_SIR

Address Offset	0x03		
Physical Address	0x0000 0083	**Instance**	INT_SCPIH
Description	For testing, the PIH software interrupt PIH_SIR register generates an interrupt event on the gpio_int1_n or gpio_int2_n request line by writing 1 to the targeted SIR bit in a specific test mode. External interrupt requests and internal software requests are merged before being sent to the PIH.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	Reserved	PIH6SIR	PIH5SIR	PIH4SIR	PIH3SIR	PIH2SIR	PIH1SIR

Bits	Field Name	Description	Type	Reset
7	Reserved	Read returns 0.	RW	0
6	Reserved	Read returns 0.	RW	0
5	PIH6SIR	PIH interrupt line test 6 0x0: PIH6 software interrupt not set 0x1: PIH6 software interrupt set	RW	0
4	PIH5SIR	PIH interrupt line test 5 0x0: PIH5 software interrupt not set 0x1: PIH5 software interrupt set	RW	0
3	PIH4SIR	PIH interrupt line test 4 0x0: PIH4 software interrupt not set 0x1: PIH4 software interrupt set	RW	0
2	PIH3SIR	PIH interrupt line test 3	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: PIH3 software interrupt not set		
		0x1: PIH3 software interrupt set		
1	PIH2SIR	PIH interrupt line test 2	RW	0
		0x0: PIH2 software interrupt not set		
		0x1: PIH2 software interrupt set		
0	PIH1SIR	PIH interrupt line test 1	RW	0
		0x0: PIH1 software interrupt not set		
		0x1: PIH1 software interrupt set		

4.6.3 GPIO

This section provides information about the interrupts in the GPIO module instance in the device. Table 4-8 is the GPIO register summary. The registers in the module instance are described separately in Table 4-9 through Table 4-26.

Table 4-8. GPIO Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
GPIO_ISR1A	RW	8	0x0000 00B1
GPIO_ISR2A	RW	8	0x0000 00B2
GPIO_ISR3A	RW	8	0x0000 00B3
GPIO_IMR1A	RW	8	0x0000 00B4
GPIO_IMR2A	RW	8	0x0000 00B5
GPIO_IMR3A	RW	8	0x0000 00B6
GPIO_ISR1B	RW	8	0x0000 00B7
GPIO_ISR2B	RW	8	0x0000 00B8
GPIO_ISR3B	RW	8	0x0000 00B9
GPIO_IMR1B	RW	8	0x0000 00BA
GPIO_IMR2B	RW	8	0x0000 00BB
GPIO_IMR3B	RW	8	0x0000 00BC
GPIO_EDR1	RW	8	0x0000 00C0
GPIO_EDR2	RW	8	0x0000 00C1
GPIO_EDR3	RW	8	0x0000 00C2
GPIO_EDR4	RW	8	0x0000 00C3
GPIO_EDR5	RW	8	0x0000 00C4
GPIO_SIH_CTRL	RW	8	0x0000 00C5

Table 4-9. GPIO_ISR1A

Address Offset	0x019		
Physical Address	0x0000 00B1	**Instance**	INT_SCGPIO
Description	The ISR1A register determines which input GPIO[0:7] pin triggered the interrupt line gpio_int1_n request. As this table shows, bit 0 corresponds to po_pad_gpio[0], bit 1 to po_pad_gpio[1], etc. When a bit in this register is set to 1, the corresponding GPIO pin is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR1 register. If the user writes 0 to a bit in this register, the value does not change when in COR mode. The ISR1A register is synchronous with the interface OCP clock. A read of 1 in any bit means that the corresponding interrupt event is active on interrupt request line 1.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7ISR1	GPIO6ISR1	GPIO5ISR1	GPIO4ISR1	GPIO3ISR1	GPIO2ISR1	GPIO1ISR1	GPIO0ISR1

Bits	Field Name	Description		Type	Reset
7	GPIO7ISR1	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
6	GPIO6ISR1	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
5	GPIO5ISR1	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
4	GPIO4ISR1	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
3	GPIO3ISR1	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
2	GPIO2ISR1	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
1	GPIO1ISR1	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
0	GPIO0ISR1	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		

Table 4-10. GPIO_ISR2A

Address Offset	0x01A		
Physical Address	0x0000 00B2	**Instance**	INT_SCGPIO
Description	This ISR2A register determines which input GPIO[8:15] pin triggered the interrupt line gpio_int1_n request. As this table shows, bit 0 corresponds to po_pad_gpio[8], bit 1 to po_pad_gpio[9], etc. When a bit in this register is set to 1, the corresponding GPIO pin is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR2 register. If the user writes 0 to a bit in this register, the value does not change when in COR mode. The ISR2A register is synchronous with the interface OCP clock. A read of 1 in any bit means that the corresponding interrupt event is active on interrupt request line 1.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15ISR2	GPIO14ISR2	GPIO13ISR2	GPIO12ISR2	GPIO11ISR2	GPIO10ISR2	GPIO9ISR2	GPIO8ISR2

Bits	Field Name	Description		Type	Reset
7	GPIO15ISR2	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
6	GPIO14ISR2	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
5	GPIO13ISR2	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
4	GPIO12ISR2	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
3	GPIO11ISR2	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
2	GPIO10ISR2	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
1	GPIO9ISR22	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
0	GPIO8ISR2	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		

Table 4-11. GPIO_ISR3A

Address Offset	0x01B		
Physical Address	0x0000 00B3	**Instance**	INT_SCGPIO
Description	This ISR3A register determines which input GPIO[16:17] pin triggered the interrupt line gpio_int1_n request. As this table shows, bit 0 corresponds to po_pad_gpio[16] and bit 1 to po_pad_gpio[17]. When a bit in this register is set to 1, the corresponding GPIO pin is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR3 register. If the user writes 0 to a bit in this register, the value does not change when in COR mode. The ISR3A register is synchronous with the interface OCP clock. A read of 1 in any bit means that the corresponding interrupt event is active on interrupt request line 1.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17ISR3	GPIO16ISR3

Bits	Field Name	Description		Type	Reset
7:2	Reserved	Read returns 0.		R	0x00
1	GPIO17ISR3	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		
0	GPIO16ISR3	0x0:	GPIO hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 1 request line		

Table 4-12. GPIO_IMR1A

Address Offset	0x01C		
Physical Address	0x0000 00B4	**Instance**	INT_SCGPIO
Description	This IMR1A register lets the user mask/unmask the expected transition on inputs GPIO[0:7] from generating an interrupt request on gpio_int1_n. The interrupt mask registers are programmed synchronously with the interface OCP clock. Writing 0 in any bit unmasks the corresponding GPIO interrupt event on interrupt request line 1. By default, all interrupts are masked.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7IMR1	GPIO6IMR1	GPIO5IMR1	GPIO4IMR1	GPIO3IMR1	GPIO2IMR1	GPIO1IMR1	GPIO0IMR1

Bits	Field Name	Description		Type	Reset
7	GPIO7IMR1	0x0:	GPIO event not masked on processor 1 request line	RW	1
		0x1:	GPIO event masked on processor 1 request line		
6	GPIO6IMR1	0x0:	GPIO event not masked on processor 1 request line	RW	1
		0x1:	GPIO event masked on processor 1 request line		
5	GPIO5IMR1	0x0:	GPIO event not masked on processor 1 request line	RW	1
		0x1:	GPIO event masked on processor 1 request line		
4	GPIO4IMR1	0x0:	GPIO event not masked on processor 1 request line	RW	1
		0x1:	GPIO event masked on processor 1 request line		
3	GPIO3IMR1	0x0:	GPIO event not masked on processor 1 request line	RW	1
		0x1:	GPIO event masked on processor 1 request line		
2	GPIO2IMR1	0x0:	GPIO event not masked on processor 1 request line	RW	1
		0x1:	GPIO event masked on processor 1 request line		

Bits	Field Name	Description	Type	Reset
1	GPIO1IMR1	0x0: GPIO event not masked on processor 1 request line 0x1: GPIO event masked on processor 1 request line	RW	1
0	GPIO0IMR1	0x0: GPIO event not masked on processor 1 request line 0x1: GPIO event masked on processor 1 request line	RW	1

Table 4-13. GPIO_IMR2A

Address Offset	0x01D		
Physical Address	0x0000 00B5	**Instance**	INT_SCGPIO
Description	This IMR2A register lets the user mask/unmask the expected transition on inputs GPIO[8:15] from generating an interrupt request on gpio_int1_n. The interrupt mask registers are programmed synchronously with the interface OCP clock. Writing 0 in any bit unmasks the corresponding GPIO interrupt event on interrupt request line 1. By default, all interrupts are masked.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15IMR2	GPIO14IMR2	GPIO13IMR2	GPIO12IMR2	GPIO11IMR2	GPIO10IMR2	GPIO9IMR2	GPIO8IMR2

Bits	Field Name	Description	Type	Reset
7	GPIO15IMR2	0x0: GPIO event not masked on processor 1 request line 0x1: GPIO event masked on processor 1 request line	RW	1
6	GPIO14IMR2	0x0: GPIO event not masked on processor 1 request line 0x1: GPIO event masked on processor 1 request line	RW	1
5	GPIO13IMR2	0x0: GPIO event not masked on processor 1 request line 0x1: GPIO event masked on processor 1 request line	RW	1
4	GPIO12IMR2	0x0: GPIO event not masked on processor 1 request line 0x1: GPIO event masked on processor 1 request line	RW	1
3	GPIO11IMR2	0x0: GPIO event not masked on processor 1 request line 0x1: GPIO event masked on processor 1 request line	RW	1
2	GPIO10IMR2	0x0: GPIO event not masked on processor 1 request line 0x1: GPIO event masked on processor 1 request line	RW	1
1	GPIO9IMR2	0x0: GPIO event not masked on processor 1 request line 0x1: GPIO event masked on processor 1 request line	RW	1
0	GPIO8IMR2	0x0: GPIO event not masked on processor 1 request line 0x1: GPIO event masked on processor 1 request line	RW	1

Table 4-14. GPIO_IMR3A

Address Offset	0x01E		
Physical Address	0x0000 00B6	**Instance**	INT_SCGPIO
Description	This IMR3A register lets the user mask/unmask the expected transition on inputs GPIO[16:17] from generating an interrupt request on gpio_int1_n. The interrupt mask registers are programmed synchronously with the interface OCP clock. Writing 0 in any bit unmasks the corresponding GPIO interrupt event on interrupt request line 1. By default, all interrupts are masked.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17IMR3	GPIO16IMR3

Bits	Field Name	Description	Type	Reset
7:2	Reserved	Read returns 0.	R	0x00
1	GPIO17IMR3	0x0: GPIO event not masked on processor 1 request line 0x1: GPIO event masked on processor 1 request line	RW	1
0	GPIO16IMR3	0x0: GPIO event not masked on processor 1 request line 0x1: GPIO event masked on processor 1 request line	RW	1

Table 4-15. GPIO_ISR1B

Address Offset	0x01F		
Physical Address	0x0000 00B7	**Instance**	INT_SCGPIO
Description	This ISR1B register determines which input GPIO[0:7] pin triggered the interrupt line gpio_int2_n request. As this table shows, bit 0 corresponds to po_pad_gpio[0], bit 1 to po_pad_gpio[7], etc. When a bit in this register is set to 1, the corresponding GPIO pin is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR1 register. If the user writes 0 to a bit in this register, the value does not change when in COR mode. The ISR1B register is synchronous with the interface OCP clock. A read of 1 in any bit means that the corresponding interrupt event is active on interrupt request line 2.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7ISR1	GPIO6ISR1	GPIO5ISR1	GPIO4ISR1	GPIO3ISR1	GPIO2ISR1	GPIO1ISR1	GPIO0ISR1

Bits	Field Name	Description	Type	Reset
7	GPIO7ISR1	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
6	GPIO6ISR1	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
5	GPIO5ISR1	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
4	GPIO4ISR1	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
3	GPIO3ISR1	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
2	GPIO2ISR1	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
1	GPIO1ISR1	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
0	GPIO0ISR1	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0

Table 4-16. GPIO_ISR2B

Address Offset	0x020		
Physical Address	0x0000 00B8	**Instance**	INT_SCGPIO
Description	This ISR2B register determines which input GPIO[8:15] pin triggered the interrupt line gpio_int2_n request. As this table shows, bit 0 corresponds to po_pad_gpio[8], bit 1 to po_pad_gpio[9], etc. When a bit in this register is set to 1, the corresponding GPIO pin is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR2 register. If the user writes 0 to a bit in this register, the value does not change when in COR mode. The ISR2B register is synchronous with the interface OCP clock. A read of 1 in any bit means that the corresponding interrupt event is active on interrupt request line 2.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15ISR2	GPIO14ISR2	GPIO13ISR2	GPIO12ISR2	GPIO11ISR2	GPIO10ISR21	GPIO9ISR2	GPIO8ISR2

Bits	Field Name	Description	Type	Reset
7	GPIO15ISR2	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
6	GPIO14ISR2	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
5	GPIO13ISR2	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
4	GPIO12ISR2	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
3	GPIO11ISR2	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
2	GPIO10ISR2	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
1	GPIO9ISR2	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0
0	GPIO8ISR2	0x0: GPIO hardware interrupt inactive on processor 2 request line 0x1: GPIO hardware interrupt active on processor 2 request line	RW	0

Table 4-17. GPIO_ISR3B

Address Offset	0x021		
Physical Address	0x0000 00B9	**Instance**	INT_SCGPIO
Description	This ISR3B register determines which input GPIO[16:17] pins triggered the interrupt line gpio_int2_n request. As this table shows, bit 0 corresponds to po_pad_gpio[16] and bit 1 to po_pad_gpio[17]. When a bit in this register is set to 1, the corresponding GPIO pin is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR3 register. If the user writes 0 to a bit in this register, the value does not change when in COR mode. The ISR3B register is synchronous with the interface OCP clock. A read of 1 in any bit means that the corresponding interrupt event is active on interrupt request line 2.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17ISR3	GPIO16ISR3

Bits	Field Name	Description		Type	Reset
7:2	Reserved	Read returns 0.		R	0x00
1	GPIO17ISR3	0x0:	GPIO hardware interrupt inactive on processor 2 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 2 request line		
0	GPIO16ISR3	0x0:	GPIO hardware interrupt inactive on processor 2 request line	RW	0
		0x1:	GPIO hardware interrupt active on processor 2 request line		

Table 4-18. GPIO_IMR1B

Address Offset	0x22		
Physical Address	0x0000 00BA	**Instance**	INT_SCGPIO
Description	This IMR1B register lets the user mask/unmask the expected transition on inputs GPIO[0:7] from generating an interrupt request on gpio_int2_n. The interrupt mask registers are programmed synchronously with the interface OCP clock. Writing 0 in any bit unmasks the corresponding GPIO interrupt event on interrupt request line 2. By default, all interrupts are masked.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7IMR1	GPIO6IMR1	GPIO5IMR1	GPIO4IMR1	GPIO3IMR1	GPIO2IMR1	GPIO1IMR1	GPIO0IMR1

Bits	Field Name	Description		Type	Reset
7	GPIO7IMR1	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
6	GPIO6IMR1	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
5	GPIO5IMR1	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
4	GPIO4IMR1	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
3	GPIO3IMR1	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
2	GPIO2IMR1	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
1	GPIO1IMR1	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
0	GPIO0IMR1	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		

Table 4-19. GPIO_IMR2B

Address Offset	0x23		
Physical Address	0x0000 00BB	**Instance**	INT_SCGPIO
Description	This IMR2B register lets the user mask/unmask the expected transition on inputs GPIO[8:15] from generating an interrupt request on gpio_int2_n. The interrupt mask registers are programmed synchronously with the interface OCP clock. Writing 0 in any bit unmasks the corresponding GPIO interrupt event on interrupt request line 2. By default, all interrupts are masked.		
Type	RW		
Write Latency			

7	6	5	5	4	2	1	0
GPIO15IMR2	GPIO14IMR2	GPIO13IMR2	GPIO12IMR2	GPIO11IMR2	GPIO10IMR2	GPIO9IMR2	GPIO8IMR2

Bits	Field Name	Description		Type	Reset
7	GPIO15IMR2	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
6	GPIO14IMR2	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
5	GPIO13IMR2	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
4	GPIO12IMR2	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
3	GPIO11IMR2	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
2	GPIO10IMR2	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
1	GPIO9IMR2	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
0	GPIO8IMR2	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		

Table 4-20. GPIO_IMR3B

Address Offset	0x24		
Physical Address	0x0000 00BC	**Instance**	INT_SCGPIO
Description	This IMR3B register lets the user mask/unmask the expected transition on inputs GPIO[16:17] from generating an interrupt request on gpio_int2_n. The interrupt mask registers are programmed synchronously with the interface OCP clock. Writing 0 in any bit unmasks the corresponding GPIO interrupt event on interrupt request line 2. By default, all interrupts are masked.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17IMR3	GPIO16IMR3

Bits	Field Name	Description		Type	Reset
7:2	Reserved	Read returns 0.		R	0x00
1	GPIO17IMR3	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		
0	GPIO16IMR3	0x0:	GPIO event not masked on processor 2 request line	RW	1
		0x1:	GPIO event masked on processor 2 request line		

Table 4-21. GPIO_EDR1

Address Offset	0x28		
Physical Address	0x0000 00C0	**Instance**	INT_SCGPIO
Description	This interrupt edge-detection register GPIO_EDR1 lets the user define, for each external GPIO[0:3] pin configured as input, the expected edge to trigger an interrupt request. The interrupt request can be generated by a high-to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions accruing (bits are 11). To disable edge detection, the relevant bits corresponding to the GPIO must be reset (00).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO3RISING	GPIO3 FALLING	GPIO2RISING	GPIO2 FALLING	GPIO1RISING	GPIO1 FALLING	GPIO0RISING	GPIO0 FALLING

Bits	Field Name	Description	Type	Reset
7	GPIO3RISING	0x0: GPIO rising detection disabled 0x1: GPIO rising detection enabled	RW	0
6	GPIO3FALLING	0x0: GPIO falling detection disabled 0x1: GPIO falling detection enabled	RW	0
5	GPIO2RISING	0x0: GPIO rising detection disabled 0x1: GPIO rising detection enabled	RW	0
4	GPIO2FALLING	0x0: GPIO falling detection disabled 0x1: GPIO falling detection enabled	RW	0
3	GPIO1RISING	0x0: GPIO rising detection disabled 0x1: GPIO rising detection enabled	RW	0
2	GPIO1FALLING	0x0: GPIO falling detection disabled 0x1: GPIO falling detection enabled	RW	0
1	GPIO0RISING	0x0: GPIO rising detection disabled 0x1: GPIO rising detection enabled	RW	0
0	GPIO0FALLING	0x0: GPIO falling detection disabled 0x1: GPIO falling detection enabled	RW	0

Table 4-22. GPIO_EDR2

Address Offset	0x29		
Physical Address	0x0000 00C1	**Instance**	INT_SCGPIO
Description	This interrupt edge-detection register GPIO_EDR2 lets the user define, for each external GPIO[4:7] pin configured as input, the expected edge to trigger an interrupt request. The interrupt request can be generated by a high-to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions accruing (bits are 11). To disable edge detection, the relevant bits corresponding to the GPIO must be reset (00).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7RISING	GPIO7 FALLING	GPIO6RISING	GPIO6 FALLING	GPIO5RISING	GPIO5 FALLING	GPIO4RISING	GPIO4 FALLING

Bits	Field Name	Description		Type	Reset
7	GPIO7RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
6	GPIO7FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		
5	GPIO6RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
4	GPIO6FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		
3	GPIO5RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
2	GPIO5FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		
1	GPIO4RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
0	GPIO4FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		

Table 4-23. GPIO_EDR3

Address Offset	0x2A		
Physical Address	0x0000 00C2	**Instance**	INT_SCGPIO
Description	This interrupt edge-detection register GPIO_EDR3 lets the user define, for each external GPIO[8:1] pin configured as input, the expected edge to trigger an interrupt request. The interrupt request can be generated by a high-to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions accruing (bits are 11). To disable edge detection, the relevant bits corresponding to the GPIO must be reset (00).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO11RISING	GPIO11 FALLING	GPIO10RISING	GPIO10 FALLING	GPIO9RISING	GPIO9 FALLING	GPIO9 FALLING	GPIO8 FALLING

Bits	Field Name	Description		Type	Reset
7	GPIO11RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
6	GPIO11FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		
5	GPIO10RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
4	GPIO10FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		
3	GPIO9RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
2	GPIO9FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		
1	GPIO8RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
0	GPIO8FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		

Table 4-24. GPIO_EDR4

Address Offset	0x2B		
Physical Address	0x0000 00C3	**Instance**	INT_SCGPIO
Description	This interrupt edge-detection register GPIO_EDR4 lets the user define, for each external GPIO[13:15] pin configured as input, the expected edge to trigger an interrupt request. The interrupt request can be generated by a high-to-low transition (bits are 01), a low-to-high transition (bits are 11). To disable edge detection, the relevant bits corresponding to the GPIO must be reset (00).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15RISING	GPIO15 FALLING	GPIO14RISING	GPIO14 FALLING	GPIO13RISING	GPIO13 FALLING	GPIO12RISING	GPIO12 FALLING

Bits	Field Name	Description		Type	Reset
7	GPIO15RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
6	GPIO15FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		
5	GPIO14RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		

Bits	Field Name	Description		Type	Reset
4	GPIO14FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		
3	GPIO13RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
2	GPIO13FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		
1	GPIO12RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
0	GPIO12FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		

Table 4-25. GPIO_EDR5

Address Offset	0x2C		
Physical Address	0x0000 00C4	**Instance**	INT_SCGPIO
Description	This interrupt edge-detection register GPIO_EDR lets the user define, for each external GPIO[16:17] pin configured as input, the expected edge to trigger an interrupt request. The interrupt request can be generated by a high-to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions accruing (bits are 11). To disable edge detection, the relevant bits corresponding to the GPIO must be reset (00).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				GPIO17RISING	GPIO17 FALLING	GPIO16RISING	GPIO16 FALLING

Bits	Field Name	Description		Type	Reset
7:4	Reserved	Read returns 0.		R	0x0
3	GPIO17RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
2	GPIO17FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		
1	GPIO16RISING	0x0:	GPIO rising detection disabled	RW	0
		0x1:	GPIO rising detection enabled		
0	GPIO16FALLING	0x0:	GPIO falling detection disabled	RW	0
		0x1:	GPIO falling detection enabled		

Table 4-26. GPIO_SIH_CTRL

Address Offset	0x2D		
Physical Address	0x0000 00C5	**Instance**	INT_SCGPIO
Description	This GPIO SIH control register GPIO_SIH_CTRL lets the user disable a pending incoming event during software interrupt latency by programming 1 in the PENDDIS bit. By writing 0 in the EXCLEN bit, the user disables exclusivity between interrupt request lines gpio_int1_n and gpio_int2_n. The COR bit enables the COR feature. This means that a read access to the ISR clears this register and releases the associated interrupt line (default value). If disabled, a read access to a specific address value clears all ISRs in the SIH.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved					COR	PENDDIS	EXCLEN

Bits	Field Name	Description		Type	Reset
7:3	Reserved	Read returns 0.		R	0x00
2	COR	0x0:	Clear ISR-specific bit field when in write access mode.	RW	0
		0x1:	Clear ISR when in read mode.		
1	PENDDIS	0x0:	Pending event feature is enabled.	RW	0
		0x1:	Pending event feature is disabled.		
0	EXCLEN	0x0:	Exclusivity feature is disabled.	RW	1
		0x1:	Exclusivity feature is enabled.		

4.6.4 Keypad

This section provides information about the interrupts in the keypad module instance in the device. Table 4-27 is the keypad register summary. The registers in the module instance are described separately in Table 4-28 through Table 4-33.

Table 4-27. Keypad Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
KEYP_ISR1	RW	8	0x0000 00E3
KEYP_IMR1	RW	8	0x0000 00E4
KEYP_ISR2	RW	8	0x0000 00E5
KEYP_IMR2	RW	8	0x0000 00E6
KEYP_EDR	RW	8	0x0000 00E8
KEYP_SIH_CTRL	RW	8	0x0000 00E9

Table 4-28. KEYP_ISR1

Address Offset	0x11		
Physical Address	0x0000 00E3	**Instance**	AUX_SCkeypad
Description	This interrupt status ISR1 register is used to determine which input keypad event triggered the interrupt line kbd_int1_n request. As this table shows, bit 0 corresponds to a key-pressed event (ITKP), bit 1 to a long-key-pressed event (ITLK), and bit 2 to a time-out event (ITTO). When a bit in this register is set to 1, the corresponding event is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the interrupt status ISR1 register. If the user writes 0 to a bit in this register, the value does not change when in COR mode. The interrupt status ISR1 register is synchronous with the interface OCP clock.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				ITMISR1	ITTOISR1	ITLKISR1	ITKPISR1

Bits	Field Name	Description		Type	Reset
7:4	Reserved	Read returns 0.		RW	0x0
3	ITMISR1	0x0:	Missing event hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	Missing event hardware interrupt active on processor 1 request line in test mode only		
2	ITTOISR1	0x0:	Time-out hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	Time-out hardware interrupt active on processor 1 request line		
1	ITLKISR1	0x0:	Long-key hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	Long-key hardware interrupt active on processor 1 request line		
0	ITKPISR1	0x0:	Key-pressed hardware interrupt inactive on processor 1 request line	RW	0
		0x1:	Key-pressed hardware interrupt active on processor 1 request line		

Table 4-29. KEYP_IMR1

Address Offset	0x12		
Physical Address	0x0000 00E4	**Instance**	AUX_SCkeypad
Description	This IMR1 register lets the user mask the expected transition on keypad event from generating an interrupt request on KEYP_INT1_n. The interrupt mask registers are programmed synchronously with the interface OCP clock.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				ITMISIMR1	ITTOIMR1	ITLKIMR1	ITKPIMR1

Bits	Field Name	Description		Type	Reset
7:4	Reserved	Read returns 0.		RW	0x0
3	ITMISIMR1	0x0:	Key-pressed event not masked on processor 1 request line	RW	1
		0x1:	Missed event masked on processor 1 request line (active in test mode only)		
2	ITTOIMR1	0x0:	Time-out event not masked on processor 1 request line	RW	1
		0x1:	Time-out event masked on processor 1 request line		
1	ITLKIMR1	0x0:	Long-key event not masked on processor 1 request line	RW	1
		0x1:	Long-key event masked on processor 1 request line		
0	ITKPIMR1	0x0:	Key-pressed event not masked on processor 1 request line	RW	1
		0x1:	Key-pressed event masked on processor 1 request line		

Table 4-30. KEYP_ISR2

Address Offset	0x13		
Physical Address	0x0000 00E5	**Instance**	AUX_SCkeypad
Description	This ISR2 register determines which input keypad event triggered the interrupt line KEYP_INT2_n request. As this table shows, bit 0 corresponds to a ITKP, bit 1 to a ITLK, and bit 2 to a ITTO. When a bit in this register is set to 1, the corresponding event is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR2 register. If the user writes 0 to a bit in this register, the value does not change when in COR mode. The ISR2 register is synchronous with the interface OCP clock.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				ITMISR2	ITTOISR2	ITLKISR2	ITKPISR2

Bits	Field Name	Description		Type	Reset
7:4	Reserved	Read returns 0.		RW	0x0
3	ITMISR2	0x0:	Missing event hardware interrupt inactive on processor 2 request line	RW	0
		0x1:	Missing event hardware interrupt active on processor 2 request line in test mode only.		
2	ITTOISR2	0x0:	Time-out hardware interrupt inactive on processor 2 request line	RW	0
		0x1:	Time-out hardware interrupt active on processor 2 request line		
1	ITLKISR2	0x0:	Long-key hardware interrupt inactive on processor 2 request line	RW	0
		0x1:	Long-key hardware interrupt active on processor 2 request line		
0	ITKPISR2	0x0:	Key-pressed event not masked on processor 1 request line	RW	0
		0x1:	Key-pressed event masked on processor 1 request line		

Table 4-31. KEYP_IMR2

Address Offset	0x14		
Physical Address	0x0000 00E6	**Instance**	AUX_SCkeypad
Description	This IMR2 register lets the user mask the expected transition on keypad event from generating an interrupt request on KEYP_INT2_n. The interrupt mask registers are programmed synchronously with the interface OCP clock.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				ITMISIMR2	ITTOIMR2	ITLKIMR2	ITKPIMR2

Bits	Field Name	Description		Type	Reset
7:4	Reserved	Read returns 0.		RW	0x0
3	ITMISIMR2	0x0:	Key-pressed event not masked on processor 2 request line	RW	1
		0x1:	Missed event masked on processor 2 request line (active in test mode only)		
2	ITTOIMR2	0x0:	Time-out event not masked on processor 2 request line	RW	1
		0x1:	Time-out event masked on processor 2 request line		
1	ITLKIMR2	0x0:	Long-key event not masked on processor 2 request line	RW	1
		0x1:	Long-key event masked on processor 2 request line		
0	ITKPIMR2	0x0:	Key-pressed event not masked on processor 2 request line	RW	1
		0x1:	Key-pressed event masked on processor 2 request line		

Table 4-32. KEYP_EDR

Address Offset	0x16		
Physical Address	0x0000 00C3	**Instance**	AUX_SCkeypad
Description	This interrupt edge-detection register KEYP_EDR lets the user define, for each external event (key pressed, long key, and time-out event), the expected edge to trigger an interrupt request. The interrupt request can be generated by a high-to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions accruing (bits are 11). To disable edge detection, the bits corresponding to the keypad event must be reset (00).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ITMISRISING	ITMISFALLING	ITTORISING	ITTOFALLING	ITLKRISING	ITLKFALLING	ITKPRISING	ITKPFALLING

Bits	Field Name	Description		Type	Reset
7	ITMISRISING	0x0:	Missed event rising detection disabled	RW	0
		0x1:	Missed event rising detection enabled (test mode only)		
6	ITMISFALLING	0x0:	Missed event falling detection disabled	RW	1
		0x1:	Missed event falling detection enabled (test mode only)		
5	ITTORISING	0x0:	Time-out event rising detection disabled	RW	0
		0x1:	Time-out event rising detection enabled		
4	ITTOFALLING	0x0:	Time-out event falling detection disabled	RW	1
		0x1:	Time-out event falling detection enabled		
3	ITLKRISING	0x0:	Long-key event rising detection disabled	RW	0
		0x1:	Long-key event rising detection enabled		
2	ITLKFALLING	0x0:	Long-key event falling detection disabled	RW	1

Bits	Field Name	Description		Type	Reset
		0x1:	Long-key event falling detection enabled		
1	ITKPRISING	0x0:	Key-pressed event rising detection disabled	RW	0
		0x1:	Key-pressed event rising detection enabled		
0	ITKPFALLING	0x0:	Key-pressed event falling detection disabled	RW	1
		0x1:	Key-pressed event falling detection enabled		

Table 4-33. KEYP_SIH_CTRL

Address Offset	0x17		
Physical Address	0x0000 00E9	**Instance**	AUX_SCkeypad
Description	This KEYP SIH control register KEYP_SIH_CTRL lets the user disable a pending incoming event during software interrupt latency by programming 1 in the PENDDIS bit. By writing 0 in the EXCLEN bit, the user disables exclusivity between interrupt request lines keyp_int1_n and keyp_int2_n. The COR bit enables the COR feature. This means that a read access to the ISR clears this register and releases the associated interrupt line (default value). If disabled, a read access to a specific address value clears all ISRs in the SIH.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved					COR	PENDDIS	EXCLEN

Bits	Field Name	Description		Type	Reset
7:3	Reserved	Read returns 0.		R	0x00
2	COR	0x0:	Clear ISR-specific bit field when in write access mode.	RW	0
		0x1:	Clear ISR when in read mode.		
1	PENDDIS	0x0:	Pending event feature is enabled.	RW	0
		0x1:	Pending event feature is disabled.		
0	EXCLEN	0x0:	Exclusivity is disabled.	RW	1
		0x1:	Exclusivity is enabled.		

4.6.5 MADC

This section provides information about the interrupts in the MADC module instance in the device. Table 4-34 is the MADC register summary. The registers in the module instance are described separately in Table 4-35 through Table 4-40.

Table 4-34. MADC Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
MADC_ISR1	RW	8	0x0000 0061
MADC_IMR1	RW	8	0x0000 0062
MADC_ISR2	RW	8	0x0000 0063
MADC_IMR2	RW	8	0x0000 0064
MADC_EDR	RW	8	0x0000 0066
MADC_SIH_CTRL	RW	8	0x0000 0067

Table 4-35. MADC_ISR1

Address Offset	0x61		
Physical Address	0x0000 0061	**Instance**	AUX_SCMADC
Description	This ISR1 register determines which end-of-sequence (RT, SW1, SW2, or USB) triggered the interrupt line po_madc_p1_n request. When a bit in this register is set to 1, the corresponding end-of-sequence is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR1 register. When a bit in this register is set to 1, the corresponding interrupt line is released. If the user writes 0 to a bit in this register, the value does not change. The ISR1 register is synchronous with the interface OCP clock.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RSVD4	RSVD3	RSVD2	RSVD1	USB_ISR1	SW2_ISR1	SW1_ISR1	RT_ISR1

Bits	Field Name	Description	Type	Reset
7	RSVD4	Read returns 0.	Reserved	0
6	RSVD3	Read returns 0.	Reserved	0
5	RSVD2	Read returns 0.	Reserved	0
4	RSVD1	Read returns 0.	Reserved	0
3	USB_ISR1	0: Interrupt not set 1: Interrupt set	RW	0
2	SW2_ISR1	0: Interrupt not set 1: Interrupt set	RW	0
1	SW1_ISR1	0: Interrupt not set 1: Interrupt set	RW	0
0	RT_ISR1	0: Interrupt not set 1: Interrupt set	RW	0

Table 4-36. MADC_IMR1

Address Offset	0x62		
Physical Address	0x0000 0062	**Instance**	AUX_SCMADC
Description	This IMR1 register lets the user mask the expected transition on end-of-sequence from generating an interrupt request on po_madc_p1_n. The interrupt mask registers are programmed synchronously with the interface OCP clock.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RSVD4	RSVD3	RSVD2	RSVD1	USB_IMR1	SW2_IMR1	SW1_IMR1	RT_IMR1

Bits	Field Name	Description	Type	Reset
7	RSVD4	Read returns 0.	Reserved	0
6	RSVD3	Read returns 0.	Reserved	0
5	RSVD2	Read returns 0.	Reserved	0
4	RSVD1	Read returns 0.	Reserved	0
3	USB_IMR1	0: Interrupt is not masked. 1: Interrupt is masked.	RW	1
2	SW2_IMR1	0: Interrupt is not masked. 1: Interrupt is masked.	RW	1
1	SW1_IMR1	0: Interrupt is not masked. 1: Interrupt is masked.	RW	1
0	RT_IMR1	0: Interrupt is not masked. 1: Interrupt is masked.	RW	1

Table 4-37. MADC_ISR2

Address Offset	0x63		
Physical Address	0x0000 0063	**Instance**	AUX_SCMADC
Description	This ISR2 register determines which end-of-sequence (RT, SW1, SW2, or USB) triggered the interrupt line po_madc_p2_n request. When a bit in this register is set to 1, the corresponding end-of-sequence is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR2 register. When a bit in this register is set to 1, the corresponding interrupt line is released. If the user writes 0 to a bit in this register, the value does not change. The ISR2 register is synchronous with the interface OCP clock.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RSVD4	RSVD3	RSVD2	RSVD1	USB_ISR2	SW2_ISR2	SW1_ISR2	RT_ISR2

Bits	Field Name	Description	Type	Reset
7	RSVD4	Read returns 0.	Reserved	0
6	RSVD3	Read returns 0.	Reserved	0
5	RSVD2	Read returns 0.	Reserved	0
4	RSVD1	Read returns 0.	Reserved	0
3	USB_ISR2	0: Interrupt not set 1: Interrupt set	RW	0
2	SW2_ISR2	0: Interrupt not set 1: Interrupt set	RW	0
1	SW1_ISR2	0: Interrupt not set	RW	0

Bits	Field Name	Description	Type	Reset
		1: Interrupt set		
0	RT_ISR2	0: Interrupt not set	RW	0
		1: Interrupt set		

Table 4-38. MADC_IMR2

Address Offset	0x64		
Physical Address	0x0000 0064	**Instance**	AUX_SCMADC
Description	This IMR2 register lets the user mask the expected transition on end-of-sequence from generating an interrupt request on po_madc_p2_n. The interrupt mask registers are programmed synchronously with the interface OCP clock.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RSVD4	RSVD3	RSVD2	RSVD1	USB_IMR2	SW2_IMR2	SW1_IMR2	RT_IMR2

Bits	Field Name	Description	Type	Reset
7	RSVD4	Read returns 0.	Reserved	0
6	RSVD3	Read returns 0.	Reserved	0
5	RSVD2	Read returns 0.	Reserved	0
4	RSVD1	Read returns 0.	Reserved	0
3	USB_IMR2	0: Interrupt is not masked.	RW	1
		1: Interrupt is masked.		
2	SW2_IMR2	0: Interrupt is not masked.	RW	1
		1: Interrupt is masked.		
1	SW1_IMR2	0: Interrupt is not masked.	RW	1
		1: Interrupt is masked.		
0	RT_IMR2	0: Interrupt is not masked.	RW	1
		1: Interrupt is masked.		

Table 4-39. MADC_EDR

Address Offset	0x66		
Physical Address	0x0000 0066	**Instance**	AUX_SCkeypad
Description	This interrupt edge-detection register MADC_EDR lets the user define, for all signals (end-of-real-time sequence, end-of-SW1 sequence, end-of-SW2 sequence, and end-of-USB sequence) the expected edge to trigger an interrupt request. The interrupt request can be generated by a high-to-low transition (bits are 01), a low-to-high transition (bits are 10) or both transitions accruing (bits are 11). To get falling-edge detection, the bits corresponding to the MADC must be reset (55).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
USB_EDRRISING	USB_EDRFALLING	SW2_EDRRISING	SW2_EDRFALLING	SW1_EDRRISING	SW1_EDRFALLING	RT_EDRRISING	RT_EDRFALLING

Bits	Field Name	Description	Type	Reset
7	USB_EDRRISING	0: Rising detection disabled 1: Rising detection enabled	RW	0
6	USB_ EDRFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	1
5	SW2_EDRRISING	0: Rising detection disabled 1: Rising detection enabled	RW	0
4	SW2_ EDRFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	1
3	SW1_EDRRISING	0: Rising detection disabled 1: Rising detection enabled	RW	0
2	SW1_ EDRFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	1
1	RT_EDRRISING	0: Rising detection disabled 1: Rising detection enabled	RW	0
0	RT_EDRFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	1

Table 4-40. MADC_SIH_CTRL

Address Offset	0x67		
Physical Address	0x0000 0067	**Instance**	AUX_SCkeypad
Description	This MADC SIH control register lets the user disable a pending incoming event during software interrupt latency by programming 1 in the PENDDIS bit. By writing 0 in the EXCLEN bit, the user disables exclusivity between the interrupt request lines madc_int1_n and madc_int2_n. The COR bit enables the clear-on-read feature. This means that a read access to the ISR clears this register and releases the associated interrupt line (default value). If disabled, a read access to a specific address value clears all ISRs in the SIH.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	COR	PENDDIS	EXCLEN

Bits	Field Name	Description	Type	Reset
7	Reserved	Read returns 0.	RW	0
6	Reserved	Read returns 0.	RW	0
5	Reserved	Read returns 0.	RW	0
4	Reserved	Read returns 0.	RW	0
3	Reserved	Read returns 0.	RW	0
2	COR	0: Clear ISR on read. 1: Clear ISR-specific bit field when write access.	Reserved	1
1	PENDDIS	0: Pending event enabled 1: Pending event disabled	RW	1
0	EXCLEN	0: Exclusivity disabled 1: Exclusivity enabled	RW	1

4.6.6 Power Interrupts

This section provides information about power interrupts in the INT module instance in the device. Table 4-41 is the INT register summary. The registers in the module instance are described separately in Table 4-42 through Table 4-48.

Table 4-41. INT Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
PWR_ISR1	RW	8	0x0000 002E
PWR_IMR1	RW	8	0x0000 002F
PWR_ISR2	RW	8	0x0000 0030
PWR_IMR2	RW	8	0x0000 0031
PWR_EDR1	RW	8	0x0000 0033
PWR_EDR2	RW	8	0x0000 0034
PWR_SIH_CTRL	RW	8	0x0000 0035

Table 4-42. PWR_ISR1

Address Offset	0x00		
Physical Address	0x0000 002E	**Instance**	POWERINT
Description	The interrupt status register ISR1 is used to determine which input event triggered the interrupt line int1_n request (VRRTC domain).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	PWROK_TIMEOUT	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset
7	SC_DETECT		RW	0
6	MBCHG		RW	0
5	PWROK_TIMEOUT		RW	0
4	HOT_DIE		RW	0
3	RTC_IT		RW	0
2	USB_PRES		RW	0
1	CHG_PRES		RW	0
0	PWRON	Because the PWRON signal is active low, the signal is inverted when used.	RW	0

Table 4-43. PWR_IMR1

Address Offset	0x01		
Physical Address	0x0000 002F	**Instance**	POWERINT
Description	This interrupt mask register IMR1 allows masking of an event to keep it from generating an interrupt request on _int1_n (VRRTC domain).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	PWROK_TIMEOUT	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset
7	SC_DETECT		RW	0
6	MBCHG		RW	0
5	PWROK_TIMEOUT		RW	0
4	HOT_DIE		RW	0
3	RTC_IT		RW	0
2	USB_PRES		RW	0
1	CHG_PRES		RW	0
0	PWRON		RW	0

Table 4-44. PWR_ISR2

Address Offset	0x02		
Physical Address	0x0000 0030	**Instance**	POWERINT
Description	This interrupt status register ISR2 is used to determine which input event triggered the interrupt line int2_n request (VRRTC domain).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	PWROK_TIMEOUT	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset
7	SC_DETECT		RW	0
6	MBCHG		RW	0
5	PWROK_TIMEOUT		RW	0
4	HOT_DIE		RW	0
3	RTC_IT		RW	0
2	USB_PRES		RW	0
1	CHG_PRES		RW	0

Bits	Field Name	Description	Type	Reset
0	PWRON	Because the PWRON signal is active low, the signal is inverted when used.	RW	0

Table 4-45. PWR_IMR2

Address Offset	0x03		
Physical Address	0x0000 0031	**Instance**	POWERINT
Description	This interrupt mask register IMR2 allows masking of an event to keep it from generating an interrupt request on _int1_n (VRRTC domain).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	PWROK_TIMEOUT	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset
7	SC_DETECT		RW	0
6	MBCHG		RW	0
5	PWROK_TIMEOUT		RW	0
4	HOT_DIE		RW	0
3	RTC_IT		RW	0
2	USB_PRES		RW	0
1	CHG_PRES		RW	0
0	PWRON		RW	0

Table 4-46. PWR_EDR1

Address Offset	0x05		
Physical Address	0x0000 0033	**Instance**	POWERINT
Description	Power edge-detection register 1 for PWRON, charger presence, USB presence, and RTC IT (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RTC_IT_ RISING	RTC_IT_ FALLING	USB_PRES_RISING	USB_PRES_FALLING	CHG_PRES_RISING	CHG_PRES_FALLING	PWRON_RISING	PWRON_FALLING

Bits	Field Name	Description	Type	Reset
7	RTC_IT_RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	1
6	RTC_IT_FALLING	0: Falling-edge detection disabled	RW	1

Bits	Field Name	Description	Type	Reset
		1: Falling-edge detection enabled		
5	USB_PRES_RISING	0: Rising-edge detection disabled	RW	1
		1: Rising-edge detection enabled		
4	USB_PRES_FALLING	0: Falling-edge detection disabled	RW	1
		1: Falling-edge detection enabled		
3	CHG_PRES_RISING	0: Rising-edge detection disabled	RW	1
		1: Rising-edge detection enabled		
2	CHG_PRES_FALLING	0: Falling-edge detection disabled	RW	1
		1: Falling-edge detection enabled		
1	PWRON_RISING	0: Rising-edge detection disabled	RW	1
		1: Rising-edge detection enabled		
0	PWRON_FALLING	0: Falling-edge detection disabled	RW	1
		1: Falling-edge detection enabled		

Table 4-47. PWR_EDR2

Address Offset	0x06		
Physical Address	0x0000 0034	**Instance**	POWERINT
Description	Power edge-detection register 2 short-circuit detect, main battery charger, power ok, and hot-die presences (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_DETECT_RISING	SC_DETECT_FALLING	MBCHG_RISING	MBCHG_FALLING	PWROK_TIMEOUT_RISING	PWROK_TIMEOUT_FALLING	HOT_DIE_RISING	HOT_DIE_FALLING

Bits	Field Name	Description	Type	Reset
7	SC_DETECT_RISING	0: Rising-edge detection disabled	RW	1
		1: Rising-edge detection enabled		
6	SC_DETECT_FALLING	0: Falling-edge detection disabled	RW	1
		1: Falling-edge detection enabled		
5	MBCHG_RISING	0: Rising-edge detection disabled	RW	1
		1: Rising-edge detection enabled		
4	MBCHG_FALLING	0: Falling-edge detection disabled	RW	1
		1: Falling-edge detection enabled		
3	PWROK_TIMEOUT_RISING	0: Rising-edge detection disabled	RW	1
		1: Rising-edge detection enabled		
2	PWROK_TIMEOUT_FALLING	0: Falling-edge detection disabled	RW	1
		1: Falling-edge detection enabled		
1	HOT_DIE_RISING	0: Rising-edge detection disabled	RW	1
		1: Rising-edge detection enabled		
0	HOT_DIE_FALLING	0: Falling-edge detection disabled	RW	1

Bits	Field Name	Description	Type	Reset
		1: Falling-edge detection enabled		

Table 4-48. PWR_SIH_CTRL

Address Offset	0x07		
Physical Address	0x0000 0035	**Instance**	POWERINT
Description	Lets the user disable a pending incoming event during software interrupt latency by programming 1 in the PENDDIS field. By writing 0 in the EXCLEN field, the user disables exclusivity between interrupt request lines int1_n and int2_n. The COR bit enables the clear-on-read feature. This means that a read access to the ISR clears this register and releases the associated interrupt line (default value). If disabled, a read access to a specific address value clears all ISRs in the SIH (VRRTC domain).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved					COR	PENDDIS	EXCLEN

Bits	Field Name	Description	Type	Reset
7:3	Reserved		R	0x00
2	COR		RW	0
1	PENDDIS		RW	0
0	EXCLEN		RW	1

4.6.7 USB

This section provides information about the interrupts in the USB module instance in the device. Table 4-49 is the USB register summary. The registers in the module instance are described separately in Table 4-50 through Table 4-88.

Table 4-49. USB Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
USB_INT_EN_RISE	RW	8	0x0000 000D
USB_INT_EN_RISE_SET	RW	8	0x0000 000E
USB_INT_EN_RISE_CLR	RW	8	0x0000 000F
USB_INT_EN_FALL	RW	8	0x0000 0010
USB_INT_EN_FALL_SET	RW	8	0x0000 0011
USB_INT_EN_FALL_CLR	RW	8	0x0000 0012
USB_INT_STS	R	8	0x0000 0013
USB_INT_LATCH	R	8	0x0000 0014
CARKIT_INT_EN	RW	8	0x0000 001D
CARKIT_INT_EN_SET	RW	8	0x0000 001E
CARKIT_INT_EN_CLR	RW	8	0c0000 001F
CARKIT_INT_STS	R	8	0x0000 0020
CARKIT_INT_LATCH	R	8	0x0000 0021
OTHER_INT_EN_RISE	RW	8	0x0000 0086
OTHER_INT_EN_RISE_SET	RW	8	0x0000 0087
OTHER_INT_EN_RISE_CLR	RW	8	0x0000 0088
OTHER_INT_EN_FALL	RW	8	0x0000 0089
OTHER_INT_EN_FALL_SET	RW	8	0x0000 008A
OTHER_INT_EN_FALL_CLR	RW	8	0x0000 008B
OTHER_INT_STS	R	8	0x0000 008C
OTHER_INT_LATCH	R	8	0x0000 008D

Table 4-49. USB Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address
ID_INT_EN_RISE	RW	8	0x0000 008E
ID_INT_EN_RISE_SET	RW	8	0x0000 008F
ID_INT_EN_RISE_CLR	RW	8	0x0000 0090
ID_INT_EN_FALL	RW	8	0x0000 0091
ID_INT_EN_FALL_SET	RW	8	0x0000 0092
ID_INT_EN_FALL_CLR	RW	8	0x0000 0093
ID_INT_STS	RW	8	0x0000 0094
ID_INT_LATCH	R	8	0x0000 0095
CARKIT_SM_1_INT_EN	RW	8	0x0000 0097
CARKIT_SM_1_INT_EN_SET	RW	8	0x0000 0098
CARKIT_SM_1_INT_EN_CLR	RW	8	0x0000 0099
CARKIT_SM_1_INT_STS	RW	8	0x0000 009A
CARKIT_SM_1_INT_LATCH	R	8	0x0000 009B
CARKIT_SM_2_INT_EN	RW	8	0x0000 009C
CARKIT_SM_2_INT_EN_SET	RW	8	0x0000 009D
CARKIT_SM_2_INT_EN_CLR	RW	8	0x0000 009E
CARKIT_SM_2_INT_STS	RW	8	0x0000 009F
CARKIT_SM_2_INT_LATCH	R	8	0x0000 00A0

Table 4-50. USB_INT_EN_RISE

Address Offset	0x0D		
Physical Address	0x0000 000D	**Instance**	USB_SCUSB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_RISE	Generates an interrupt event notification when IDGND changes from low to high Event is automatically masked if IDPULLUP bit is cleared to 0 and for 50 ms after IDPULLUP is set to 1.	RW	1
3	SESSEND_RISE	Generates an interrupt event notification when SESSEND changes from low to high	RW	1

Bits	Field Name	Description	Type	Reset
2	SESSVALID_RISE	Generates an interrupt event notification when SESSVALID changes from low to high. SESSVALID is the same as UTMI + AValid.	RW	1
1	VBUSVALID_RISE	Generates an interrupt event notification when VBUSVALID changes from low to high	RW	1
0	HOSTDISCONNECT_RISE	Generates an interrupt event notification when HOSTDISCONNECT changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown are set to 1b).	RW	1

Table 4-51. USB_INT_EN_RISE_SET

Address Offset	0x0E		
Physical Address	0x0000 000E	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the USB_INT_EN_RISE register with the read/set-only property (writing 1 sets a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_RISE		RW	1
3	SESSEND_RISE		RW	1
2	SESSVALID_RISE		RW	1
1	VBUSVALID_RISE		RW	1
0	HOSTDISCONNECT_RISE		RW	1

Table 4-52. USB_INT_EN_RISE_CLR

Address Offset	0x0F		
Physical Address	0x0000 000F	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the USB_INT_EN_RISE register with the read/clear-only property (writing 1 clears a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_RISE		RW	1
3	SESSEND_RISE		RW	1
2	SESSVALID_RISE		RW	1
1	VBUSVALID_RISE		RW	1
0	HOSTDISCONNECT_RISE		RW	1

Table 4-53. USB_INT_EN_FALL

Address Offset	0x10		
Physical Address	0x0000 0010	**Instance**	USB_SCUSB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_FALL	Generates an interrupt event notification when IDGND changes from high to low Event is automatically masked if IDPULLUP bit is cleared to 0 and for 50 ms after IDPULLUP is set to 1.	RW	1
3	SESSEND_FALL	Generates an interrupt event notification when SESSEND changes from high to low	RW	1
2	SESSVALID_FALL	Generates an interrupt event notification when SESSVALID changes from high to low. SESSVALID is the same as UTMI + AValid.	RW	1

Bits	Field Name	Description	Type	Reset
1	VBUSVALID_FALL	Generates an interrupt event notification when VBUSVALID changes from high to low	RW	1
0	HOSTDISCONNECT_FALL	Generates an interrupt event notification when HOSTDISCONNECT changes from high to low. Applicable only in host mode (DpPulldown and DmPulldown are set to 1b).	RW	1

Table 4-54. USB_INT_EN_SET

Address Offset	0x11		
Physical Address	0x0000 0011	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the USB_INT_EN_FALL register with the read/set-only property (writing 1 sets a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_FALL		RW	1
3	SESSEND_FALL		RW	1
2	SESSVALID_FALL		RW	1
1	VBUSVALID_FALL		RW	1
0	HOSTDISCONNECT_FALL		RW	1

Table 4-55. USB_INT_EN_CLR

Address Offset	0x12		
Physical Address	0x0000 0012	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the USB_INT_EN_FALL register with the read/clear-only property (writing 1 clears a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_FALL		RW	1
3	SESSEND_FALL		RW	1
2	SESSVALID_FALL		RW	1
1	VBUSVALID_FALL		RW	1
0	HOSTDISCONNECT_FALL		RW	1

Table 4-56. USB_INT_STS

Address Offset	0x13		
Physical Address	0x0000 0013	**Instance**	USB_SCUSB
Description	Indicates the current value of the interrupt source signal		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			IDGND	SESSEND	SESSVALID	VBUSVALID	HOSTDISCONNECT

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND	Current value of UTMI + IDGND output. This bit is not updated if the IDPULLUP bit is reset to 0 and for 50 ms after IDPULLUP is set to 1.	RW	0
3	SESSEND	Current value of UTMI + SESSEND output	RW	0
2	SESSVALID	Current value of UTMI + SESSVALID output. SESSVALID is the same as UTMI + AValid.	RW	0
1	VBUSVALID	Current value of UTMI + VBUSVALID output	RW	0
0	HOSTDISCONNECT	Current value of UTMI + HOSTDISCONNECT output. Applicable only in host mode. Automatically reset to 0 when low-power mode is entered.	RW	0

Table 4-57. USB_INT_LATCH

Address Offset	0x14		
Physical Address	0x0000 0014	**Instance**	USB_SCUSB
Description	These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY automatically clears all bits when the link reads this register, or when the low-power mode is entered. The PHY also clears this register when serial mode or carkit mode is entered, regardless of the value of ClockSuspendM. The PHY follows the rules defined in Table 26 of the ULPI specification for setting any latch register bit. **Note:** If register read data is returned to the link in the same cycle that a USB interrupt latch bit is to be set, the interrupt condition is given immediately in the register read data and the latch bit is not set. **Note:** It is optional for the link to read the USB interrupt latch register in synchronous mode, because the RX CMD byte already indicates the interrupt source directly.		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			IDGND_LATCH	SESSEND_LATCH	SESSVALID_LATCH	VBUSVALID_LATCH	HOSTDISCONNECT_LATCH

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_LATCH	Set to 1 by the PHY when an unmasked event occurs on IDGND. Cleared when this register is read.	R	0
3	SESSEND_LATCH	Set to 1 by the PHY when an unmasked event occurs on SESSEND. Cleared when this register is read.	R	0
2	SESSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on SESSVALID. Cleared when this register is read. SESSVALID is the same as UTMI + AValid.	R	0
1	VBUSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on VBUSVALID. Cleared when this register is read.	RW	0
0	HOSTDISCONNECT_LATCH	Set to 1 by the PHY when an unmasked event occurs on HOSTDISCONNECT. Cleared when this register is read. Applicable only in host mode.	RW	0

Table 4-58. CARKIT_INT_EN

Address Offset	0x1D		
Physical Address	0x0000 001D	**Instance**	USB_SCUSB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			CARDP_FALL_EN	CARDP_RISE_EN	CARINTDET_EN	IDFLOAT_FALL_EN	IDFLOAT_RISE_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	CARDP_FALL_EN	Generates an interrupt event notification when a falling voltage on the D+ line crosses the VPH_DP_LO threshold. **Warning:** This bit must not be set if the RXPLSEN bit in the CARKIT_PULSE_CONTROL register is set.	RW	0
3	CARDP_RISE_EN	Generates an interrupt event notification when a rising voltage on the D+ line crosses the VPH_DP_LO threshold. **Warning:** This bit must not be set if the RXPLSEN bit in the CARKIT_PULSE_CONTROL register is set.	RW	0
2	CARINTDET_EN	Generates an interrupt event notification when the carkit interrupt timer reaches the value stored in the carkit interrupt delay register. This bit must be set only during stereo mode (SPKRIGHTEN is set and MICEN is cleared in the CARKIT_CONTROL register). 0b: Disabled 1b: Enabled	RW	0
1	IDFLOAT_FALL_EN	Generates an interrupt event notification when the ID pin changes from floating to not floating The IDPULLUP bit in the OTG control register must be set.	RW	0
0	IDFLOAT_RISE_EN	Generates an interrupt event notification when the ID pin changes from not floating to floating The IDPULLUP bit in the OTG control register must be set.	RW	0

Table 4-59. CARKIT_INT_EN_SET

Address Offset	0x1E		
Physical Address	0x0000 001E	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the CARKIT_INT_EN register with the read/set-only property (writing 1 sets a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			CARDP_FALL_EN	CARDP_RISE_EN	CARINTDET_ EN	IDFLOAT_FALL_EN	IDFLOAT_RISE_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	CARDP_FALL_EN		RW	0
3	CARDP_RISE_EN		RW	0
2	CARINTDET_EN		RW	0
1	IDFLOAT_FALL_EN		RW	0
0	IDFLOAT_RISE_EN		RW	0

Table 4-60. CARKIT_INT_EN_CLR

Address Offset	0x1F		
Physical Address	0x0000 001F	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the CARKIT_INT_EN register with the read/clear-only property (writing 1 clears a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			CARDP_FALL_EN	CARDP_RISE_EN	CARINTDET_ EN	IDFLOAT_FALL_EN	IDFLOAT_RISE_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	CARDP_FALL_EN		RW	0
3	CARDP_RISE_EN		RW	0
2	CARINTDET_EN		RW	0
1	IDFLOAT_FALL_EN		RW	0
0	IDFLOAT_RISE_EN		RW	0

Table 4-61. CARKIT_INT_STS

Address Offset	0x20		
Physical Address	0x0000 0020	**Instance**	USB_SCUSB
Description	When a carkit interrupt event notification occurs, the link can read this register to determine which event triggered the interrupt.		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved					CARDP	CARINTDET	IDFLOAT

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	CARDP	Asserted when the D+ line is above the VPH_DP_LO threshold	R	0
1	CARINTDET	Asserted when the CARINTDET_LATCH bit in the CARKIT_INT_LATCH register is set	R	0
0	IDFLOAT	Asserted when the ID pin is floating	R	0

Table 4-62. CARKIT_INT_LATCH

Address Offset	0x21		
Physical Address	0x0000 0021	**Instance**	USB_SCUSB
Description	These bits are set by the PHY when an unmasked carkit event occurs. The PHY automatically clears all bits when the link reads this register, or when low-power mode is entered. **Note:** If register read data is returned to the link in the same cycle that a carkit interrupt latch bit is to be set, the interrupt condition is given immediately in the register read data, and the latch bit is not set.		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved					CARDP_LATCH	CARINTDET_LATCH	IDFLOAT_LATCH

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	CARDP_LATCH	Asserted if the CARDP_FALL_EN bit in the CARKIT_INT_EN register is set when the a falling voltage on the D+ line crosses the VPH_DP_LO threshold Also asserted if the CARDP_RISE_EN is set when a rising voltage crosses the VPH_DP_LO threshold	R	0

Bits	Field Name	Description	Type	Reset
1	CARINTDET_LATCH	Asserted if the CARINTDET_EN bit in the CARKIT_INT_EN register is set and the carkit interrupt timer reaches the value stored in the carkit interrupt delay register. This bit is used only to detect an interrupt from a CEA carkit during stereo audio.	R	0
0	IDFLOAT	Asserted if the IDFLOAT_RISE_EN bit in the CARKIT_INT_EN register is set, and the ID line changes from not floating to floating Also asserted if the IDFLOAT_FALL_EN bit in the CARKIT_INT_EN register is set, and the ID line changes from floating to not floating	R	0

Table 4-63. OTHER_INT_EN_RISE

Address Offset	0x86		
Physical Address	0x0000 0086	**Instance**	USB_SCUSB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
VB_SESS_VLD_RISE_EN	DM_HI_RISE_EN	DP_HI_RISE_EN	Reserved			MANU_RISE_EN	ABNORMAL_STRESS_RISE_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_RISE_EN	If this bit is set, it generates an interrupt event notification when the VB_SESS_VLD pin changes from low to high.	RW	0
6	DM_HI_RISE_EN	If this bit is set, it generates an interrupt event notification when the DM_HI pin changes from low to high.	RW	0
5	DP_HI_RISE_EN	If this bit is set, it generates an interrupt event notification when the DP_HI pin changes from low to high.	RW	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	MANU_RISE_EN	If this bit is set, it generates an interrupt event notification when the MANU pin changes from low to high.	RW	0
0	ABNORMAL_STRESS_RISE_EN	If this bit is set, it generates an interrupt event notification if the stress protection circuit has been activated.	RW	0

Table 4-64. OTHER_INT_EN_RISE_SET

Address Offset	0x87		
Physical Address	0x0000 0087	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the OTHER_INT_EN_RISE_SET register with the read/set-only property (writing 1 sets a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
VB_SESS_VLD_RISE_EN	DM_HI_RISE_EN	DP_HI_RISE_EN	Reserved			MANU_RISE_EN	ABNORMAL_STRESS_RISE_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_RISE_EN		RW	0
6	DM_HI_RISE_EN		RW	0
5	DP_HI_RISE_EN		RW	0
4	Reserved		RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	MANU_RISE_EN		RW	0
0	ABNORMAL_STRESS_RISE_EN		RW	0

Table 4-65. OTHER_INT_EN_RISE_CLR

Address Offset	0x88		
Physical Address	0x0000 0088	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the OTHER_INT_EN_RISE register with the read/clear-only property (writing 1 clears a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
VB_SESS_VLD_RISE_EN	DM_HI_RISE_EN	DP_HI_RISE_EN	Reserved			MANU_RISE_EN	ABNORMAL_STRESS_RISE_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_RISE_EN		RW	0
6	DM_HI_RISE_EN		RW	0
5	DP_HI_RISE_EN		RW	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	MANU_RISE_EN		RW	0
0	ABNORMAL_STRESS_RISE_EN		RW	0

Table 4-66. OTHER_INT_EN_FALL

Address Offset	0x89		
Physical Address	0x0000 0089	**Instance**	USB_SCUSB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
VB_SESS_VLD_FALL_EN	DM_HI_FALL_EN	DP_HI_FALL_EN	Reserved			MANU_FALL_EN	ABNORMAL_STRESS_FALL_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_FALL_EN	If this bit is set, it generates an interrupt event notification when the VB_SESS_VLD pin changes from high to low.	RW	0
6	DM_HI_FALL_EN	If this bit is set, it generates an interrupt event notification when the DM_HI pin changes from high to low.	RW	0
5	DP_HI_FALL_EN	If this bit is set, it generates an interrupt event notification when the DP_HI pin changes from high to low.	RW	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	MANU_FALL_EN	If this bit is set, it generates an interrupt event notification when the MANU pin changes from high to low.	RW	0
0	ABNORMAL_STRESS_FALL_EN	If this bit is set, it generates an interrupt event notification if the stress protection circuit is activated.	RW	0

Table 4-67. OTHER_INT_EN_FALL_SET

Address Offset	0x8A		
Physical Address	0x0000 008A	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the OTHER_INT_EN_FALL register with the read/set-only property (writing 1 sets a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
VB_SESS_VLD_FALL_EN	DM_HI_FALL_EN	DP_HI_FALL_EN	Reserved			MANU_FALL_EN	ABNORMAL_STRESS_FALL_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_FALL_EN		RW	0
6	DM_HI_FALL_EN		RW	0
5	DP_HI_FALL_EN		RW	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	MANU_FALL_EN		RW	0
0	ABNORMAL_STRESS_ FALL_EN		RW	0

Table 4-68. OTHER_INT_EN_FALL_CLR

Address Offset	0x8B		
Physical Address	0x0000 008B	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the OTHER_INT_EN_FALL register with the read/clear-only property (writing 1 clears a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
VB_SESS_VLD_FALL_EN	DM_HI_FALL_EN	DP_HI_FALL_ EN	Reserved			MANU_FALL_EN	ABNORMAL_STRESS_FALL_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_FALL_EN		RW	0
6	DM_HI_FALL_EN		RW	0
5	DP_HI_FALL_EN		RW	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	MANU_FALL_EN		RW	0
0	ABNORMAL_STRESS_ FALL_EN		RW	0

Table 4-69. OTHER_INT_STS

Address Offset	0x8C		
Physical Address	0x0000 008C	**Instance**	USB_SCUSB
Description	Indicates the current value of the interrupt source signal		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
VB_SESS_VLD	DM_HI	DP_HI	Reserved			MANU	ABNORMAL_STRESS

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD	Same as VB_SESS_VLD pin	R	0
6	DM_HI	Same as DM_HI pin	R	0
5	DP_HI	Same as DP_HI pin	R	0
4	Reserved		R	0
3	Reserved	Asserted when the BDIS_ACON bit in the OTHER_INT_LATCH register is set.	R	0
2	Reserved		R	0
1	MANU	Same as the MANU pin	R	0
0	ABNORMAL_STRESS_ FALL_EN	An abnormal condition caused the short withstand protection circuit to be activated. This can be caused by the attachment of a defective cable or a defective device.	R	0

Table 4-70. OTHER_INT_LATCH

Address Offset	0x8D		
Physical Address	0x0000 008D	**Instance**	USB_SCUSB
Description	These bits are set by the PHY when an unmasked specific event occurs. The PHY automatically clears all bits when the link reads this register, or when the low-power mode is entered. **Note:** If register read data is returned to the link in the same cycle that an OTHER_INT_LATCH bit is to be set, the interrupt condition is given immediately in the register read data, and the latch bit is not set.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
VB_SESS_VLD	DM_HI	DP_HI	Reserved			MANU_LATCH	ABNORMAL_STRESS_LATCH

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD	Set when VB_SESS_VLD changes level and the event is unmasked	RW	0
6	DM_HI	Set when DM_HI changes level and the event is unmasked	RW	0
5	DP_HI	Set when DP_HI changes level and the event is unmasked	RW	0
4	Reserved		RW	0
3	Reserved	Set when BDIS_ACON_EN is set, and transceiver asserts dp_pullup after detecting the B-device disconnect	RW	0
2	Reserved		RW	0
1	MANU_LATCH	Asserted if the MANU_RISE bit in the OTHER_INTERRUPT_ENABLE register is set, and the MANU input pin changes from low to high Also asserted if the MANU_FALL bit in the OTHER_INTERRUPT_ENABLE register is set, and the MANU input pin changes from high to low	RW	0
0	ABNORMAL_STRESS_ LATCH	Asserted if the ABNORMAL_STRESS bit in the OTHER_INTERRUPT_ENABLE register is set, and a stress condition has been detected (example, shorts)	RW	0

Table 4-71. ID_INT_EN_RISE

Address Offset	0x8E		
Physical Address	0x0000 008E	**Instance**	USB_SCUSB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				ID_RES_FLOAT	ID_RES_440K	ID_RES_200K	ID_RES_102K

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	ID_RES_FLOAT	If this bit is set, it generates an interrupt event notification when the ID_RES_FLOAT pin changes from low to high.	RW	0
2	ID_RES_440K	If this bit is set, it generates an interrupt event notification when the ID_RES_440K pin changes from low to high.	RW	0
1	ID_RES_200K	If this bit is set, it generates an interrupt event notification when the ID_RES_200K pin changes from low to high.	RW	0
0	ID_RES_102K	If this bit is set, it generates an interrupt event notification when the ID_RES_102K pin changes from low to high.	RW	0

Table 4-72. ID_INT_EN_RISE_SET

Address Offset	0x8F		
Physical Address	0x0000 008F	**Instance**	USB_SCUSB
Description	This register does not physically exist. This is the same as the ID_INT_EN_RISE register with the read/set-only property (writing 1 sets a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	0	
Reserved				ID_RES_FLOAT	ID_RES_440K	ID_RES_200K	ID_RES_102K

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	ID_RES_FLOAT		RW	0
2	ID_RES_440K		RW	0
1	ID_RES_200K		RW	0
0	ID_RES_102K		RW	0

Table 4-73. ID_INT_EN_RISE_CLR

Address Offset	0x90		
Physical Address	0x0000 0090	**Instance**	USB_SCUSB
Description	This register does not physically exist. This is the same as the ID_ENT_EN_RISE register with the read/clear-only property (writing 1 clears a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				ID_RES_FLOAT	ID_RES_440K	ID_RES_200K	ID_RES_102K

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	ID_RES_FLOAT		RW	0
2	ID_RES_440K		RW	0
1	ID_RES_200K		RW	0
0	ID_RES_102K		RW	0

Table 4-74. ID_INT_EN_FALL

Address Offset	0x91		
Physical Address	0x0000 0091	**Instance**	USB_SCUSB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from high to low.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				ID_RES_FLOAT	ID_RES_440K	ID_RES_200K	ID_RES_102K

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	ID_RES_FLOAT	If this bit is set, it generates an interrupt event notification when the ID_RES_FLOAT pin changes from high to low.	RW	0
2	ID_RES_440K	If this bit is set, it generates an interrupt event notification when the ID_RES_440K pin changes from high to low.	RW	0

Bits	Field Name	Description	Type	Reset
1	ID_RES_200K	If this bit is set, it generates an interrupt event notification when the ID_RES_200K pin changes from high to low.	RW	0
0	ID_RES_102K	If this bit is set, it generates an interrupt event notification when the ID_RES_102K pin changes from high to low.	RW	0

Table 4-75. ID_INT_EN_FALL_SET

Address Offset	0x92		
Physical Address	0x0000 0092	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the ID_INT_EN_FALL register with the read/set-only property (writing 1 sets a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				ID_RES_FLOAT	ID_RES_440K	ID_RES_200K	ID_RES_102K

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	ID_RES_FLOAT		RW	0
2	ID_RES_440K		RW	0
1	ID_RES_200K		RW	0
0	ID_RES_102K		RW	0

Table 4-76. ID_INT_EN_FALL_CLR

Address Offset	0x93		
Physical Address	0x0000 0093	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the ID_INT_EN_FALL register with the read/clear-only property (writing 1 clears a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				ID_RES_FLOAT	ID_RES_440K	ID_RES_200K	ID_RES_102K

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	ID_RES_FLOAT		RW	0
2	ID_RES_440K		RW	0
1	ID_RES_200K		RW	0
0	ID_RES_102K		RW	0

Table 4-77. ID_INT_STS

Address Offset	0x94		
Physical Address	0x0000 0094	**Instance**	USB_SCUSB
Description	Indicates the current value of the interrupt source signal		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				ID_RES_FLOAT	ID_RES_440K	ID_RES_200K	ID_RES_102K

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	ID_RES_FLOAT	Same as ID_RES_FLOAT pin	R	0
2	ID_RES_440K	Same as ID_RES_440K pin	R	0
1	ID_RES_200K	Same as ID_RES_200K pin	R	0
0	ID_RES_102K	Same as ID_RES_102K pin	R	0

Table 4-78. ID_INT_LATCH

Address Offset	0x95		
Physical Address	0x0000 0095	**Instance**	USB_SCUSB
Description	These bits are set by the PHY when an unmasked specific event occurs. The PHY automatically clears all bits when the link reads this register, or when the low-power mode is entered.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				ID_RES_FLOAT	ID_RES_440K	ID_RES_200K	ID_RES_102K

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	ID_RES_FLOAT	Set when ID_RES_FLOAT changes level and the event is unmasked	R	0
2	ID_RES_440K	Set when ID_RES_440K changes level and the event is unmasked	R	0
1	ID_RES_200K	Set when ID_RES_200K changes level and the event is unmasked	R	0
0	ID_RES_102K	Set when ID_RES_102K changes level and the event is unmasked	R	0

Table 4-79. CARKIT_SM_1_INT_EN

Address Offset	0x97		
Physical Address	0x0000 0097	**Instance**	USB_SCUSB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding interrupt event is activated in the carkit state-machine.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	PSM_ERROR_EN	PH_ACC_EN	CHARGER_EN	USB_HOST_EN	USB_OTG_B_EN	CARKIT_EN	DISCONNECTED_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	PSM_ERROR_EN	If this bit is set, it generates an interrupt event notification when entering PH_ERROR state in the hardware state-machine.	RW	0
5	PH_ACC_EN	If this bit is set, it generates an interrupt event notification when entering PH_PACC state in the hardware state-machine.	RW	0
4	CHARGER_EN	If this bit is set, it generates an interrupt event notification when entering PH_CHARGER state in the hardware state-machine.	RW	0
3	USB_HOST_EN	If this bit is set, it generates an interrupt event notification when entering PH_USB_HOST state in the hardware state-machine.	RW	0
2	USB_OTG_B_EN	If this bit is set, it generates an interrupt event notification when entering PH_USB_OTG_B state in the hardware state-machine.	RW	0
1	CARKIT_EN	If this bit is set, it generates an interrupt event notification when entering PH_UART or PH_USB_READY state in the hardware state-machine.	RW	0
0	DISCONNECTED_EN	If this bit is set, it generates an interrupt event notification when entering PH_DISC state in the hardware state-machine.	RW	0

Table 4-80. CARKIT_SM_1_INT_EN_SET

Address Offset	0x98		
Physical Address	0x0000 0098	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the CARKIT_SM_1_INT_EN register with the read/set-only property (writing 1 sets a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	PSM_ERROR_EN	PH_ACC_EN	CHARGER_EN	USB_HOST_EN	USB_OTG_B_EN	CARKIT_EN	DISCONNECTED_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	PSM_ERROR_EN		RW	0
5	PH_ACC_EN		RW	0
4	CHARGER_EN		RW	0
3	USB_HOST_EN		RW	0
2	USB_OTG_B_EN		RW	0
1	CARKIT_EN		RW	0
0	DISCONNECTED_EN		RW	0

Table 4-81. CARKIT_SM_1_INT_EN_CLR

Address Offset	0x99		
Physical Address	0x0000 0099	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the CARKIT_SM_1_INT_EN register with the read/clear-only property (writing 1 clears a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	PSM_ERROR_EN	PH_ACC_EN	CHARGER_EN	USB_HOST_EN	USB_OTG_B_EN	CARKIT_EN	DISCONNECTED_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	PSM_ERROR_EN		RW	0
5	PH_ACC_EN		RW	0
4	CHARGER_EN		RW	0

Bits	Field Name	Description	Type	Reset
3	USB_HOST_EN		RW	0
2	USB_OTG_B_EN		RW	0
1	CARKIT_EN		RW	0
0	DISCONNECTED_EN		RW	0

Table 4-82. CARKIT_SM_1_INT_STS

Address Offset	0x9A		
Physical Address	0x0000 009A	**Instance**	USB_SCUSB
Description	Indicates the current value of the interrupt source signal from the carkit hardware state-machine		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	PSM_ERROR	PH_ACC	CHARGER	USB_HOST	USB_OTG_B	CARKIT	DISCONNECTED

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	PSM_ERROR	Active high when psm_error interrupt source signal is valid	R	0
5	PH_ACC	Active high when ph_acc interrupt source signal is valid	R	0
4	CHARGER	Active high when charger interrupt source signal is valid	R	0
3	USB_HOST	Active high when usb_host interrupt source signal is valid	R	0
2	USB_OTG_B	Active high when usb_otg_b interrupt source signal is valid	R	0
1	CARKIT	Active high when carkit interrupt source signal is valid	R	0
0	DISCONNECTED	Active high when disconnected interrupt source signal is valid	R	0

Table 4-83. CARKIT_SM_1_INT_LATCH

Address Offset	0x9B		
Physical Address	0x0000 009B	**Instance**	USB_SCUSB
Description	These bits are set when an unmasked carkit state-machine event occurs. All set bits are automatically cleared when the link reads this register, or when low-power mode is entered.		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	PSM_ERROR_LATCH	PH_ACC_LATCH	CHARGER_LATCH	USB_HOST_LATCH	USB_OTG_B_LATCH	CARKIT_LATCH	DISCONNECTED_LATCH

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	PSM_ERROR_LATCH	Set when entering PH_ERROR in the hardware state-machine and the event is unmasked	R	0
5	PH_ACC_LATCH	Set when entering PH_PACC in the hardware state-machine and the event is unmasked	R	0
4	CHARGER_LATCH	Set when entering PH_CHARGER in the hardware state-machine and the event is unmasked	R	0
3	USB_HOST_LATCH	Set when entering PH_USB_HOST in the hardware state-machine and the event is unmasked	R	0
2	USB_OTG_B_LATCH	Set when entering PH_USB_OTG_B in the hardware state-machine and the event is unmasked	R	0
1	CARKIT_LATCH	Set when entering PH_UART or PH_USB_READY in the hardware state-machine and the event is unmasked	R	0
0	DISCONNECTED_LATCH	Set when entering PH_DISC in the hardware state-machine and the event is unmasked	R	0

Table 4-84. CARKIT_SM_2_INT_EN

Address Offset	0x9C		
Physical Address	0x0000 009C	**Instance**	USB_SCUSB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding interrupt event is activated in the carkit state-machine.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
STOP_PLS_MISS_EN	Reserved			STEREO_TO_MONO_EN	Reserved	PHONE_UART_EN	PH_NO_ACK_EN

Bits	Field Name	Description	Type	Reset
7	STOP_PLS_MISS_EN	If this bit is set, it generates an interrupt event notification when in DDA mode and the pulse is not received successfully.	RW	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	STEREO_TO_MONO_EN	If this bit is set, it generates an interrupt event notification when entering PH_AUD_MOVE_INT_4W state in the hardware state-machine.	RW	0
2	Reserved		R	0
1	PHONE_UART_EN	If this bit is set, it generates an interrupt event notification when entering PH_PHONE_INT_4W or PH_PHONE_INT_5W state in the hardware state-machine.	RW	0
0	PH_NO_ACK_EN	If this bit is set, it generates an interrupt event notification when entering PH_NO_ACK_5W state in the hardware state-machine.	RW	0

Table 4-85. CARKIT_SM_2_INT_EN_SET

Address Offset	0x9D		
Physical Address	0x0000 009D	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the CARKIT_SM_2_INT_EN register with the read/set-only property (writing 1 sets a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
STOP_PLS_MISS_EN	Reserved			STEREO_TO_MONO_EN	Reserved	PHONE_UART_EN	PH_NO_ACK_EN

Bits	Field Name	Description	Type	Reset
7	STOP_PLS_MISS_EN		RW	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	STEREO_TO_MONO_EN		RW	0
2	Reserved		R	0
1	PHONE_UART_EN		RW	0
0	PH_NO_ACK_EN		RW	0

Table 4-86. CARKIT_SM_2_INT_EN_CLR

Address Offset	0x9E		
Physical Address	0x0000 009E	**Instance**	USB_SCUSB
Description	This register does not physically exist. It is the same as the CARKIT_SM_2_INT_EN register with the read/clear-only property (writing 1 clears a particular bit; writing 0 has no effect).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
STOP_PLS_MISS_EN	Reserved			STEREO_TO_MONO_EN	Reserved	PHONE_UART_EN	PH_NO_ACK_EN

Bits	Field Name	Description	Type	Reset
7	STOP_PLS_MISS_EN		RW	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	STEREO_TO_MONO_EN		RW	0
2	Reserved		R	0
1	PHONE_UART_EN		RW	0
0	PH_NO_ACK_EN		RW	0

Table 4-87. CARKIT_SM_2_INT_STS

Address Offset	0x9F		
Physical Address	0x0000 009F	**Instance**	USB_SCUSB
Description	Indicates the current value of the interrupt source signal from the carkit hardware state-machine		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
STOP_PLS_MISS	Reserved			STEREO_TO_MONO	Reserved	PHONE_UART	PH_NO_ACK

Bits	Field Name	Description	Type	Reset
7	STOP_PLS_MISS	Active high when the stop_pls_miss interrupt source signal is valid	R	0
6	Reserved		RW	0
5	Reserved		RW	0
4	Reserved		R	0
3	STEREO_TO_MONO	Active high when the stereo_to_mono interrupt source signal is valid	R	0
2	Reserved		R	0
1	PHONE_UART	Active high when the phone_uart interrupt source signal is valid	R	0
0	PH_NO_ACK	Active high when the ph_no_ack interrupt source signal is valid	R	0

Table 4-88. CARKIT_SM_2_INT_LATCH

Address Offset	0xA0		
Physical Address	0x0000 00A0	**Instance**	USB_SCUSB
Description	These bits are set when an unmasked carkit state-machine event occurs. All set bits are automatically cleared when the link reads this register, or when low-power mode is entered.		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
STOP_PLS_MISS	Reserved			STEREO_TO_MONO	Reserved	PHONE_UART	PH_NO_ACK

Bits	Field Name	Description	Type	Reset
7	STOP_PLS_MISS	Set when in DDA mode and the pulse is not received successfully and the event is unmasked	R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	STEREO_TO_MONO	Set when entering PH_AUD_MOVE_INT_4W in the hardware state-machine and the event is unmasked	R	0
2	Reserved		R	0
1	PHONE_UART	Set when entering PH_PHONE_INT_4W or PH_PHONE_INT_5W in the hardware state-machine and the event is unmasked	R	0
0	PH_NO_ACK	Set when entering PH_NO_ACK_5W in the hardware state-machine and the event is unmasked	R	0

Resets and Power Management

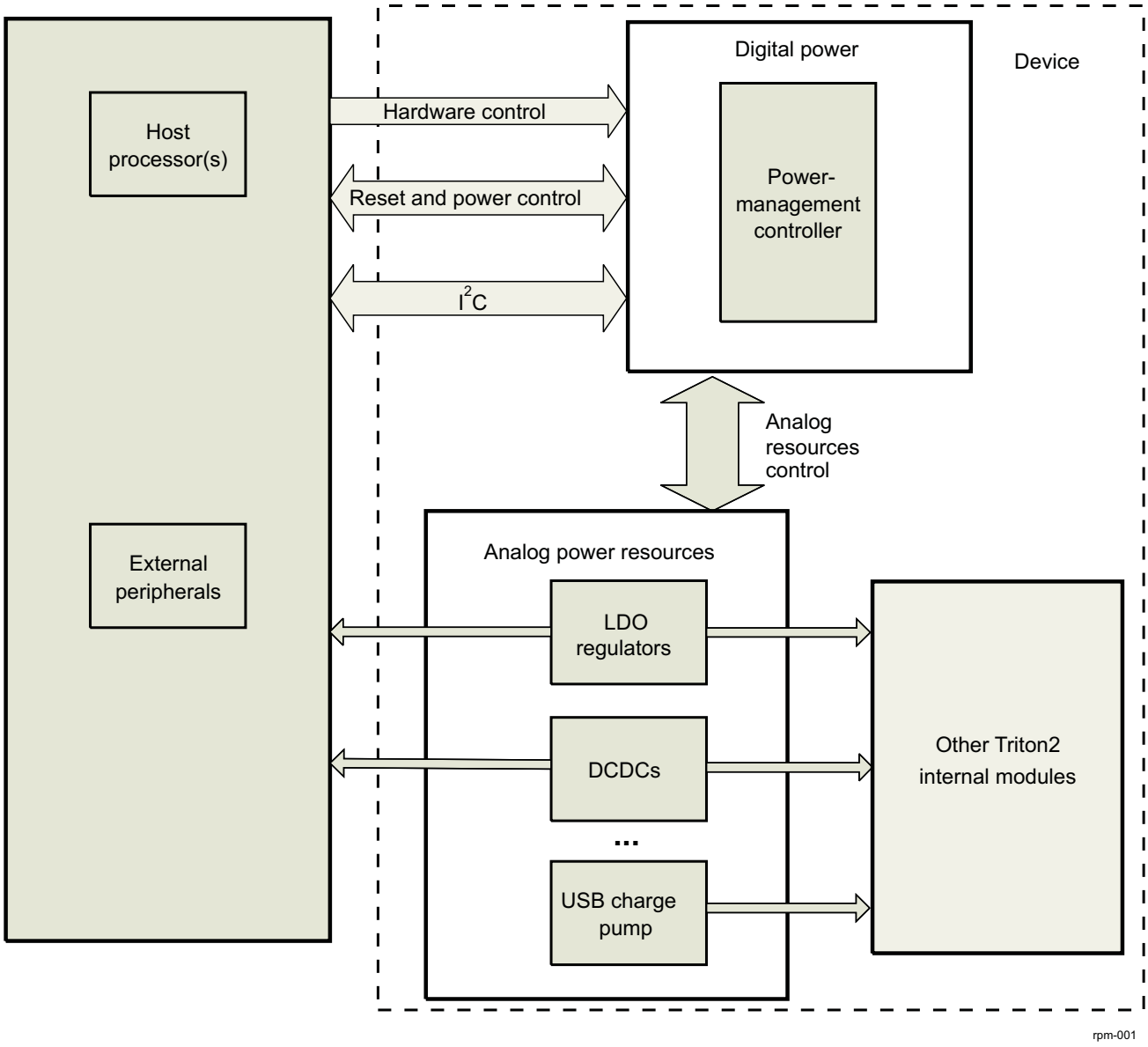
This chapter describes the power-management system of the device and the protocol for communicating with the power-management system.

Topic **Page**

5.1 Resets and Power-Management Overview

This chapter provides the details of the protocol required to interface with the PWR_SC module in the device. Figure 5-1 is the top-level block diagram for the device power-management system.

Figure 5-1. Device Power-Management System



The power-management system (digital module) has the following features:

- 21 shared power resources available to the device internal and external resources
- Resource grouping based on applications
- SmartReflex™-compliant dynamic voltage management for processor core
- Management of all power and reset functions
- Software control of power resources using configurable registers
- Reduction in leakage by reduction of capability to deliver power
- Backup registers and secured registers
- Master and slave operating modes
- Two linear regulator supplies for peripherals
- Two low dropouts (LDOs) for phase-locked loops (PLLs) and a digital-to-analog converter (DAC)

5.2 Resets and Power-Management Environment

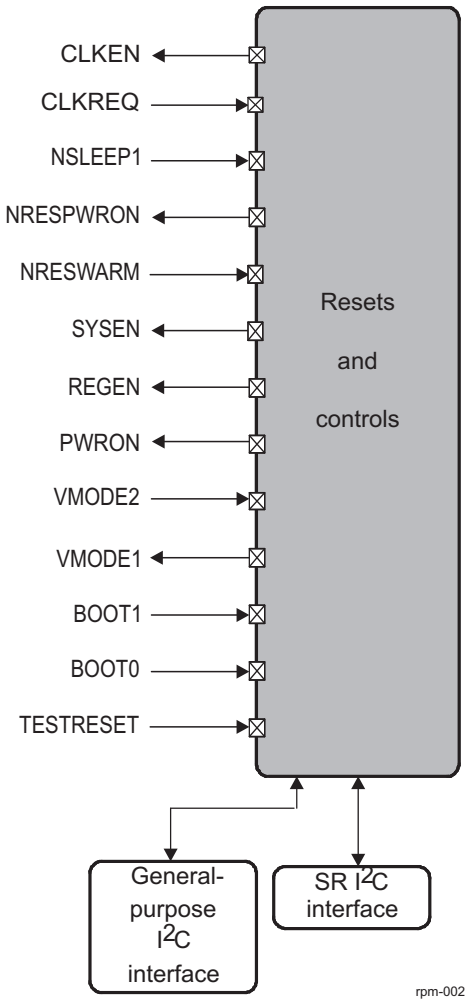
The device system consists of three processor groups, each associated with specific functionality for power management. These are categorized as processor[n] groups (n = 1, 2, or 3); each group contributes resources to integrate specific functionality:

- The processor1 (P1) group contains application devices, with all devices contributing to integrate main application functionality (OMAP™).
- The processor2 (P2) group contains modem devices, with all devices contributing to integrate modem subsystem functionality.
- The processor3 (P3) group contains peripherals, with all other devices implementing specific applications.

5.2.1 Control and Reset External Interface

Figure 5-2 shows the reset and control signals to the device. The general-purpose (GP) inter-integrated circuit (I^2C™) and SmartReflex I^2C bus interfaces provide read/write access to the registers.

Figure 5-2. Device Reset and Control Block



5.2.1.1 TESTRESET

The TESTRESET pin is tied low by internal connections.

5.2.1.2 BOOT0 and BOOT1

The BOOT0 and BOOT1 pins configure the device in master or slave mode. These pins also select the process mode (C021 or C027). Mode configuration settings are listed in Table 5-2. Slave boot mode is dedicated to OMAP34XX; external adaptation is required for OMAP2430.

NOTE: C027 is a reference to OMAP2430 and C021 is a reference to OMAP34XX.

5.2.1.3 VMODE1 and VMODE2

The VMODE1 and VMODE2 pins are used for the voltage-scaling feature of the device. Voltage scaling starts on the VMODE rising-edge transition, causing the DC/DC voltage to go from VFLOOR to VROOF. When VMODE transitions on the falling edge, the DC/DC voltage goes from VROOF to VFLOOR. VMODE2 behaves the same as VMODE1. VMODE1 and VMODE2 are the digital voltage scaling linked with VDD1 and VDD2, respectively. See Section 5.4.10, *Dynamic Voltage Scaling Management*, for more voltage-scaling information.

5.2.1.4 PWRON

The PWRON signal is activated by a push-button when the device is in master mode. In master mode, the voltage on this input is the battery voltage. The PWRON signal can also be driven by a digital signal when the device boots up in slave mode. In slave mode, PWRON pulls low when VBAT rises, and PWRON must be pulled down by an external pulldown on this pad.

5.2.1.5 REGEN

REGEN is an output of the device connected to slave power integrated circuits (ICs) or external LDOs that power on before input offset voltage (VIO). This pad has an open drain that can be enabled and disabled using the REGEN_PU_DISABLE register. In the power-on sequence, REGEN comes before VIO.

5.2.1.6 SYSEN

SYSEN is a bidirectional signal of the device that controls slave power ICs. All power ICs should have an open drain connected to this line. In master mode, the device sets SYSEN high to enable the slave power ICs. In slave mode, when one of the power ICs drives SYSEN low, all devices of the platform stay in WAIT-ON state. For information about device states, see Section 5.4.1, *System States*.

5.2.1.7 nRESWARM

nRESWARM is an active low input reset signal to the device. Depending on the application, this signal can be connected to a reset button, an RC cell, or the warm reset output of an application processor.

For more information about warm reset, see Section 5.3.2.1, *Resets*.

5.2.1.8 nRESPWRON

The nRESPWRON output signal is the reset signal delivered to the host processor at power-on reset (POR) when the voltage core and input/output (I/O) are correctly set up.

5.2.1.9 nSLEEP1

nSLEEP1 is an input to the device. nSLEEP1 controls all the power resources owned by P1. Power resources are associated with P1 by register configuration. The <resource name>_DEV_GRP register can be configured; for example, if the VAUX1_DEV_GRP[7:5] DEV_GRP bit field is set to 001, the VAUX1 resource is owned by P1.

When nSLEEPx is high, the power resource(s) owned by Px are out of SLEEP (they can deliver maximum power with the penalty of power resource leakage). When nSLEEPx is low, the power resource(s) owned by Px are in SLEEP, which reduces its leakage by reducing its capability to deliver power.

5.2.1.10 CLKREQ

CLKREQ is the peripheral clock request pin on the device. This is associated with P3. It can be configured to enable the clock signal or to control the LDOs and to enable the clock signal for the peripheral devices. By default, CLKREQ is disabled and no resources are associated.

5.2.1.11 CLKEN

CLKEN can control external devices.

Because CLKEN is a device resource, its state depends on the device group assignment (the CLKEN_DEV_GRP[7:5] DEV_GRP bit field). This signal is typically used to enable the clock provider for the system. For details about power resources, see Section 5.4.3, *Power-Management Controller*.

NOTE: By default, the CLKEN resource belongs to the P1, P2, and P3 device groups (the CLKEN_DEV_GRP[7:5] DEV_GRP bit field is set to 0x7). Its state depends on P1, P2, and P3 state transitions triggered by the associated hardware events. For more information about these hardware events, see Section 5.4.7, *Hardware Events for State Changes*.

Table 5-1 lists the reset and control signals and gives their default values where applicable.

5.2.1.11.1 Default Values for Reset and Control Signals

Table 5-1. Reset and Control Signals

Signal	I/O (1)	Default Value
PWRON	I	N/A
REGEN	O	0
SYSEN	O	0
nRESWARM	I	N/A
nRESPWRON	O	0
nSLEEP1	I	N/A
BOOT0	I	N/A
BOOT1	I	N/A
VMODE1	I	N/A
VMODE2	I	N/A
CLKREQ	I	N/A
CLKEN	O	1

(1) I = Input; O = Output

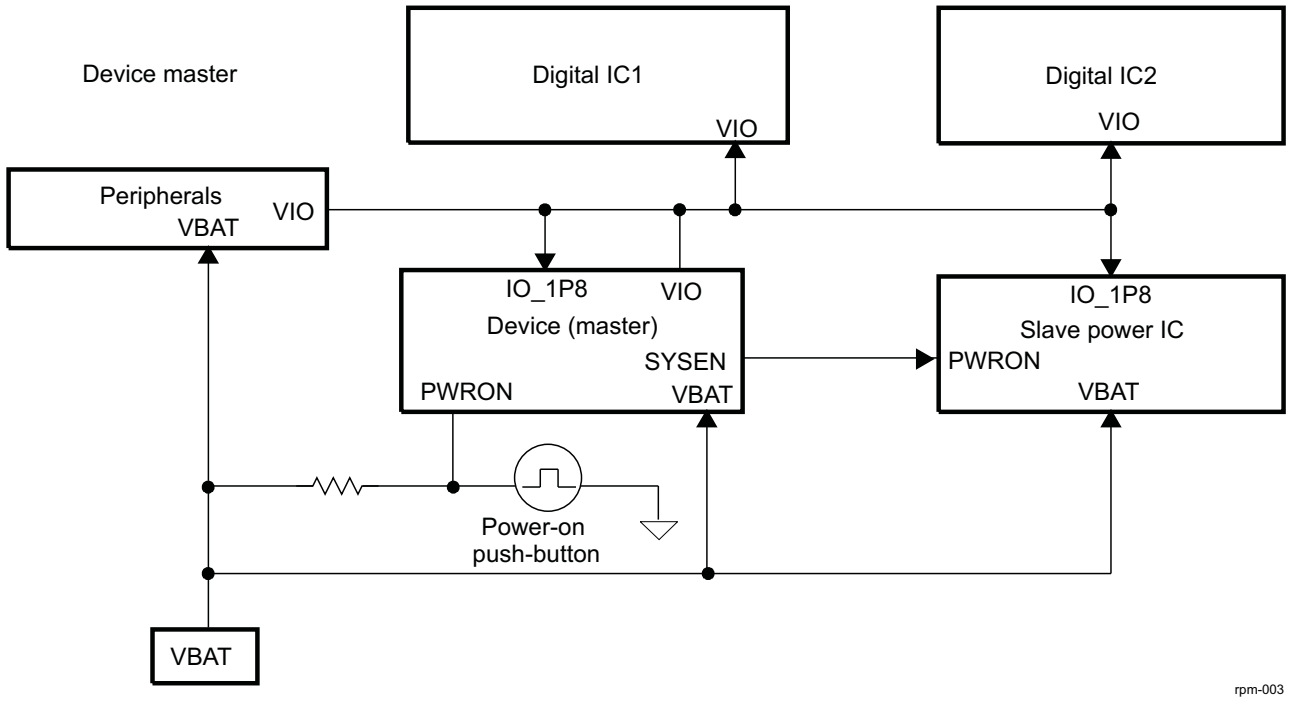
5.2.2 Device Connections to External ICs

The decision to boot the device in master or slave mode is based on how the device is configured with the rest of the chipset. Slave boot mode is dedicated to OMAP34XX; external adaptation is required for OMAP2430.

5.2.2.1 Master Mode

When in master mode, the device can be powered on with a power-on button (PWRON), and controls the other power ICs in the system. The slave power IC is controlled by the SYSEN signal from the master, as shown in Figure 5-3.

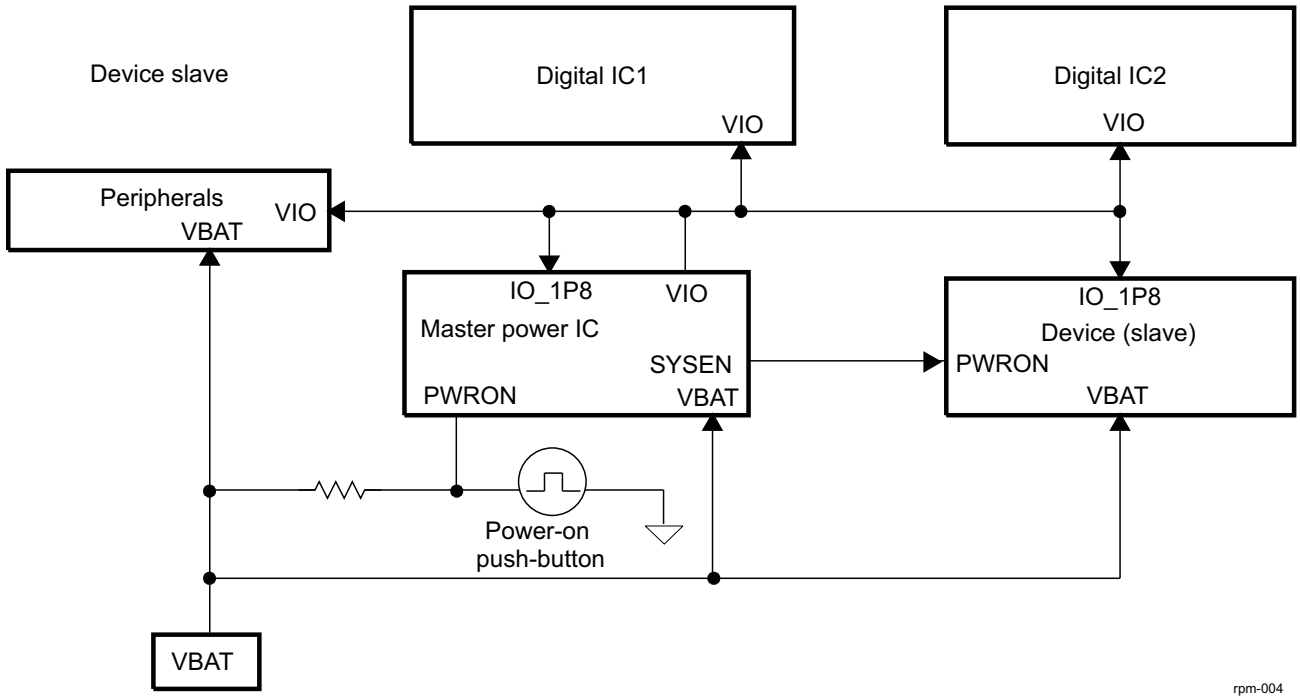
Figure 5-3. Master Mode Integration



5.2.2.2 Slave Mode

When in slave mode, the power IC is controlled by another device in the system with a digital signal on the PWRON input. Figure 5-4 shows an example of an application with the device as a slave to another power IC.

Figure 5-4. Slave Mode Integration



NOTE: SYSEN should be directly connected to PWRON for slave mode configuration if two TPS65930/20 parts are used.

5.3 Reset and Power-Management Integration

This section shows different boot modes for the the device. Boot mode selection determines whether the device is configured in master or slave mode. The boot core voltage and the power-up sequence are different for each mode.

5.3.1 Boot Modes

The device can be configured in master or slave mode, as shown in Figure 5-3 and Figure 5-4. Mode settings are configurable using the boot pins on the device. The boot pins are input to the device, as seen in Table 5-2. In master mode, the device powers up using the PWRON push-button and controls the other power ICs with SYSEN and REGEN (REGEN is one of the power resources available in the device). In slave mode, the device is controlled by another power IC with a digital signal on PWRON.

The modes corresponding to the BOOT0-BOOT1 combination values are listed in Table 5-2. Slave boot mode is dedicated to OMAP34XX; external adaptation is required for OMAP2430.

Table 5-2. Boot Modes

Mode	BOOT0	BOOT1	Boot Core Voltage
Master_C027 (MC027S)	0	0	1.3 V
Master_C027 (MC027)	0	1	1.3 V
Master_C021 (MC021)	1	0	1.2 V
Slave_C021 (SC021)	1	1	1.2 V

Register Bit	On	Off
STARTON_VBAT (master mode only)(1)	1 (default)	0
STARTON_VBUS (master mode only)(1)	1 (default)	0

(1) C027 is a reference to the OMAP2430 processor and C021 is a reference to the OMAP34XX processor.

In master mode, when the STARTON_VBAT bit is set to ON (1), if a main battery is inserted with voltage greater than the $VBAT_{min}$ high threshold, the device starts the transition sequence to ACTIVE state. When the STARTON_VBAT bit is set to OFF (0), the device does not start on battery insertion. The STARTON_VBAT bit is 1 by default, so after the first battery insertion, the device starts automatically. In slave mode, this bit has no effect.

In master mode, when the STARTON_VBUS bit is set to ON (1), if VBUS voltage is detected, the device starts the sequence to transition to ACTIVE state on VBUS detection. When the STARTON_VBUS bit is set to OFF (0), the device does not start on VBUS detection. The STARTON_VBUS bit is 1 by default, so after the first battery insertion, the user must clear this bit to prevent the device from starting on VBUS detection. In slave mode, this bit has no effect.

5.3.2 Resets and Power Management

5.3.2.1 Resets

- POR: Caused by a low battery. The device also resets itself, including the backup domain registers (except the reset management that generates the reset), when the battery is removed within 8 seconds after PWRON is pressed for more than 8 seconds and then released. This is not only a manual reset, but also a switch-off of the device.

  Pressing PWRON for 8 seconds without removing the battery also restarts the device (even if the backup registers are not reset).

NOTE: When PWRON is pressed for 8 seconds and the battery is not removed, all the registers in the VBAT domain except SC_CONFIG, SC_DETECT1, SC_DETECT2, WATCHDOG_CFG, and IT_CHECK_CFG are reset, and the registers in the backup domain are reset only when the battery is removed after pressing the PWRON key for 8 seconds.

NOTE: When the STS_BOOT[3] PWRON_8s bit is set to 1, a restart has occurred after a PWRON low for more than 8 seconds.

- Warm reset: The device can be configured to perform a warm reset of the system to bring the system to a known defined state. The device detects a request for a warm reset on the nRESWARM pin. The SmartReflex I^2C accesses are canceled. The minimum duration of the pulse on the nRESWARM pin is two 32-kHz clock cycles.

  A warm-reset sequence can be programmed in device spare memory spaces by writing to the MEMORY_DATA and MEMORY_ADDRESS registers. The starting address of this sequence can then be programmed in the SEQ_ADD_WARM register. For more information about how to program device power-management sequences, see Section 5.5.3, *Programming Example for Skipping an Address*. When the nRESWARM signal is detected, the sequence preprogrammed in memory is executed.

  Based on system requirements, a warm-reset sequence can be programmed to reset some device modules and bring device resources to a known defined state. Table 5-3 describes a sample warm-reset sequence.

Table 5-3. Sample Warm Reset Sequence

Steps	RES_ID	RES_GRP	RES_Type 2	Device Resources Allocated	Resource State	Delay (in 32-kHz clock)
0	27	X	0	Triton reset	OFF	2
1	X	All	1	Enable CLKEN, VINTANA1, VINTDIG, and VINTANA2	ACTIVE	14
2	X	PP	2	Enable PP VAUX2	WARMRESET	14
3	X	PP	3	Disable PP VDAC and VMMC1	OFF	14
4	15	X	0	Enable PP VDD1	WARMRESET	14
5	16	X	0	Enable PP VDD2	WARMRESET	14
6	7	X	0	Enable PP VPLL1	WARMRESET	96
7	25	X	0	Enable HFCLKOUT	ACTIVE	2
8	27	X	0	Released Triton reset	ACTIVE	2

The resources can be programmed using singular messages (to individual power sources) or broadcast messages (to all power sources). In Table 5-3, X indicates a don't care value because the resources can be referred to the resource ID or the resource group. Refer to Table 5-8 for details on resource IDs, default resource groups and default resource types.

The warm-reset sequence described in Table 5-3 changes the TRITON_RESET resource to off mode at the beginning of the sequence, and then to on mode at the end of the sequence. This change in state of TRITON_RESET resets all the digital logic in the device, except for some in the PWR subchip. For details about the effect of this reset, see Table 5-4.

NOTE: If a warm-reset sequence toggles the TRITON_RESET resource, the host processor must reinitialize the value of bits that are reset, returning them to their default values.

When a warm reset signal is detected, the sequence is executed for the resources assigned to the device group for which a warm reset was enabled. The warm reset for device groups can be enabled by setting the ENABLE_WARMRESET bit of the Px_SW_EVENTS (x = 1, 2, 3) register to 1. When this bit is set to 0, there is no effect of warm reset on the resources assigned to that device group.

The sample warm-reset sequence affects the state of some resources listed in Table 5-3. The power bus messages can be programmed so that the resources go to the WAIT-ON (0000), ACTIVE (1110), SLEEP (1000), or WARMRESET (1111) states. The resource states (operating modes) are listed in Table 5-5. When the requested state of the resource is WARMRESET, the output voltage of that resource (LDOs and switched mode power supplies [SMPS]) is set to its default reset value, and the device group (DEV_GRP) is changed depending on the WARM_CFG bit of the same register. If the WARM_CFG bit is set to 1, the DEV_GRP of that resource is set to 111 when the resource is requested to undergo WARMRESET. If the WARM_CFG bit is 0, there is no effect of warm reset on the resource device group. At the end of the warm reset, the resource is in ACTIVE state.

The warm-reset sequence is programmed by writing to the spare memory words in the device.

For more information about the format of spare memory words, see Table 5-25 andSection 5.5.4,

Programming Example for Adding a Delay. The sequence can be a broadcast message or a singular message. For the message format, see Section 5.4.3.1, *Power Bus Message Format*.

Table 5-3 specifies the power resource that is to undergo warm reset and the state of the resource after warm reset. The table also shows the resource ID, group, and type, where applicable, for the resource. The Delay column specifies the delay before executing the next command in the sequence when a warm reset is executed.

To program a warm reset:

1. Program the warm-reset sequence using the MEMORY_ADDRESS and MEMORY_DATA registers.
2. Program the starting address of the warm-reset sequence in the SEQ_ADD_WARM register.
3. Program the <resource name>_DEV_GRP WARM_CFG bit if the DEV_GRP bit field of the resource is to be set to 111 after a warm reset on that resource.
4. Enable warm reset for device groups by writing to the ENABLE_WARMRESET bit of the Px_SW_EVENTS (x = 1, 2, 3) register.

- TRITON_RESET: This is not a global reset. This reset occurs when the TRITON_RESET resource is turned off and then on again by the TRITON_RESET configurable registers. When this reset occurs, the device resets some bits to their default values (see Table 5-4). These bits must have the desired values rewritten to them after the reset.

  Table 5-4 lists the bits that reset the default values during warm reset.

Table 5-4. Register Bits That Reset to Default Values During Warm Reset

Register	Bit(s)	Field Name	Reset
P1_SW_EVENTS	3	LVL_WAKEUP	0
P2_SW_EVENTS	3	LVL_WAKEUP	0
P3_SW_EVENTS	3	LVL_WAKEUP	0
PB_WORD_MSB	7:0	PB_WORD_MSB	0xFF
PB_WORD_LSB	7:0	PB_WORD_LSB	0xFF
MEMORY_ADDRESS	7:0	ADDRESS	0x00
SC_CONFIG	7	ENABLE	0
SC_CONFIG	6	MODE	0
SC_CONFIG	5	AUTOCUT	0
SC_CONFIG	4:0	TEN_SEL	0x00
WATCHDOG_CFG	4:0	WATCHDOG	0x00
IT_CHECK_CFG	2:1	IT_CHECK_DELAY	0x0
IT_CHECK_CFG	0	ITCHECK_ENABLE	0
VIBRATOR_CFG	3	VIB_CFG	0
VIBRATOR_CFG	2	VIB_PWM	0
VIBRATOR_CFG	1:0	VIB_DSEL	0x00
VDD1_VMODE_CFG	2	DCDC_SLP	0
VDD1_VMODE_CFG	1	READ_REG	0
VDD1_VMODE_CFG	0	ENABLE_VMODE	0
VDD2_VMODE_CFG	2	DCDC_SLP	0
VDD2_VMODE_CFG	1	READ_REG	0
VDD2_VMODE_CFG	0	ENABLE_VMODE	0

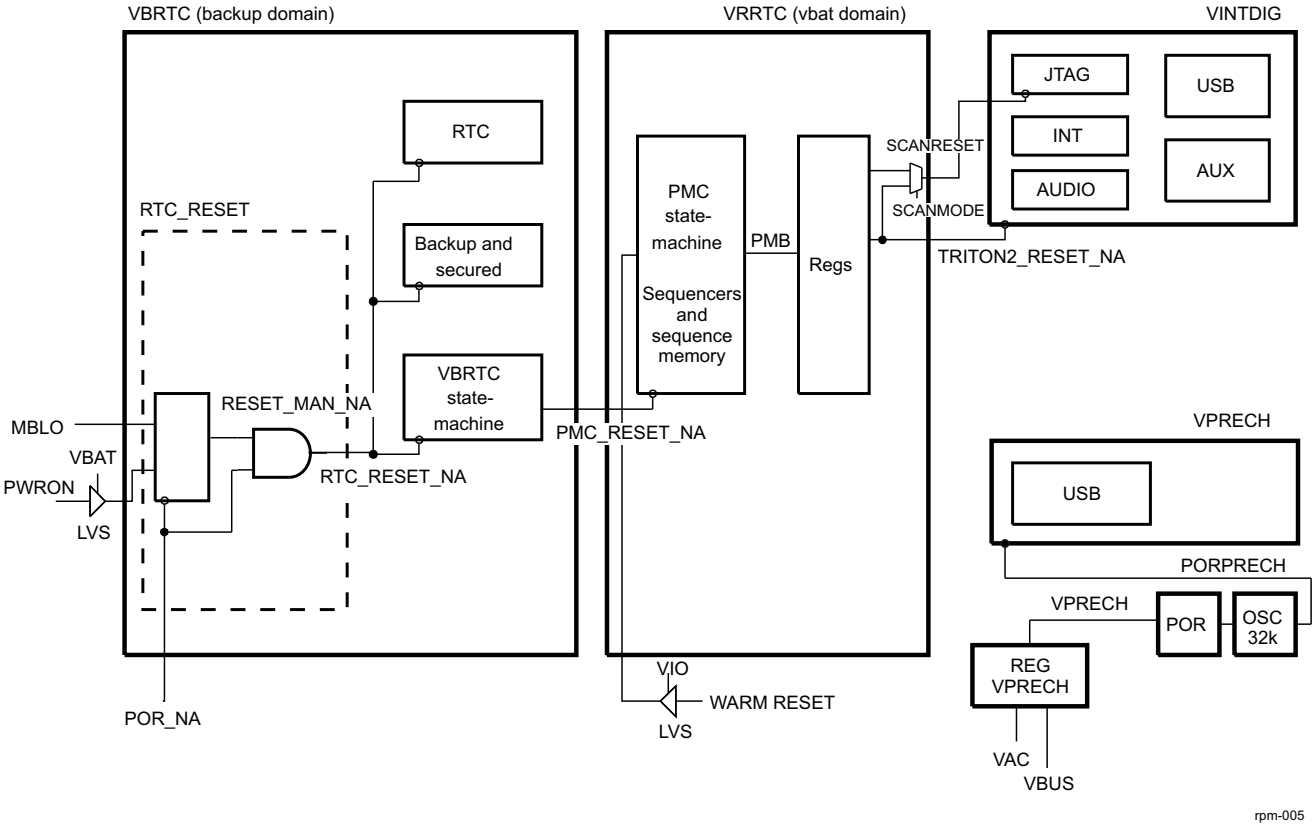
- PMC_RESET: This is caused by either of two conditions:
  - Battery voltage goes below 2.7 V.
  - A thermal shutdown occurs.

This resets all power-management blocks except the backup domain. In the preceding cases, the device goes to backup mode to save backup register values and to store and update time information.

5.3.2.2 Device Reset Tree

Figure 5-5 shows the reset tree for the device.

Figure 5-5. Device Reset Tree



VBRTC is the backup power domain and is on in backup, wait-on, and active modes. The VBRTC state-machine sends a reset signal to the program memory controller (PMC) state-machine. The PMC block is powered on by the VRRTC power resource. The VRRTC power resource is on in wait-on and active modes. When the device is in WAIT-ON state and receives a reset signal from the VBRTC state-machine, the PMC state-machine is activated. The PMC state-machine controls the analog and digital resources through the configurable registers. The VINTDIG power resource is on in active mode.

5.3.2.3 Power Management

To save power, the device can be configured in different modes for different regulators. All the power resources are listed in Table 5-8. The following subsections describe the operating modes available for the power resources.

5.3.2.3.1 Voltage Regulator Operating Modes (All Types Except USB)

The voltage regulators have three operating modes to optimize mean power consumption:

- Off mode: The output voltage is not maintained and voltage regulator power consumption is 0.
- On mode: The regulator can deliver its nominal output voltage with full-load current capability.
- Sleep mode: The nominal output voltage is maintained with very low power consumption but with low-load current capability.

5.3.2.3.2 LDO USB1V5 and USB1V8 Operating Modes

- Off mode: An internal signal drives the LDO to its DISABLED state. This resource can also be configured to stay enabled when an OFF command is issued.
- Sleep mode: An internal signal drives the LDO to its ACTIVE state by default. This resource can also

be configured to stay disabled when a SLEEP command is issued.

- Enabled mode: An internal signal drives the LDO to its ENABLED state.

5.3.2.3.3 LDO USB3V1 Operating Modes

- Off mode: The LDO is in DISABLED state. This resource can also be configured to stay enabled or in sleep mode when an OFF command is issued.
- Sleep mode: The LDO is in SLEEP state by default. This resource can also be configured to stay disabled or in active mode when a SLEEP command is issued.
- Enabled mode: The LDO is in SLEEP state by default. This resource can also be configured to stay disabled or in active mode when a SLEEP command is issued.

5.3.2.3.4 DC/DC Operating Modes

- Off mode: The output voltage is not maintained; DC/DC power consumption is 0.
- Active mode: DC/DC delivers its nominal output voltage with a full-load current capability.
- Sleep mode: The nominal output voltage is maintained with low-power consumption, but with low-load current capability.

A common local oscillator is implemented for all DC/DC. DC/DC output voltage can be controlled by the SmartReflex high-speed I^2C.

5.3.2.3.5 Main Power Reference Operating Modes

- On mode: The bandgap can deliver accurate nominal reference voltage.
- Sleep mode: A lower-than-nominal output voltage is maintained with very low power consumption, but with low-load current capability.

5.3.2.3.6 REGEN, SYSEN, nRESPWRON, 32KCLKOUT, and TRITON_RESET Digital Signal Operating Modes

- Active mode: The digital signal is forced to ACTIVE state.
- Sleep mode: The digital signal is forced to ACTIVE state.
- Off mode: The digital I/O signal is forced to DISABLED state.

5.3.2.3.7 HFCLKOUT CLKEN Digital Signal Operating Modes

Active mode: The digital signal is forced to ACTIVE state.

Sleep mode: The digital signal is forced to DISABLED state.

Off mode: The digital I/O signal is forced to DISABLED state.

5.3.3 Resource Operating Modes

Table 5-5 lists the operating modes for the available resources. The left-hand column shows the binary value of the field used to set a resource to the desired state. The values to change the resource state can be written in the OFF_STATE or SLEEP_STATE bit field of the <resource name>_ REMAP register.

Table 5-5. Operating Modes

Resource State	LDOs	DC/DC	MAIN_PR	Digital Signal
1111(15) WARMRESET	WARM RESET	WARM RESET	ACTIVE	WARM RESET
1110(14) ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1101(13)	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1100(12)	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1011(11)	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1010(10)	ACTIVE	ACTIVE	ACTIVE	ACTIVE

Table 5-5. Operating Modes (continued)

Resource State	LDOs	DC/DC	MAIN_PR	Digital Signal
1001(9)	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1000(8) SLEEP	SLEEP	SLEEP	ACTIVE	SLEEP
0111(7)	SLEEP	SLEEP	ACTIVE	SLEEP
0110(6)	SLEEP	SLEEP	ACTIVE	SLEEP
0101(5)	SLEEP	SLEEP	ACTIVE	SLEEP
0100(4)	SLEEP	SLEEP	ACTIVE	SLEEP
0011(3)	SLEEP	SLEEP	ACTIVE	SLEEP
0010(2)	SLEEP	SLEEP	ACTIVE	SLEEP
0001(1)	SLEEP	SLEEP	ACTIVE	SLEEP
0000(0) WAIT-ON	OFF	OFF	OFF	OFF

To keep backup register values and store and update time information, the device goes to backup mode when the battery voltage falls below 2.7 V. The MBLO signal from the analog resources indicates this transition to digital resources.

5.4 Reset and Power Management Functional Description

5.4.1 System States

The power-management system provides five system states for optimal power use by the system, as listed in Table 5-6.

Table 5-6. System States

System State	Description
NO SUPPLY	System is not powered by a battery.
BACKUP	System is powered only with backup battery and maintains only VBRTC supply.
WAIT-ON	Subsystem is powered by the main battery and maintains only VRRTC supply. It can accept switch-on requests.
ACTIVE	Subsystem is powered by the main battery, all supplies are enabled with full current capability, internal reset is released, and the associated processor is running.
SLEEP	The main battery powers the subsystem; selected supplies are enabled, but in low consumption mode; and the associated processor is in low-power mode.

NO SUPPLY and BACKUP are global states (they are the same for all processor groups). ACTIVE, WAIT-ON, and SLEEP are subsystem states (different processor groups can be in different states). Global system states are managed through dedicated hardware, while subsystem states are managed by a power-management state-machine.

5.4.1.1 System State Transitions

Three categories of events can trigger state transitions:

- Hardware events: Energy insertion, wake-up requests, charger, USB, and real-time clock (RTC)
- Software events: Switch-off commands, switch-on commands, and sleep-on commands
- Emergency events: Main battery removal, main battery fail, and thermal shutdown

Table 5-7 lists and describes the state transitions. Figure 5-6 is the state transition diagram.

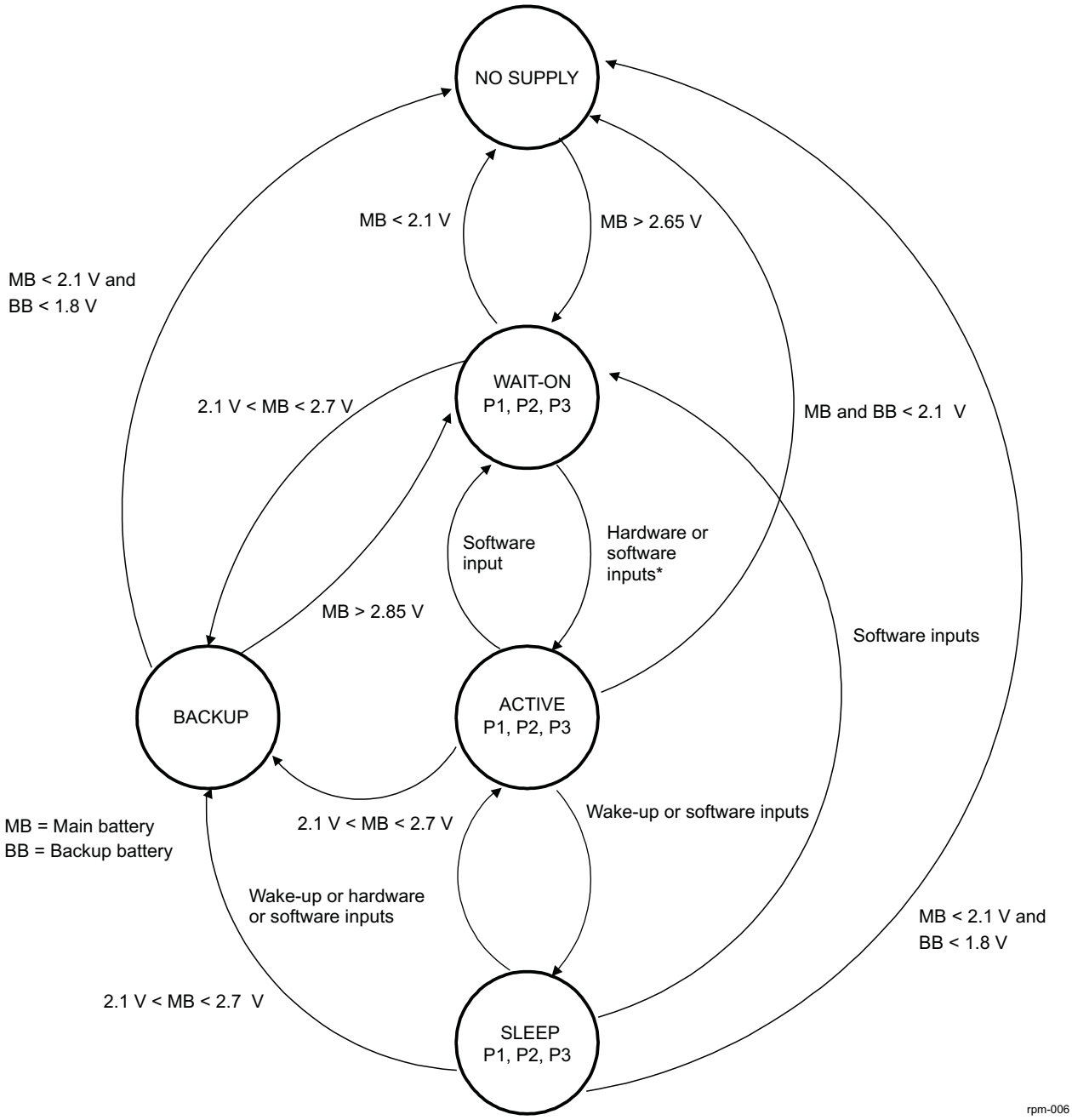
Table 5-7. State Transitions

Transition	Description
Power on	System is in NO SUPPLY state. Insertion of a valid main battery starts the transition to WAIT-ON state.

Table 5-7. State Transitions (continued)

Transition	Description
Power off	From any state, the system is subjected to a removal of all energy sources. This initiates a transition to NO SUPPLY state.
Switch on	System is in WAIT-ON state able to accept hardware switch-on conditions. This initiates a transition to ACTIVE state.
Switch off	System is powered and in ACTIVE or SLEEP state. A software condition can initiate a transition to WAIT-ON state.
SLEEP on	System is powered and in ACTIVE state. A hardware condition enabled by a register access initiates a transition to SLEEP state.
Sleep off	System is powered and in sleep mode. A hardware condition can initiate a transition to active mode.
BACKUP on	System is powered and in ACTIVE, SLEEP, or WAIT-ON state. The detection of a low main battery initiates the transition to BACKUP state.
BACKUP off	System is in BACKUP state. The detection of a main battery above 2.85 V initiates the transition to WAIT-ON state.
nRESWARM	System is powered and in ACTIVE or SLEEP state. When nRESWARM signal rises, it initiates a transition to set the device in a defined ACTIVE state.

Figure 5-6. State Transition Diagram



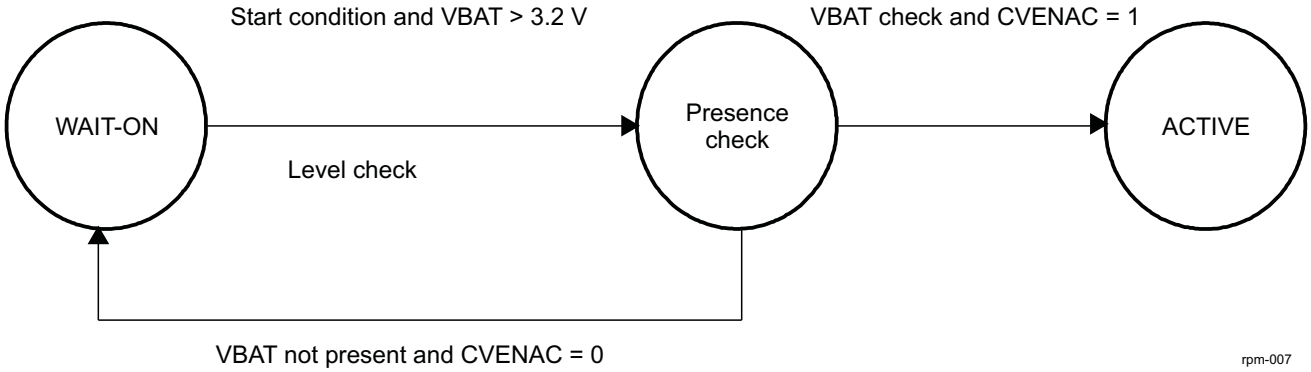
5.4.1.2 WAIT-ON-to-ACTIVE Transition

To implement the battery-level check and the battery-presence check, the transition from WAIT-ON state to ACTIVE state is split into two subsequences:

- WAIT-ON-to-presence check
- Presence check-to-ACTIVE

The base address of each sequence is stored in a register. WAIT-ON-to-battery-presence check is stored in the SEQ_ADD_W2P register, and battery-presence check-to-ACTIVE state is stored in the SEQ_ADD_P2A register. Figure 5-7 shows the WAIT-ON-to-ACTIVE transition.

Figure 5-7. State Transition: WAIT-ON to ACTIVE State



The memory address for these registers is as follows:

- SEQ_ADD_W2P has an address 0.
- SEQ_ADD_P2A has an address 4.

This can be seen in Table 5-37.

5.4.2 Power Resources

5.4.2.1 Shared Resources

In this device, power resources are shared to achieve an efficient power supply scheme while avoiding redundancy. Boot modes (MC027S, MC027, MC021, and SC021) define initial resource mapping. When a resource is assigned to one processor group, its state depends on the assigned processor group state. When a resource is assigned to more than one processor group, it is in the highest required state

The 21 power resources can be divided into analog resources and digital signals. The analog resources are the LDO regulators, DC/DC regulators, and analog references. The digital signals are the reset and clock signals. These resources are further categorized into resource groups called power references (PRs), power providers (PPs), and reset and control signals (RCs). For details, see Table 5-9.

After power-on reset (POR), power resources are shared as listed in Table 5-8. An x in the table indicates a power resource that is active at POR in the given mode.

Table 5-8. Power Resources

MAPPING	COMMON			MC021				MC027				MC027S				SC021			
T2 Resources	ID Static	GRP	TYP2	TYP1	DEV_GRP			TYP1	DEV_GRP			TYP1	DEV_GRP			TYP1	DEV_GRP		
					P3	P2	P1		P3	P2	P1		P3	P2	P1		P3	P2	P1
VAUX2	2	PP	0	0				0				4	x			0			
VMMC1	5	PP	0	0				0				0				0			
VPLL1	7	PP	0	3			x	0			x	0			x	3			x
VDAC	10	PP	0	0				0				0				0			
VINTANA1[1]	11	PP	0	1	x	x	x	1	x	x	x	1	x	x	x	1	x	x	x
VINTANA2[1]	12	PP	0	0	x	x	x	0	x	x	x	0	x	x	x	0	x	x	x
VINTDIG[1]	13	PP	0	1	x	x	x	1	x	x	x	1	x	x	x	1	x	x	x
VIO	14	PP	0	2	x	x	x	2	x	x	x	3	x	x	x	2	x	x	x
VDD1	15	PP	0	4			x	3			x	4			x	4			x
VDD2	16	PP	0	3			x	4		x		5		x		3			x
VUSB_1v5[1]	17	PP	0	0				0				0				0			
VUSB_1v8[1]	18	PP	0	0				0				0				0			
VUSB_3v1[1]	19	PP	0	0	x	x	x	0	x	x	x	0	x	x	x	0	x	x	x
REGEN	21	PP	0	2	x	x	x	2	x	x	x	2	x	x	x	2	x	x	x
nRESPWRON	22	RC	0	0	x	x	x	0	x	x	x	0	x	x	x	0	x	x	x
CLKEN	23	RC	0	3	x	x	x	5	x	x	x	5	x	x	x	3	x	x	x
SYSEN	24	RC	0	6	x	x	x	6	x	x	x	6	x	x	x	6	x	x	x
HFCLKOUT	25	RC	0	0	x	x	x	0	x	x	x	0	x	x	x	0	x	x	x
32KCLKOUT	26	RC	0	0	x	x	x	0	x	x	x	0	x	x	x	0	x	x	x
TRITON_ RESET[1]	27	RC	0	6	x	x	x	6	x	x	x	6	x	x	x	6	x	x	x
Main_Ref[1]	28	PR	0	0	x	x	x	0	x	x	x	0	x	x	x	0	x	x	x

(1) Device internal resource

Power Providers
Reset and Control
Power Reference

Resource mapping can be updated by register access. For example, unassigned resources can be assigned to a processor group by software by modifying the <resource>_DEV_GRP[7:5] DEV_GRP bit field.

5.4.2.2 External Power Resource

Table 5-9 lists the external power source for the device and indicates whether the power source is available only when the device is configured in master or slave mode.

Table 5-9. Primary Resources

Power Source	Mode (1)
Battery	M, S

(1) M = Master; S = Slave

5.4.2.3 Backup Resource

The backup power resource is the power source that maintains the RTC and minimum logic. This source is listed in Table 5-10.

Table 5-10. Backup Resource

Backup Source	Mode (1)
Battery	M, S

(1) M = Master; S = Slave

5.4.2.4 Event Definition

Table 5-11 through Table 5-15 list the triggering hardware events for the device. Each event is indicated in master mode or slave mode and with the corresponding state transitions. All states and state transitions are described in Section 5.4.1.1, *System State Transitions*.

5.4.2.4.1 Starting Events

Table 5-11 lists the events that put the device in ACTIVE state.

Table 5-11. Starting Events

Number	Starting Event	Mode (1)	State Transition
1	Battery insertion and STARTON_VBAT = 1	M	Switch ON
2	PWRON button pressed	M	Switch ON
3	PWRON digital signal high	S	Switch ON
4	RTC alarm	M	Switch ON
5	Back from stopping event 2 and 3	M	Switch ON
6	VBUS detection and STARTON_VBUS = 1	M	Switch ON

(1) M = Master; S = Slave

VBUS and USB levels are reset to 0 when VBAT is low. When recovering from a VBAT domain reset (for example, when changing from NO_BAT to VBAT > 3.2 V), if the starting condition levels are valid, the device starts (example: it starts if VBUS is already plugged in).

A main battery with more than 3.2 V potential puts the device in ACTIVE state.

The PWRON button, when pressed momentarily, causes the device to transition from WAIT-ON to ACTIVE state (if there is a valid VBAT). A long press of the PWRON button has a different effect (see Table 5-12).

When the device returns from thermal shutdown (when the temperature goes below the 160-degree threshold), the device goes to ACTIVE state. For the PMC to reset, the MSK_THERMAL_SHUTDOWN bit must be set to 0. The STS_BOOT[6] TS bit indicates whether a thermal shutdown occurred since the last reset.

5.4.2.4.2 Stopping Events

Table 5-12 lists the events that put the device in WAIT-ON state.

Table 5-12. Stopping Events

Number	Stopping Event	Mode (1)	State Transition
1	PWRON digital signal low	S	Switch OFF
2	Power-on button pressed 6 seconds (default) and interrupt not acknowledged (programmable 3, 4, 5, or 6 s)	M	Restart
3	Watchdog expires	M	Switch OFF
4	Temperature ≥ thermal shutdown level (150°C)	M	Switch OFF
5	Power-on button pressed 8 seconds	M	Restart

(1) M = Master; S = Slave

The watchdog is disabled by default (WATCHDOG_CFG WATCHDOG = 0x00). It is enabled by writing a nonzero value to the WATCHDOG bit field.

Stopping event 2 (power-on button pressed 6 seconds and interrupt not acknowledged) can be enabled by setting the IT_CHECK_CFG[0] ITCHECK_ENABLE bit to 0x1. Delay to acknowledge interrupt can be programmed through the IT_CHECK_CFG[2:1] IT_CHECK_DELAY bit field.

Stopping event 3 can occur when the watchdog is enabled; the host processor should write back a nonzero value before the watchdog decrements to 0. If the host processor software fails to write back a nonzero value to the WATCHDOG bit field before it reaches 0, the device resets and goes to WAIT-ON state. If the STARTON_SWBUG bit in the CFG_Px_TRANSITION (x = 1, 2, or 3) register is set to 1, the device automatically goes to ACTIVE state. If the STARTON_SWBUG bit is set to 0, the device remains in WAIT-ON state.

Stopping event 5 (power-on button pressed 8 seconds) can be enabled by setting the Px_SW_EVENTS[6] STOPON_PWRON bit (x = 1, 2, or 3) to 0x1. When the device receives the event 5 register, the registers, except for those in the backup domain, are reset and the device restarts.

5.4.2.4.3 Backup Events

No events put the TPS65930 and TPS65920 in BACKUP state, because these devices do not have access to a backup battery.

5.4.2.4.4 Shutdown Events

Table 5-13 lists the events that put the device in NO SUPPLY state.

Table 5-13. Shutdown Events

Shutdown Event	Mode (1)	State Transition
Battery < 2.1 V	M, S	Power OFF
PWRON pressed 8 s and battery < 2.7 V in the following 8 s	M	Power OFF

(1) M = Master; S = Slave

5.4.2.4.5 Partial OFF Events

Table 5-14 lists the events that put the device in sleep mode.

Table 5-14. Partial OFF Events

Partial OFF Event	Mode (1)	State Transition
nSLEEP1 goes low. CLKREQ goes low.	M, S	SLEEP → ON

(1) M = Master; S = Slave

When the system goes to SLEEP state from ACTIVE state, it executes the ACTIVE-to-SLEEP transition. For more information about the SLEEP→ON transition, see Section 5.4.9.2, *SLEEP → ON and SLEEP → OFF Transitions*.

5.4.2.4.6 Partial ON Events

Table 5-15 lists the events that put the device in active mode.

Table 5-15. Partial ON Events

Partial ON Event	Mode (1)	State Transition
nSLEEP1 comes back high. CLKREQ goes high.	M, S	SLEEP → OFF

(1) M = Master; S = Slave

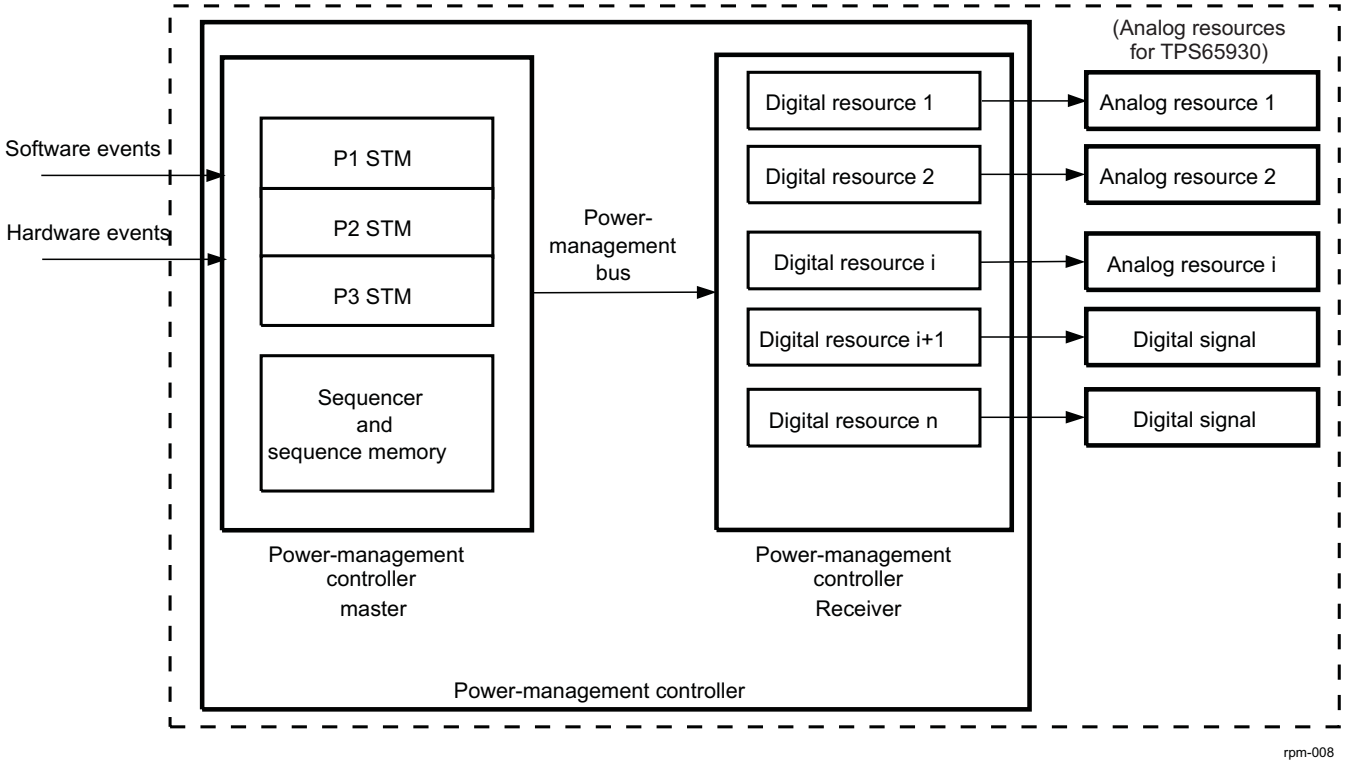
When the system goes to ACTIVE state from SLEEP state, it executes the SLEEP-to-ACTIVE transition. For more information about the SLEEP → OFF transition, see Section 5.4.9.2, *SLEEP → ON and SLEEP → OFF Transitions*.

5.4.3 Power-Management Controller

The power-management system can independently drive the power states of three subsystems (P1, P2, and P3) or a combination of the three.

The power-management state-machine manages the PP, PR, and RC power resources. Configuration registers are accessible through application software by the GP I^2C interface. Figure 5-8 is a block diagram of the power-management state-machine.

Figure 5-8. Power-Management State-Machine



The power-management controller can drive two kinds of resources, analog and digital. The power-management receiver controls the analog resources and digital signals by its dedicated digital resources. Table 5-8 lists all the power resources.

The processor state-machine (P1 STM, P2 STM, and P3 STM) receives the state change requests (hardware or software) and generates the corresponding commands for the state changes to be given to the power-management bus (PMB). The sequencer block generates the power bus word sequences. Depending on the commands received from the previous stage, the sequencer finite state-machine (FSM) selects the appropriate sequencer operation to provide the required power sequence at the input of the PMB.

The sequencer fetches power words from the memory of the sequence and performs the following steps:

1. Extracts the delay to be inserted before generating the power command to be broadcast to the PMB controller
2. Extracts the address of the next power words to be decoded
3. Sends the power broadcast command to the PMB controller adding the associated DEV_GRP information
4. Waits for the delay to be terminated
5. Jumps to next power word to be decoded

The sequence memory contains the instructions for the sequencers. All subsystems share this memory. Each sequence memory word contains the following information:

- Address (6 bits): Current memory address
- Power-management word (16 bits): Power bus message to send through the interface
- Delay (5 bits): Time to wait before sending the next word on PMB
- Next address (6 bits): Memory address of the next power-management word to send on PMB

The PMB sends broadcast messages to the state registers, which control the dedicated resources. The analog resources are configured for power management depending on the values written to the state registers.

Power transition sequences for NO SUPPLY-to-WAIT-ON and WAIT-ON-to-ACTIVE are hard-coded, as power word values are implemented in ROM. Sequencing flexibility is achieved by programming the Next Address field and by the availability of 20 spare programmable memory locations (an address, delay, and power word can be programmed). Each value is a 32-bit word. This structure provides a way to change preprogrammed sequences (for example, shorter sequences, different power words, and different delays). The memory words that allow this are listed in Table 5-38. The first power boot sequence, which is hard-coded in ROM, must be completed to provide a correct supply to a processor so that it can execute software to modify later power sequences.

5.4.3.1 Power Bus Message Format

PMB messages have two formats, broadcast message and singular message.

5.4.3.1.1 Broadcast Message (16 Bits)

PMB messages can be considered timing ticks sent by the power-management FSM sequencer with state information for the addressed resources. All power resources connected on the PMB decode this message according to their DEV_GRP, RES_GRP, RES_TYPE, and RES_TYPE2 field configuration. The fields in the broadcast message are listed in Table 5-16.

Table 5-16. Broadcast Message Fields

DEV_GRP[0:2]	MT	RES_GRP[0:2]	RES_TYPE2[0:1]	RES_TYPE[0:2]	RES_STATE[0:3]

- DEV_GRP[0:2] indicates to which device group/subsystem the PMB is directed (P1, P2, and/or P3).
- MT indicates the message type: 0 = Singular, 1 = Broadcast
- RES_GRP[0:2] indicates to which resource group the PMB message is addressed: power provider (PP), power reference (PR), and/or reset and control (RC).
  - 000 = Reserved
  - 001 = PP
  - 010 = RC
  - 011 = PP and RC
  - 100 = PR
  - 101 = PP and PR
  - 110 = RC and PR
  - 111 = All resource groups
- RES_TYPE2[0:1] indicates which specific power resource is addressed. Up to a maximum of three different resources (RES_TYPE2) per resource group can be addressed by broadcast messages.
- RES_TYPE[0:2] indicates which specific power resource is addressed. Up to a maximum of six different resources (RES_TYPE) per resource group can be addressed by broadcast messages.
- RES_STATE[0:3] indicates the state to be assumed by the power resource (OFF, ACTIVE, or SLEEP).

5.4.3.1.2 Singular Message (16 Bits)

Table 5-17 lists the fields in the singular message.

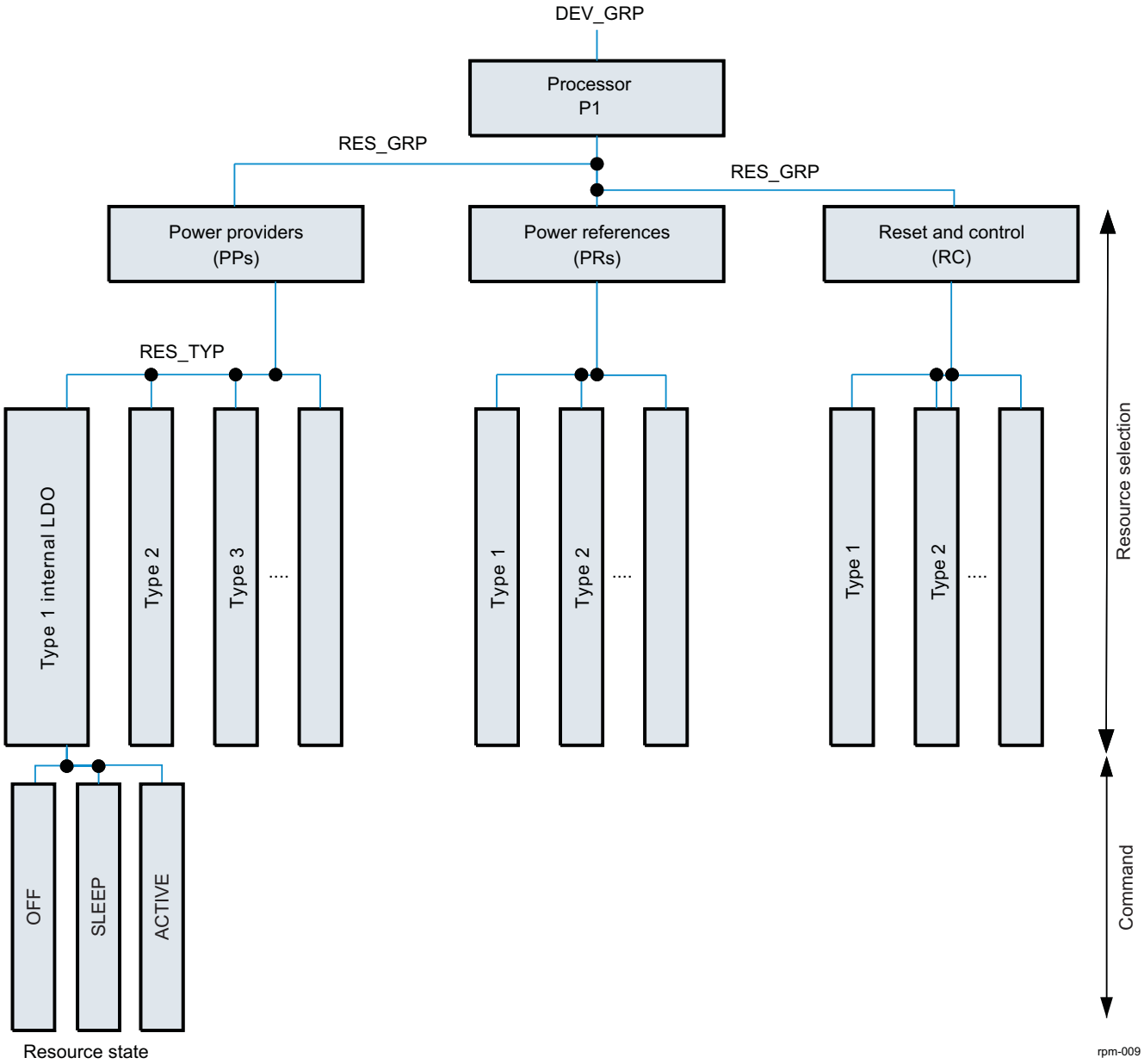
Table 5-17. Singular Message Fields

DEV_GRP[0:2]	MT	RES_ID[0:7]	RES_STATE[0:3]

- RES_ID [0:7] indicates to which of the 27 resources the PMB message is addressed.
- DEV_GRP, MT, and RES_STATE are the same as explained for the broadcast message.

Figure 5-9 shows the tree used to build the broadcast message for different power resources.

Figure 5-9. Broadcast Message Definition Tree



5.4.4 Resource Registers

Configuration registers are used to program the power resources. Software-controlled configuration registers trigger changes in the sequence memory.

5.4.4.1 Resource Configuration Register Fields

Table 5-18 lists the resource configuration register fields.

Table 5-18. Configuration Register Fields

DEV_GRP[0:2]	Device group identification: Indicates which processor group owns the power resources (P1, P2, and/or P3).
SLEEP_STATE[0:3]	This field of the REMAP register indicates the state to be taken by the resource in case of a system sleep transition.
OFF_STATE[0:3]	This field of the REMAP register indicates the state to be taken by the resource in case of a system off transition.
RES_STATE[0:3]	This read-only bit field of the DEV_GRP register indicates the current state of the resource.
<Resource>_DEDICATED[0:7]	This register is dedicated to specific configuration of the resource.

5.4.5 PMB Message to Resource State Registers

All PMB messages are sent to all resources. Each resource is defined by its RES_ID or RES_GRP, and RES_TYPE. The values of RES_ID and RES_GRP are fixed for all power resources. RES_TYPE is configurable in the <resource name>_TYPE register through the GP I^2C.

For a broadcast message, if the PMB messages RES_GRP and RES_TYPE match the resource configuration, the message is applied to that resource group.

The PMB messages DEV_GRP defines the resource requester. Each resource includes three internal state registers dedicated to each subsystem. If the message is applied to a resource, the PMB messages RES_STATE is written into the internal resource state register of the requester subsystem. For each resource, DEV_GRP in the <resource name>_DEV_GRP register indicates to which subsystems it belongs. It can be modified through GP I^2C access.

For each resource, a <resource name>_REMAP register allows modification of the resource state. When the system requires the resource to be in off mode, the OFF_STATE bit field of the REMAP register allows setting of the resource to sleep or active mode; for example, VAUX1_REMAP[3:0]. When the system requires the resource to be in sleep mode, the SLEEP_STATE bit field of the REMAP register allows setting of the resource in off or active mode; for example, VAUX1_REMAP[7:4]. The final resource state can be read in the STATE bit field of the <resource name>_DEV_GRP register.

5.4.6 Software Events for State Changes

The P1_SW_EVENTS, P2_SW_EVENTS, or P3_SW_EVENTS register can initiate a state transition for the corresponding subsystem. Table 5-19 lists the bit fields for these registers, and Table 5-20 lists the fields that are programmable and can change the states for the device.

Table 5-19. Register Bit Fields for Initiating a Software State Transition

Reserved (7)	STOPON_ PWRON (6)	STOPON_ SYSEN (5)	ENABLE_WARMRESET (4)	LVL_ WAKEUP (3)	DEVACT (2)	DEVSLP (1)	DEVOFF (0)

Table 5-20. Programmable Register Bit Fields for Initiating a Software State Transition

Software Events	Coming From	Description	State Transitions
DEVOFF	Pi	Writing 1 starts an ACTIVE-to-OFF or SLEEP-to-OFF transition. Bit automatically cleared.	ACTIVE → WAIT-ON SLEEP → WAIT-ON
DEVACTIV	Pi	Writing 1 starts an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition. Bit automatically cleared.	WAIT-ON → ACTIVE SLEEP → ACTIVE
DEVSLP	Pi	Writing 1 starts an ACTIVE-to-SLEEP transition. Bit automatically cleared.	ACTIVE → SLEEP

Additional information:

The DEVOFF bit works with the SEQ_OFFSYNC bit. If the SEQ_OFFSYNC bit is set to 1, all resources go to WAIT-ON state, regardless of the DEVOFF bit setting in the P[123]_SW_EVENTS register. If the SEQ_OFFSYNC bit is set to 0, only the resource set by DEVOFF goes to WAIT-ON state.

The LVL_WAKEUP bit configures the sleep and active modes for resources for the subsystem (P1, P2, or P3). When this bit is set to 0, the nSLEEPx signal cannot set the Px resources to sleep mode, but a rising edge of the nSLEEPx signal causes a wakeup for the P1 subsystem. Writing 1 to this bit sets the Px resources to active mode when nSLEEPx is high, and to sleep mode when nSLEEPx is low.

NOTE: The software must ensure that this bit is programmed after programming the ACTIVE-to-SLEEP and SLEEP-to-ACTIVE sequence in the device memory.

5.4.7 Hardware Events for State Changes

Table 5-21 lists the hardware events that trigger state transitions. The hardware events can be masked using the following registers:

- CFG_P1_TRANSITION
- CFG_P2_TRANSITION
- CFG_P3_TRANSITION

Table 5-21. Register Fields for Initiating a Hardware State Transition

Hardware Events	Coming From	Signal Description	State Transitions
nSLEEP1	P1	Resource associated with P1 is put to sleep when signal is low and is active when high.	SLEEP ↔ ACTIVE for P1
CLKREQ	P3	Resource associated with P3 is put to sleep when signal is low and is active when high.	SLEEP ↔ ACTIVE for P3
PWRON	Button press	This is a hardware-triggering event activated by a keypad button press ([1]).	WAIT-ON ↔ ACTIVE SLEEP → ACTIVE
nRESWARM	Pi	Set the device in a defined ACTIVE state.	ACTIVE or SLEEP → ACTIVE
PLUG_USB	USB	USB plug signal	WAIT-ON → ACTIVE SLEEP → ACTIVE
RTC_Alarm	Device internal	RTC request to initiate an active transition	SLEEP → ACTIVE WAIT-ON → ACTIVE
Main Battery Low (MBLO)	Device internal	Indicates whether VBAT < 2.7 V	Any state → Backup (or NO SUPPLY)
THERM_TS	Device internal	Thermal sensor request to generate a backup reset	Any state → WAIT-ON

[1] The KEYP_CTRL_REG[6] KBD_ON bit must be set to 1 (for more information, see Chapter 9, *Keypad Controller*).

NOTE: The USB plug signal is debounced. The debounce time is configured in the RESERVED_E[2:0] CFG_VBUSDEB bit field.

5.4.7.1 Sequence Word Delay

Table 5-22 lists the programmable delay in terms of 32-kHz clocks. The value for the delay is programmed in the memory word.

Table 5-22. PMB Delays

Basic Delay Divider	Timer							
	0	1	2	3	4	5	6	7
0	0	1	2	3	4	5	6	7
1	8	10	12	14	16	18	20	22
2	24	28	32	36	40	44	48	52

Table 5-22. PMB Delays (continued)

Basic Delay Divider	Timer							
	0	1	2	3	4	5	6	7
3	56	64	72	80	88	96	104	112

5.4.8 Power-Management Sequencing Memory Structure

A memory composed of 64 32-bit sequence words contains all messages sent by the sequencers on the PMB. Each sequence word contains the following information:

- The 16-bit message composed sent on the PMB. This message is composed of the two MSG_M and MSG_L words.
- The 8-bit delay before sending the next 16-bit message of the next sequence word
- The 6-bit most-significant bit (MSB) address in the memory of the next sequence word

A sequence base address is defined for each of the seven programmable pointers (registers). A specific sequence is running when a state transition occurs. Each pointer contains a value from 0x00 to 0x3F that corresponds to the first 32-bit sequence word location address in the power-management sequencing memory to be executed.

Table 5-23 lists the power-management sequencing pointers.

Table 5-23. Power-Management Sequencing Pointers

Pointer	Default Memory Address Value	Description
SEQ_ADD_W2P[5:0] SEQ_ADD	0x00	WAIT-ON-to-PRESENCE sequence base address
SEQ_ADD_P2A[5:0] SEQ_ADD	0x04	PRESENCE-to-ACTIVE sequence base address
SEQ_ADD_A2W[5:0] SEQ_ADD	0x0D	ACTIVE-to-WAIT-ON sequence base address
SEQ_ADD_A2S[5:0] SEQ_ADD	0x3F	ACTIVE-to-SLEEP sequence base address
SEQ_ADD_S2A12[5:0] SEQ_ADD	0x3F	P1 and P2 SLEEP-to-ACTIVE sequence base address
SEQ_ADD_S2A3[5:0] SEQ_ADD	0x3F	P3 SLEEP-to-ACTIVE sequence base address
SEQ_ADD WARM[5:0] SEQ_ADD	0x3F	Warm-reset sequence base address

Table 5-24 describes the structure of the power-management sequencing memory.

Table 5-24. Power-Management Sequencing Memory Structure

MSB Address (6-Bit)	Memory Word (32 bits)				Comment
	MSG_M Word (LSB Address 0b00)	MSG_L Word (LSB Address 0b01)	Delay Word (LSB Address 0b10)	Next Address Word (LSB Address 0b11)	
0x00					Default boot mode
0x01					
…					
0x0E					
0x1F					Not used
…					Not used
0x2A					Not used
0x2B					Spare word
…					Spare words
0x3E					Spare word
0x3F					EOS: End of sequence

Read/write word
Read-only word
Not used and read-only

For the memory location 0x00 to 0x0E, only the next address word (with the least-significant bit [LSB] address = 0b11) can be written. Thus, a next address word can be set to a spare word address. The 32-bit words at the MSB address 0x1F to 0x2A are not used. Twenty spare words can be used to modify or create a new power sequence. When the next address word equals 0x3F, it indicates the end of the sequence.

The user can access the power-management sequencing memory only 8-bit word by 8-bit word. The address of an 8-bit word (MSG_M word, MSG_L word, delay word, or next address word) is composed of the 6-bit MSB address and the 2-bit LSB address of the word (0b00: MSG_M word, 0b01: MSG_L word, 0b10: delay word, 0b11: next address word).

An 8-bit word is accessed in the power-management sequencing memory through the I^2C interface by:

- Programming the MEMORY_ADDRESS register with the address of the 8-bit word to be accessed
- Writing or reading the MEMORY_DATA register that contains the 8-bit word written to or the 8-bit word read from the power-management sequencing memory

Table 5-25 through Table 5-28 list the formats for the memory message bytes, delay byte, and the next address byte, respectively.

Table 5-25. Memory Message Byte (MSG_M) Format

Word Memory Address	MSG_M Word 0b00							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PB_MSG[7]	PB_MSG[6]	PB_MSG[5]	PB_MSG[4]	PB_MSG[3]	PB_MSG[2]	PB_MSG[1]	PB_MSG[0]
Reset Value	0	0	0	0	0	0	0	0

Table 5-26. Memory Message Byte (MSG_L) Format

Word Memory Address	MSG_L Word 0b01							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				PB_MSG[12]	PB_MSG[11]	PB_MSG[10]	PB_MSG[9]	PB_MSG[8]
Reset Value	0	0	0	0	0	0	0	0

Table 5-27. Delay Byte Format

Word Memory Address	Delay Word 0b10							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	–	–	Divider[1]	Divider[0]	–	Timer[2]	Timer[1]	Timer[0]
Reset Value	0	0	0	0	0	0	0	0

Table 5-28. Next Address Byte Format

Word Memory Address	Next Address Word 0b11							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	–	–	NEXT ADDRESS[5:0]					
Reset Value	0	0	0	0	0	0	0	0

5.4.9 State Transitions

5.4.9.1 Switch-On and Switch-Off Transitions

To allow flexibility in the power-up sequences, for the device FSM there are 13 steps for the transition from WAIT-ON to ACTIVE and 2 steps for the transition from ACTIVE to WAIT-ON. The power bus resource designer must code the resource type in the power-up sequence based on the correct resource enable timing.

To avoid timing misalignment and thus voltage misalignment during the power-up sequence, the WAIT-ON to ACTIVE and ACTIVE to WAIT-ON sequences are divided into steps occurring at the same time for all sequences. This is possible because of the synchronization capability enabled by default at boot time. At boot stage, the system resources required for the default WAIT-ON-to-ACTIVE sequence are enabled. This allows a first stage of software functionality to configure power resources of the device for specific system needs. One of these configurations can concern the sequence, thus allowing the capability of modifying the PMB transmitted words or even swapping the sequence order. The programmer must remember that those modifications remain valid only if the system does not enter NO SUPPLY state. If a restart from the latter state occurs, the default sequence, not the modified sequence, executes.

Table 5-29 lists the 13 steps for the the WAIT-ON → to → ACTIVE transition for C027 mode.

Table 5-29. WAIT-ON to ACTIVE for C027 Mode (Power-Up Sequence)

Sequence MC027S	MEM ADD	Memory Word	CLK32K	Delay (µs)	NEXT_ADD
WAIT-ON 2 PRESENCE	0	Active broadcast for all PR (MAIN_REF)	36	1099	1
WAIT-ON 2 PRESENCE	1	Enable PP VINTDIG and VINTANA1 (Type 1).	20	610	2
WAIT-ON 2 PRESENCE	2	Enable PP VUSB3V1.	20	610	3
WAIT-ON 2 PRESENCE	3	Enable PP VINTANA2.	36	1099	63
PRESENCE 2 ACTIVE	4	Enable Type 2 REGEN.	19	580	5
PRESENCE 2 ACTIVE	5	Enable Type 3 VAUX2, VIO (VIO CLK3M, then VIO).	32	977	6
PRESENCE 2 ACTIVE	6	Enable Type 4 VDD1 (VDD1 CLK3M, then VDD1), VPLL2.	56	1709	7
PRESENCE 2 ACTIVE	7	Enable Type 5 VDD2 (VDD2 CLK3M, then VDD2) and HFCLK_EN.	72	2197	8
PRESENCE 2 ACTIVE	8	ACTIVE state broadcast for all PP (VPLL1)	4	122	9
PRESENCE 2 ACTIVE	9	Enable RC CLK32K_OUT.	2	61	10
PRESENCE 2 ACTIVE	10	Enable RC SYSEN and release TRITON_RESET_NA (Type 6).	96	2930	11
PRESENCE 2 ACTIVE	11	Enable RC HFCLK_OUT.	2	61	12
PRESENCE 2 ACTIVE	12	ACTIVE state broadcast for all subsystems (nRESPWON)	2	61	63

Table 5-37 lists other power-up sequences. Table 5-30 lists the two steps associated with the resources going from ACTIVE state to WAIT-ON state.

Table 5-30. ACTIVE-to-WAIT-ON (2 Steps)

MEM ADD	Memory Word	CLK32K	Delay (µs)	NEXT _ADD
SEQ_ADD_A2W[5:0] SEQ_ADD	System reset (Triton forces SysActiv, Nrespwron digital signals to OFF and stop HFCLK_OUT)	40	1221	SEQ_ADD_A2W[5:0] SEQ_ADD + 1
SEQ_ADD_A2W[5:0] SEQ_ADD + 1	OFF state broadcast for all RES_GRP	112	3418	63

5.4.9.2 SLEEP → ON and SLEEP → OFF Transitions

SLEEP → ON and SLEEP → OFF transitions (see Table 5-31 and Table 5-32) are characterized by the presence of full or partial supply voltage on all required power domains, thus avoiding potential current leakage between power domains in use and power domains not in use.

For ACTIVE-to-SLEEP and SLEEP-to-ACTIVE transitions, the sequence depends on the situation (there is no default sequence). For example, a P1 SLEEP-to-ACTIVE sequence can be executed at the same time as a P2 ACTIVE-to-SLEEP sequence.

Table 5-31. ACTIVE-to-SLEEP (SLEEP ON)—2 Steps

MEM ADD	Memory Word	CLK32K	Delay (µs)	NEXT _ADD
SEQ_ADD_A2S[5:0] SEQ_ADDSEQ_ADD_A2S[5:0] SEQ_ADD	SLEEP broadcast for RC	2	61	SEQ_ADD_A2W[5:0] SEQ_ADD + 1
SEQ_ADD_A2S[5:0] SEQ_ADD + 1	SLEEP broadcast for PP (and PR)	2	61	63

Table 5-32. SLEEP-to-ACTIVE (SLEEP OFF)—3 Steps

MEM ADD	Memory Word	CLK32K	Delay (µs)	NEXT _ADD
Base address	Enable RC HFCLK_EN	2	61	Base address + 1
Base address + 1	ACTIVE broadcast for PP (and PR)	2	61	Base address + 2
Base address + 2	ACTIVE broadcast for RC	2	61	63

NOTE: The base address equals the SEQ_ADD_S2A3[5:0] SEQ_ADD bit field for the P3 SLEEP-to-ACTIVE transition sequence.

The base address equals the SEQ_ADD_S2A12[5:0] SEQ_ADD bit field for the P1 and P2 SLEEP-to-ACTIVE transition sequence.

5.4.10 Dynamic Voltage Scaling Management

For the dynamic voltage settings for different resources, see Section 6.4.1.1, *VDD1 SMPS Regulator*.

5.4.10.1 Voltage Scaling Using VMODE1/2 in C027 Mode

In this mode, the VDD1 voltage can be controlled, depending on the value of ENABLE_VMODE.

5.4.10.1.1 Direct Control

If the value of the VDD_VMODE_CFG[0] ENABLE_VMODE bit is 0, VDD1 voltage is directly controlled by the VDD1_VSEL[6:0] VSEL bit field. VDD voltage is calculated as VSEL x 12.5 mV + 0.6 V.

If the VDD_VMODE_CFG[2] DCDC_SLP bit is 0, output voltage in sleep mode is the same as in active mode. If the DCDC_SLP bit is 1, output voltage in sleep mode has the value as set in the VDD_VFLOOR[6:0] VFLOOR bit field.

5.4.10.1.2 Control Using VMODE

If the value of the ENABLE_VMODE bit is 1, VDD voltage is controlled by the VMODE pin. The power resource changes the voltage depending on the VMODE input. The VDD voltage is programmed through VROOF and VFLOOR. On the VMODE rising-edge transition, the VDD voltage changes from the VFLOOR value to the VROOF value; on the VMODE falling edge, the VDD voltage changes from the VROOF value to the VFLOOR value. VROOF and VFLOOR values must be set before the ENABLE_VMODE register bit is set.

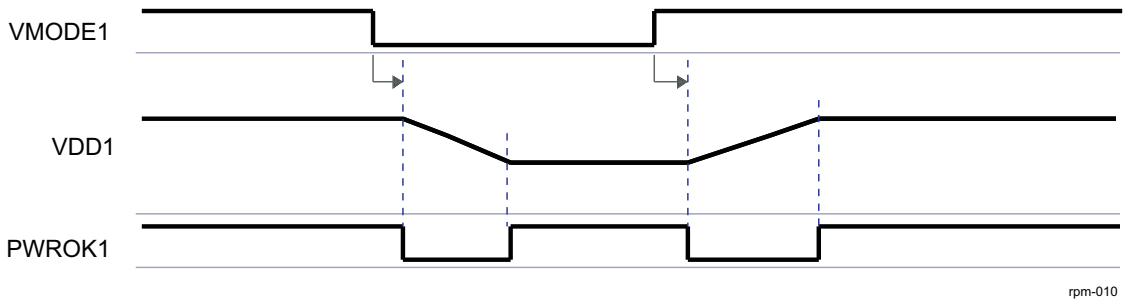
Voltage scaling occurs in 12.5-mV steps. The duration of each step can be programmed between 0 and 310 μs. This is programmable by the VDDx_STEP[4:0] STEP_REG bit field. If the duration of the step is 0, the voltage slew rate between the VFLOOR and VROOF is that of the DCDC which is 12.5-mV/3*DCDC clock cycles.

The transition between modes is different depending on whether STEP_REG = 0x0 or not. If STEP_REG = 0x0, also known as JUMP mode, regardless of whether the DCDC voltage is higher or lower than the VROOF or VFLOOR, the VSEL voltage will “jump” to these levels the moment the VMODE is enabled. To ensure correct operation the voltage change should be such that when you enable the VMODE function the voltage should not decrease from the actual voltage, for example, if VMODE = 0; VFLOOR > VSEL; or if VMODE = 1; VROOF > VSEL. This can be ensured for targeted resources, by reading the VSEL value via a register access to VDDx_VSEL register before setting VROOF and VFLOOR registers and VMODE_EN = 1.

If STEP_REG > 0x0, also knows as STEP mode then the following behaviour is observed. When VMODE is enabled, if VMODE = 0 the VSEL will transition to the VFLOOR level only if VFLOOR < VSEL. If VMODE = 1 at the moment VMODE is enabled then VSEL will transition to VROOF level only if VROOF > VSEL, otherwise the VSEL remains at the originally programmed level until a transition is seen on VMODE. In both JUMP mode and the STEP mode if the voltage of the VFLOOR or VROOF is modified while the VMODE is enabled the new value will be taken into account on the next VMODE transition which uses that level.

Figure 5-10 is the timing diagram.

Figure 5-10. Dynamic Voltage Setup Using VMODE



5.4.10.2 Management Using I²C SmartReflex Control in C021 Mode

SmartReflex is a power-management technology. It is a voltage-control technique for reducing the worst-case power of a design while maintaining the required performance frequency. With SmartReflex, it is possible to meet a specific frequency performance from a strong silicon device at a much lower voltage than from a weaker silicon device. SmartReflex takes advantage of this by lowering the supply voltage, resulting in lower active and leakage power. The voltage is determined by the performance capability of the silicon in the current environment (that is, the process, voltage, and temperature).

In this mode, a dedicated high-speed I²C can set the VDD and VPLL low-power signals and voltages. The VDD scaling is calculated in the same way as in Section 5.4.10.1.1, *Direct Control*.

To set the VDD1 voltage level, modify the VDD1_SR_CONTROL[6:0] VSEL bit field. If the VDD1_SR_CONTROL[7] MODE bit is 1, VDD is in sleep mode; otherwise, it is in active mode.

To set the VDD2 voltage level, modify the the VDD2_SR_VSEL[6:0] VSEL bit field. If the VDD1_SR_VSEL[7] MODE bit is 1, VDD is in sleep mode; otherwise, it is in active mode.

If the VDD2 is in sleep mode, VPLL is in sleep mode, and VIO is in sleep mode if no other processor needs it. The registers are described in Table 5-428 and Table 5-430.

5.4.11 BCI Functional Description

5.4.11.1 BCI Description

Figure 5-11 is a top-level block diagram of the BCI module in the device. The BCI communicates with the MADC, power, and USB modules in the device. Communication between the BCI and other modules is controlled by the finite state-machine (FSM) for precharge and main charge. In software-controlled mode, some programmable registers are modified for specific control, as discussed in , *Programming Model*. The BCI analog hardware interfaces with the device external pins, as shown in Figure 5-11, and the digital section sends and receives signals to and from other modules in the device.

Figure 5-11. BCI in the Device

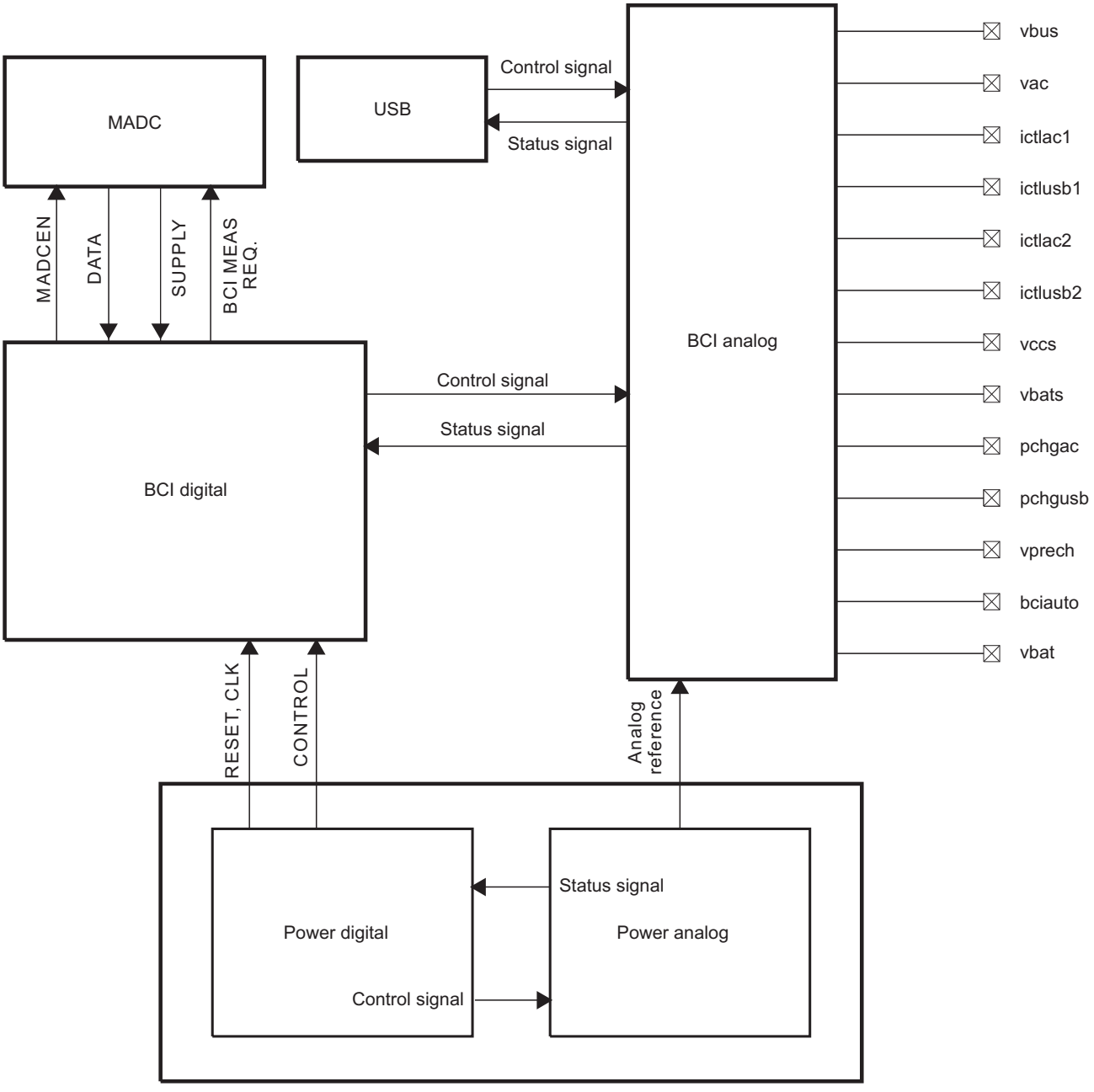


Table 5-33 lists the modes of operation for the BCI and the analog hardware used for the corresponding mode.

Table 5-33. BCI Operating Modes for the Device

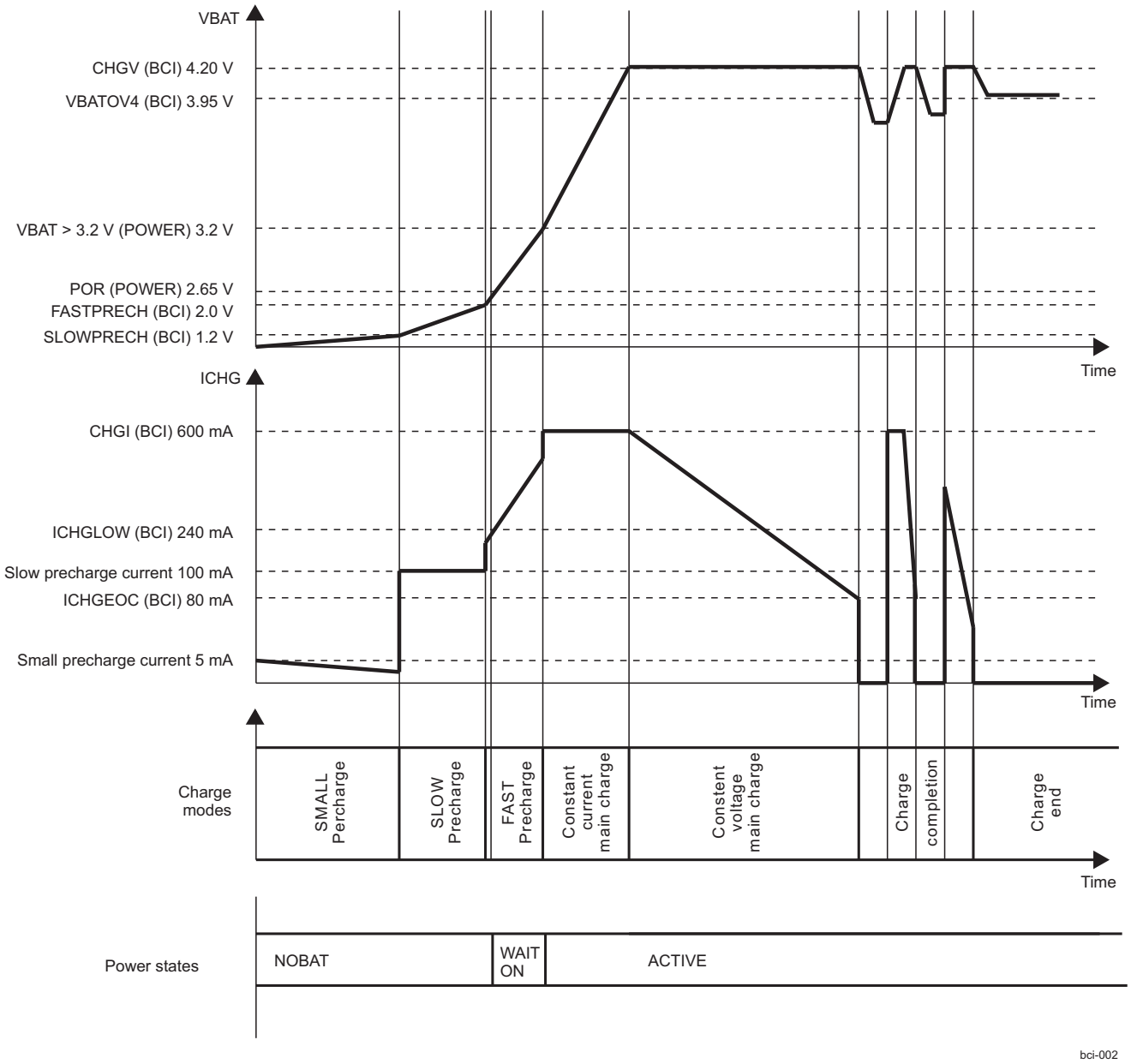
				Device Plugged In					Analog Hardware Used				
		Automatic/manual	Conditions for entering the mode	Ac chargers	USB chargers, carkits	USB host, MCPC	Ac accessory	USB accessory	Precharge hardware	Main charge hardware	Precharge analog comparators	Main charge analog comparators	MADC monitoring functions
Operating modes	Precharge	Automatic	SYSACTIV = 0 and short detect timer = 0 and charging device connected	X	X	X			X				
	Main charge	Automatic	BCIAUTOAC = 1 or BCIAUTOUSB = 1 and SYSACTIV = 1 and 3.2 V < VBAT < 4.55 V and charging device connected	X	X					X	X	X	X
		Software-controlled	LINCHEN = 1 and charging device connected	X	X	X				X	X	X	X
	Pulsed charge	Software-controlled	PWMEN = 1 and charging device connected	X						X	X	X	X
	Constant voltage (CV)	Automatic	LDOOK = 1 and battery open and charging device connected	X						X	X	X	X
	Accessory supply	Software-controlled	ACCSUPEN = 1 and accessory device connected				X	X		X	X		X

There are five operating modes for the BCI, some automatic, and some software-controlled. In automatic mode, the state-machine controls the charging steps.

Figure 5-12 is a chronogram of a typical automatic charge sequence. In precharge mode, there is no software access. The precharge state-machine controls charging up to 3.2 V. When the VBAT voltage exceeds 3.2 V, the SYSACTIV signal goes high. The power regulators are turned on and the device power-management system is activated. This also activates the power-management state-machine.

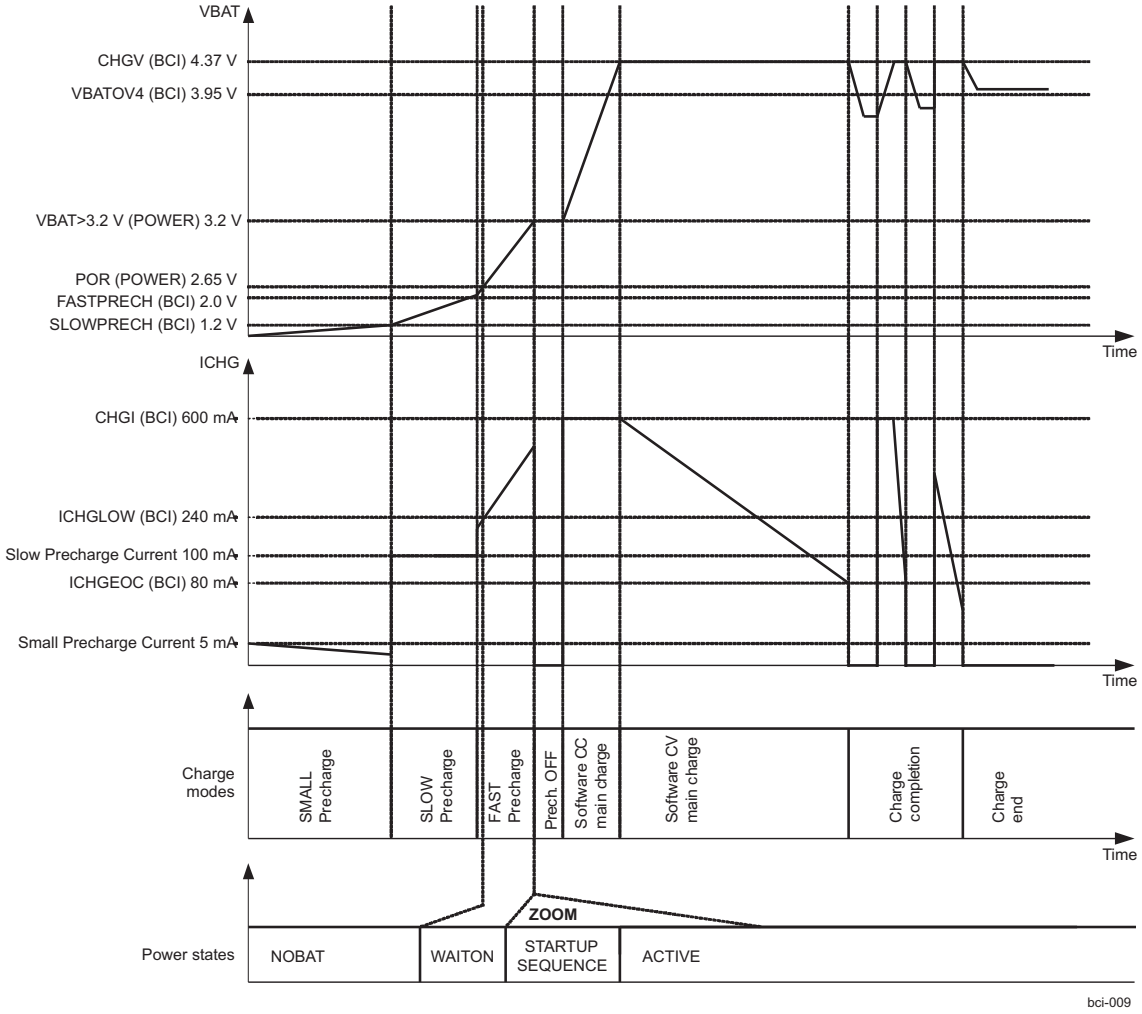
The sequence timing diagram in Figure 5-12 shows the charging sequence. A similar charging sequence can be configured in software-controlled mode.

Figure 5-12. Ac Automatic Charge Sequence Chronogram



The sequence timing diagram in Figure 5-13 shows the automatic charging sequence.

Figure 5-13. USB Automatic Charge Sequence Chronogram



5.4.11.1.1 Precharge

Precharge is systematically enabled when a charging device is connected. There is no software control for this mode. Precharge is independent of battery type. The analog core can perform three precharging schemes: small precharge, slow precharge, and fast precharge.

NOTE: Fast precharge with charger is not supported. For more information, see Section 5.4.11.1.1.6, *Fast Precharge Detection*.

The precharge FSM configures and controls the analog hardware automatically. The FSM is described in Figure 5-14.

Precharge stops automatically when the power-management system starts (the power state-machine is in active mode because VBAT > 3.2 V and an ac charger or a USB device is plugged in; the SYSACTIV signal is forced to 1). Precharge restarts automatically when the power-management system stops (the power state-machine is in backup mode because VBAT < 2.7 V; the SYSACTIV signal is forced to 0).

5.4.11.1.1.1 BCIAUTO Voltage Detection

The BCIAUTO level-detection comparator, which is part of the precharge analog hardware, detects when

a 0-kΩ (grounded pin) or larger than 140-kΩ comparator resistor is plugged between the BCIAUTO pin of the device and ground. The BCIAUTO level-detection comparator generates 2 bits: CVENACA and BCIAUTOACA. The CVENACA bit enables CV mode (the system starts with the battery disconnected) with the ac chargers. BCIAUTOACA enables the automatic charge with ac chargers. The CVENACA and BCIAUTOACA output bits of the BCIAUTO level detection are set as follows:

If CONFIG_DONE = 0:

	CVENAC	BCIAUTOAC
Rbciauto < 10 kΩ	CVENACA = 0	BCIAUTOACA = 0
Rbciauto > 140 kΩ	CVENACA = 1	BCIAUTOACA = 1

If CONFIG_DONE = 1, regardless of the value of the resistor connected on the BCIAUTO pin, CVENAC and BCIAUTOAC take the value written in the BOOT_BCI register.

The BOOT_BCI register has its reset value set to BCIAUTOAC = CVENAC = CONFIG_DONE = 1, which means that an automatic charge is enabled by default: BCIAUTOAC = 1 (software access is required to disable the automatic charge by clearing BCIAUTOAC to 0). CV mode is also the default configuration but requires a specific resistor for CVENACA = 1. For USB modes, BCIAUTOUSB is set and enables the automatic charge by the carkit or USB charger.

Avoid writing to the BCIMDEN register (using the BCIMDKEY register) when the BCIAUTOAC or BCIAUTOUSB input signal is forced to 1.

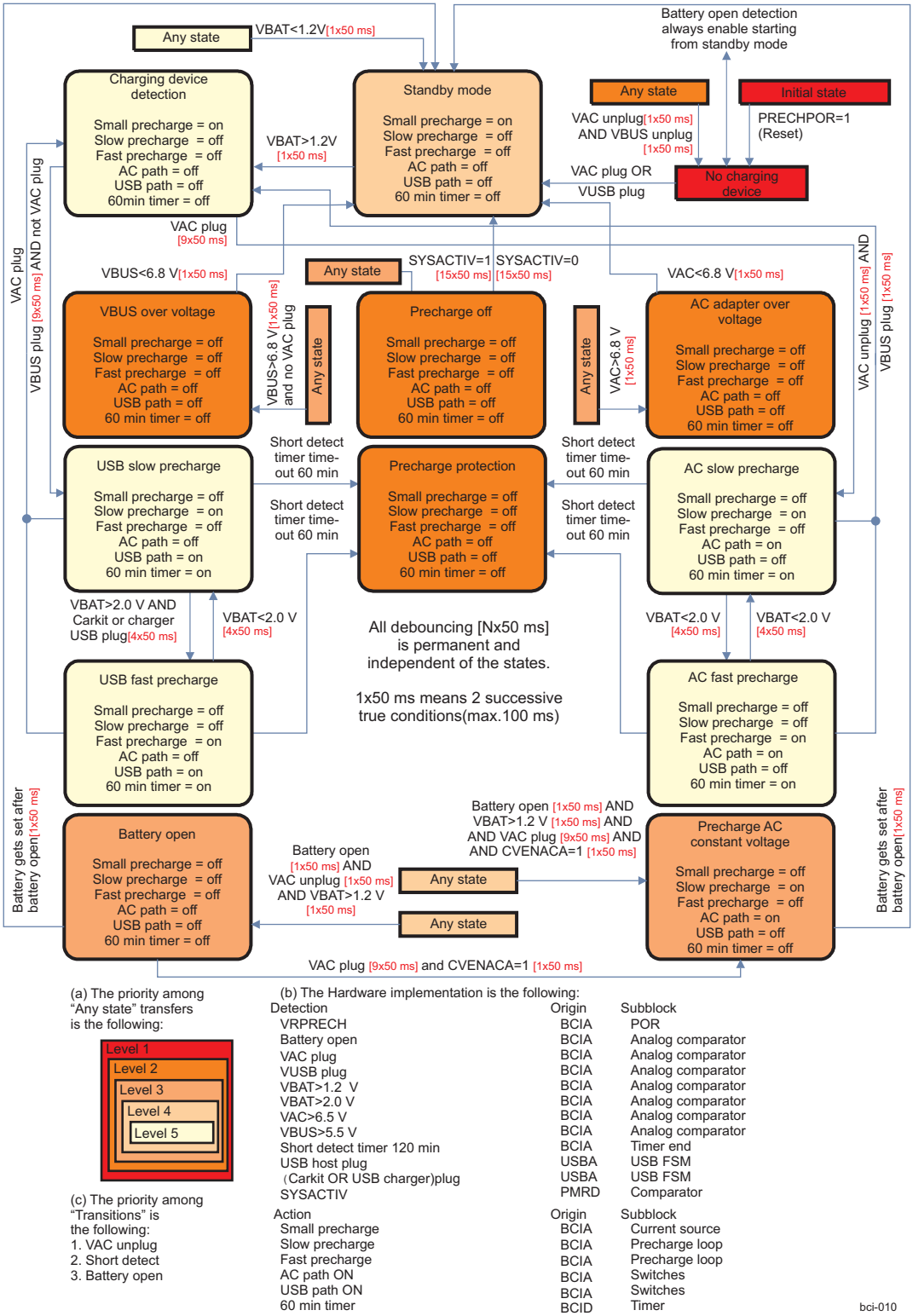
The device precharge includes the following monitoring functions:

- Ac charger detection comparator
- USB voltage (VBUS) detection comparator
- Battery open detection comparator
- VBUS overvoltage comparator
- Ac charger overvoltage comparator

The state-machine controls all of these comparators, which are shown in Figure 5-14. These comparators are not software-controlled.

NOTE: BCI balls VBATS and VCCS are not part of this device.

Figure 5-14. Precharge State-Machine



5.4.11.1.1.2 Ac Charger Detection

The ac charger presence comparator, which is part of the precharge analog hardware, detects whether an ac charger is plugged or unplugged. An interrupt is generated when the ac charger voltage is higher than the (battery voltage + 400 mV typical), or when the ac charger voltage is lower than the (battery voltage + 100 mV typical).

NOTE: In the main charge state-machine, this ac charger detection defines the VAC plug or unplug conditions.

5.4.11.1.1.3 VBUS Detection

The VBUS presence comparator, which is part of the precharge analog hardware, detects whether a USB device capable of supplying the VBUS pin is plugged in. When VBUS is detected (VBUS voltage is higher than 4.4 V), a communication between the BCI and the USB detects whether the USB device plugged is a USB host, a carkit, or a USB charger. Fast precharge with charger is not supported. For more information, see Section 5.4.11.1.1.6, *Fast Precharge Detection*.

NOTE: In the main charge state-machine, the VBUS is detected with a logical OR between the BCIMFSTS4[2] USBFASTMCHG and the BCIMFSTS4[1] USBSLOWMCHG bits.

5.4.11.1.1.4 Precharge Battery Open Detection

The precharge battery presence comparator, which is part of the precharge analog hardware, detects whether a battery is open in precharge mode. The BCIMFSTS1[3] BATSTSPCHG bit rises when the thermistor of the battery pack is connected to the ADCIN1 pin (the impedance connected between ADCIN1 and ground is lower than 100 kΩ).

NOTE: BCIMFSTS1 is a test register and hence is not shown in the register description. If the user wants to measure the resistance manually in precharge mode, this information will be helpful.

5.4.11.1.1.5 VBUS Overvoltage Detection

The VBUS overvoltage comparator is a hardware security feature that detects whether the VBUS voltage is higher than 6.8 V during precharge. The VBUS overvoltage comparator is part of the main charge analog hardware and is reused for the precharge. When the VBUS voltage is higher than 6.8 V typical during precharge, the BCIMFSTS2[1] VBUSOV bit rises and an interrupt is generated.

NOTE: VBUS overvoltage protection starts automatically in precharge mode.

5.4.11.1.1.6 Fast Precharge Detection

The fast precharge detection comparator, which is part of the precharge analog section, detects whether the battery voltage is higher than 2.0 V.

Table 5-34 lists the supported precharge type versus the precharge sources.

Table 5-34. Supported Precharge Types Versus Precharge Sources

	Precharge Type Supported		
	Slow	**Small**	**Fast**
Charger	Yes	Yes	No
Carkit	Yes	Yes	Yes
PC	Yes	Yes	No

5.4.11.1.1.7 Slow Precharge Detection

The slow precharge comparator, which is part of the precharge analog hardware, detects whether the battery is higher than 1.2 V.

5.4.11.1.1.8 Ac Charge Overvoltage Detection

The ac charge overvoltage comparator is a hardware security feature that detects whether the ac charge voltage is higher than 6.8 V during precharge. The ac charge overvoltage comparator is part of the main charge analog hardware and is reused for the precharge.

NOTE: Ac charger overvoltage protection starts automatically in precharge.

5.4.11.1.2 Main Charge

5.4.11.1.2.1 General Description

Precharge stops automatically when the power-management system starts (the power state-machine is in active mode and the SYSACTIV signal is forced to 1). The main charge can use two modes, software-controlled and automatic.

In software-controlled mode, device registers that can be programmed by the inter-integrated circuit (I^2C™) interface control and configure the analog hardware ac or USB main charge. In software-controlled mode, the USB charge supports charges with a USB host, MCPC, USB chargers, and carkits. The software enables the charging schemes, the charge path, and the charge-monitoring functions to be started.

In automatic mode, the main charge FSM controls and configures the analog hardware ac or USB main charge automatically. Figure 5-15 is the main charge state-machine. Figure 5-16 is the state transfer diagram. The FSM directly controls the registers. In automatic mode, USB charge supports charges with USB chargers and carkits. The FSM enables:

- Charging schemes to be used
- Charge path to be selected
- Charge-monitoring functions to be started
- Threshold parameters to be used (for example, overvoltage and overtemperature limits, timers to be launched, the function of the charging device plugged in, and battery status).

Parameters such as threshold and timers can be changed by software during an automatic charge.

The BCIAUTO boot pin selects between automatic and software-controlled modes and enables CV mode. BCIAUTO is associated with two power backup domain register bits (BCIAUTOAC and CVENAC).

Ac charging starts or stops automatically when an ac charger is plugged in or unplugged. In the case of a USB charger, automatic charging starts and stops according to a specific programming sequence.

If multiple charge sources are applied in automatic mode, an arbitration scheme is used and the ac charger has priority for charge and precharge.

For charging using USB, the software must enable the USB automatic charge by forcing the BOOT_BCI[1] BCIAUTOUSB bit to 1. When the USB charger is plugged in, the software detects the type of device (USB charger or carkit charger). The software must set the POWER_CTRL[5] OTG_EN bit to 1 at least 50 ms before forcing the BCIMFSTS4[2] USBFASTMCHG bit to 1.

In the hardware method, the VBUS comparator must be kept enabled by setting the BCIMFSTS4[5] VBUSUNPLGEN bit to 1. This comparator uses VBUS and battery voltage (VBAT) monitoring functions. It detects VBUS < VBUSVT (default 4.3 V) if VBAT < VBATVT (default 4.2 V) or VBUS < VBUSVT + 0.2 V (default 4.5 V) if VBAT ≥ VBATVT. The VBUS unplug condition automatically stops the charge by forcing the BCIMFSTS4[2] USBFASTMCHG and BCIMFSTS4[1] USBSLOWMCHG bits to 0. The VBUS and VBAT thresholds are programmed using the BCIMFEN4[5:4] VBATVT and BCIMFEN4[7:6] VBUSVT bit fields. The comparator results are stored in the BCIMFSTS4[7] VBUSINFVT and BCIMFSTS4[6] VBATINFVT bits.

In software mode, the VBUS comparator is disabled by setting the VBUSUNPLGEN bit to 0. The software detects that the USB device is unplugged and stops charging. The USB charge is stopped by forcing the USBFASTMCHG and USBSLOWMCHG bits to 0.

Figure 5-15. Main Charge State-Machine

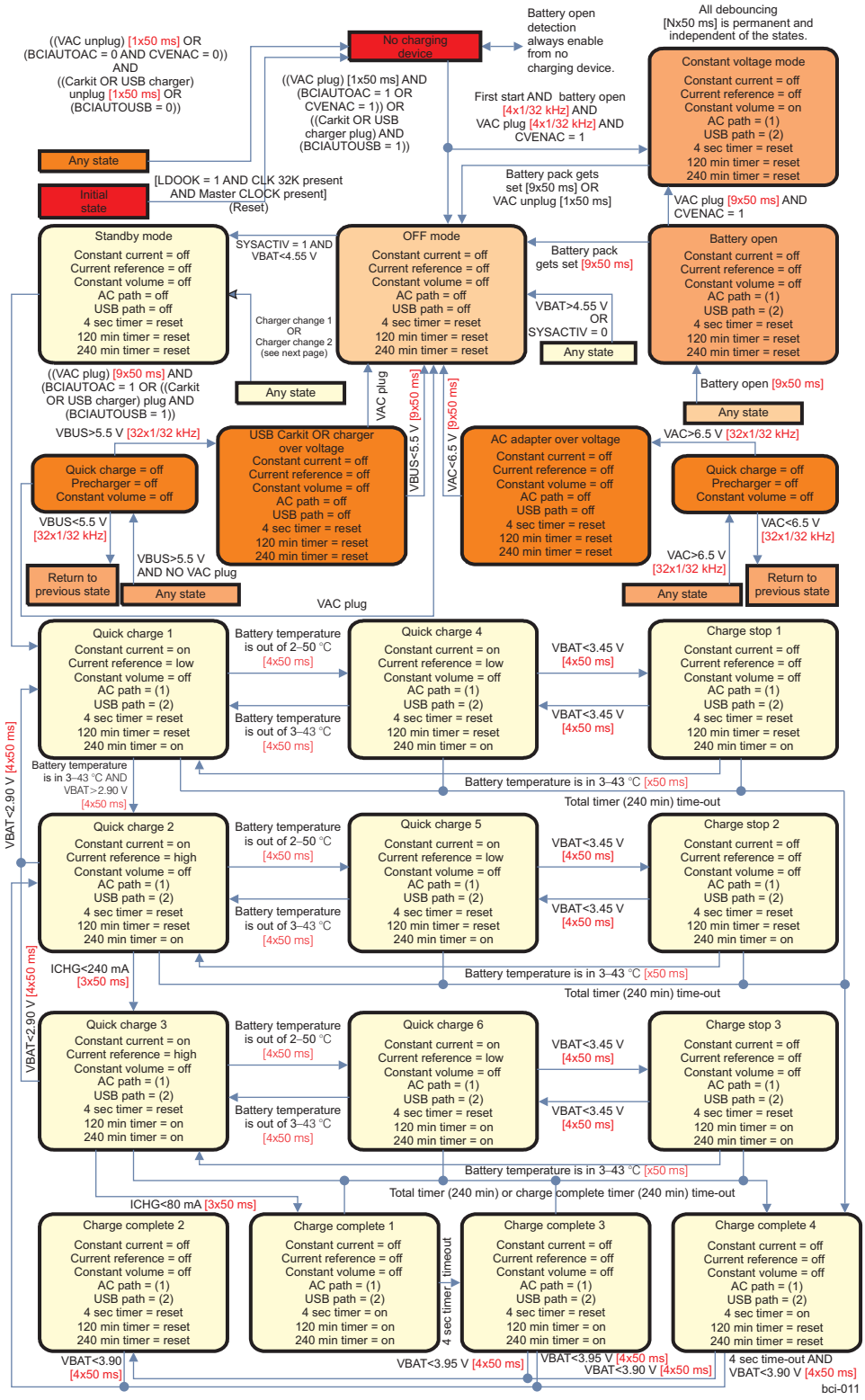
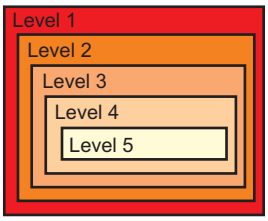


Figure 5-16. Main Charge State Transfer Diagram

CHARGER CHANGE 1:
under (USB charge) AND
((VAC plug) AND BATTERY SETS AND BCIAUTOAC = 1)

CHARGER CHANGE 2:
under (VAC charge) AND
((VAC unplug) OR BCIAUTOAC = 0)
AND BATTERY SETS AND
(Carkit OR USB charger) plug AND BCIAUTOUSB = 1)

(a) States Hierarchy/Priority Levels



(b) States Hierarchy/Priority Levels
The difference between ACPATHEN and USBPATHEN is done by a parallel arbiter process that forces ACPATHEN = 1 when VAC is plug and forces USBPATHEN = 1 when carkit OR USB charger is plug and NO VAC is plug.

(c) The hardware implementation is:

Detection	Origin	Subblock
SYSACTIV	POWER	Power state machine
VAC plug	BCIA	Analog comparator
VBUS plug	BCIA	Analog comparator
Carkit OR USB charger plug	USBA	USB precharge state machine
Battery open	BCIA	Analog comparator
Battery temperature in 3–43°C	MADC + BCID	MADC measure + digital comparator
Battery temperature in 2–50°C	MADC + BCID	MADC measure + digital comparator
VBAT<3.45 V	MADC + BCID	MADC measure + digital comparator
VBAT<2.90 V	MADC + BCID	MADC measure + digital comparator
VBAT<3.90 V	MADC + BCID	MADC measure + digital comparator
VBAT<3.95 V	MADC + BCID	MADC measure + digital comparator
ICHG<240 mA	MADC + BCID	MADC measure + digital comparator
ICHG<80 mA	MADC + BCID	MADC measure + digital comparator
VAC>6.5 V	BCIA	Analog comparator
VBUS>5.5 V	BCIA	Analog comparator
VBAT>4.55 V	BCIA	Analog comparator
4 sec timer	BCID	Digital timer
120 min timer	BCID	Digital timer
240 min timer	BCID	Digital timer

Action	Origin	Subblock
Constant current	BCIA	CC loop
Current reference	BCIA	DAC output
Constant volume	BCIA	CV loop
AC path	BCIA	Switches
USB path	BCIA	Switches
4 sec timer	BCID	Timer
120 min timer	BCID	Timer
240 min timer	BCID	Timer

BCI-008

5.4.11.1.2.1.1 Main Charge Software-Controlled Mode

In software-controlled mode, the external microcontroller (master) enables the main charge by forcing the BCIMDEN[4] LINCHEN bit to 1. The microcontroller selects the charging device by forcing the BCIMDEN[1] ACPATHEN bit to 1 for charging with an ac charger or by forcing the BCIMDEN[0] USBPATHEN bit to 1 for charging with the USB device. The BCIMDEN register is a read-only register, and the values of its fields are forced by writing to the BCIMDKEY register. The hardware forbids forcing ACPATHEN and USBPATHEN to 1 at the same time. The microcontroller monitors the charging through MADC measurements and automatic monitoring functions.

Battery overvoltage protection is enabled automatically when the LINCHEN bit is forced to 1. In this case, the voltage threshold is set to a value relative to a VBAT pin of the device equal to 4.55 V, which is typical for battery overvoltage. The software can disable this protection by using the monitoring function enable register, BCIMFEN. The BCIMFEN register is a read-only register, and the values of its fields are forced

by writing to the BCIMFKEY register. The watchdog is also enabled automatically when the LINCHEN bit is forced to 1. In this case, the delay is set to 4 seconds for the first start and to the last programmed value for other starts. The software can disable this protection by writing 0 to the BCIWD[2] WEN bit. The BCIWD register is a read-only register, and the values of its fields are forced by writing to the BCIWDKEY register.

During an ac or USB main charge, in software-controlled mode, an external microcontroller must monitor the battery and control the charge loop through the I^2C serial interface.

During a USB main charge, using the USB protocol, the microcontroller should detect the maximum charge current to be set.

In software-controlled mode, the user can enable monitoring functions. Monitoring of a function, when enabled, occurs every 50 msec. Table 5-35 lists the monitoring functions.

Table 5-35. Device Monitoring Functions

Register Field to Enable Monitoring Function	Description
VBATOVxEN	Battery overvoltage monitoring function enable. Four user settings are available (x can be from 1 to 4).
ACCHGOVEN	Ac charger overvoltage monitoring function enable
VBUSOVEN	VBUS overvoltage monitoring function enable
TBATORxEN	Battery temperature out-of-range monitoring function enable. Two temperature settings can be used (x can be 1 or 2).
ICHGEOCEN	Battery end-of-charge monitoring function enable
ICHGLOWEN	Battery charge current level monitoring function enable
ICHGHIGHEN	Battery overcurrent monitoring function enable
HSEN	Heat save function enable

5.4.11.1.2.1.2 Main Charge Automatic Mode

In automatic mode, an ac or USB charge starts automatically when the power-management system is in active mode (VBAT > 3.2 V, the SYSACTIV signal is forced to 1). In automatic mode, the analog hardware for an ac or USB main charge is automatically controlled and configured by the main charge FSM. The FSM directly controls the registers. The FSM selects the charging device by forcing the ACPATHEN and LINCHEN bits to 1 for charging with an ac charger, or by setting the USBPATHEN and LINCHEN bits to 1 for charging with the USB device.

If multiple charge sources are applied when in automatic mode, an arbitration scheme is used and the ac charge has priority for charge and precharge.

5.4.11.1.3 Pulsed Charge

Precharging stops automatically when the power-management system starts (the power state-machine is in active mode and the SYSACTIV signal is forced to 1). If power dissipation problems occur around the external components, pulsed charge with ac chargers is also supported. The external microcontroller enables the pulsed charge by setting the BCIMDEN[3] PWMEN bit to 1. The hardware forbids enabling the pulsed charge and the main charge at the same time.

A pulse-width modulation (PWM) signal controls the external PMOS transistors driven by ICTLAC1 and ICTLAC2 of the device. The frequency of the PWM signal is typically 1 Hz. The duty cycle of the 1-Hz PWM signal is set using the 10-bit field PWMDTYCY (BCIPWM1 and BCIPWM2 registers). The 1-bit PWM signal that can be read into the registers controls the external PMOS transistors driven by the ICTLAC1 and ICTLAC2 pins of the device.

This mode is supported for charging with ac chargers only. The ac charger device must limit the charge current. The battery charge current and the battery voltage are continuously monitored by the microcontroller through the MADC.

During a pulsed charge, the threshold for battery overvoltage or battery overtemperature automatic monitoring can be programmed. Battery overvoltage protection is enabled automatically when the PWMEN bit is forced to 1. In this case, the voltage threshold is set to a value relative to a VBAT pin of the device equal to 4.55 V, which is typical for battery overvoltage. The software can disable this protection using the BCIMFKEY register. The watchdog is also enabled automatically when the LINCHEN bit is forced to 1. In this case, the delay is set to 4 seconds. The software can disable this protection using the BCI watchdog key register BCIWDKEY.

During pulsed charge, in software-controlled mode, an external microcontroller must monitor the battery and control duty cycle through the I^2C serial interface.

5.4.11.1.4 CV Mode

The BCI supports CV mode, which starts automatically when there is no battery pack, a regulated ac charger is connected, and CVENAC = 1. The charging device outputs a constant voltage at the VBAT node. To start CV mode, the precharge analog hardware detects whether the battery pack is open and whether an ac charger is connected.

CV mode starts the ac overvoltage protection; CV mode is disabled for VAC > 6.5 V (typical).

The CV mode hardware implementation uses the main charge CV loop. In this mode, a 35-mA (typical) load is synched internally to stabilize the regulated VBAT voltage output, and a 47-μF (typical) external capacitor must be connected to the VBAT node.

When the battery pack is open and the ac charger is connected, the BCI is in one of three application states:

- State 1: The battery node VBAT is less than 3.2 V. The precharge FSM starts and enters precharge CV mode (if CVENACA = 1). In this mode, the precharge loop starts and regulates at 3.6 V (typical). When 3.2 V is achieved, the power-management system starts (the power state-machine changes from off to active mode). The VINTANA1, VINTANA2, and VINTDIG regulators are raised, the LDOOK signal is forced to 1 by the power state-machine, and the main charge FSM starts and enters CV mode. In this mode, the main charge CV control loop starts and regulates the battery node voltage at 4.0 V (typical). 1ms later, the power state-machine enters active mode. The SYSACTIV signal is forced to 1 by the power state-machine and the precharge slow constant current mode stops.
- State 2: The battery node VBAT is greater than 3.2 V and is in automatic charge mode. The main charge FSM enters CV mode. In this case, the CV mode hardware is already started, because the CV loop is already started.
- State 3: The battery node VBAT is greater than 3.2 V and is in software-control mode. A special CV function starts. This is the same function that starts in the CV mode used in the automatic charge mode FSM. In this case, the CV mode hardware is already started, because the CV loop is already started.

5.4.11.1.5 Accessory Supply Mode

The BCI can supply power to portable accessories without any of its inputs connected to the ac outlet or the USB outlet. This mode is enabled by forcing the BCIMDEN[2] ACCSUPEN bit to 1. In this mode, either the two external PMOS transistors driven by the ICTLAC1 and ICTLAC2 pins or the two PMOS transistors driven by the ICTLUSB1 and ICTLUSB2 pins are tied to 0, and they connect the battery voltage to the device plugged into the ac outlet or the USB outlet. Before entering this mode, an external microcontroller must detect the accessory device plugged into the ac connector or the USB connector.

5.4.11.1.6 BCI Interrupts

There are two identical interrupt generation modules in the secondary interrupt handler (SIH). The SIH processes synchronous interrupt requests to be used independently in a biprocessor environment. Each module generates an interrupt (BCI_SIH_INT1_n and BCI_SIH_INT2_n). Each module controls its own synchronous interrupt request line and has its own interrupt mask and interrupt status register. For details about the SIH, see Chapter 4, *Interrupts*.

The user can enable or disable interrupts for the following transitions:

- Battery status (BATSTS)

- Battery temperature out of range (TBATOR)
- Battery current end-of-charge (ICHGEOC)
- Battery charge low and high detection (ICHGLOW, ICHGHIGH)
- Ac charger overvoltage protection (ACCHGOV)
- USB charger overvoltage protection (VBUSOV)
- Timer overflow (TMOVF)
- Watchdog overflow (WOVF)
- VBAT overvoltage (VBATOV)
- VBAT level (VBATLVL)
- VBUS overvoltage (VBUSOV)
- Ac charger overvoltage (ACCHGOV)

The interrupt mask registers (BCIIMR1A, BCIIMR1B, BCIIMR2A, and BCIIMR2B) let the user unmask the expected BCI transition event to generate an interrupt request. To set an interrupt on any of these transitions, the corresponding bit must be set to 0.

The interrupt edge-detection registers (BCIEDR1, BCIEDR2, and BCIEDR3) let the user define for each transition event the edge expected to trigger an interrupt request. Detection can be on the rising edge, on the falling edge, or on both edges.

This interrupt status registers (BCIISR1A, BCIISR1B, BCIISR2A, and BCIISR2B) indicate the current status of the interrupt signals BCI_INT1_n and BCI_INT2_n. These read/write registers determine which monitoring function triggered an interrupt request. Each bit is cleared by default by reading the interrupt service routine (ISR) when the BCISIHCTRL[2] COR bit is set to 1. Each bit can also be cleared by writing 1 on the corresponding bit of the interrupt status register; writing 0 has no effect.

The BCI control register BCISIHCTRL lets the user enable an incoming pending event during software interrupt latency by writing 0 to the BCISIHCTRL[1] PENDDIS bit. Writing 1 in the PENDDIS bit disables the pending feature. Exclusivity can be enabled by writing 1 to the BCISIHCTRL[0] EXCLEN bit and disabled by clearing the EXCLEN bit to 0. The ISR can be configured to clear the interrupt on a read access or a write access by writing 1 or 0, respectively, to the COR bit.

5.4.11.1.7 Timers

Two registers in the BCI set the timers for the state transitions, as seen on the FSMs. The timers can be started and set for default thresholds of 4 seconds, 120 minutes, and 240 minutes. The BCITIMER1 and BCITIMER2 registers are used to set these values (see Table 5-36).

Table 5-36. Programming the BCITIMER2 Register

BCTIMER2[5:4]		**Time (min)**
1	1	256
1	0	239
0	1	222
0	0	205
BCTIMER2[3:2]		**Time (min)**
1	1	128
1	0	119
0	1	111
0	0	102
BCTIMER2[1:0]		**Time (sec)**
1	1	4.40
1	0	4.00
0	1	3.60
0	0	3.20

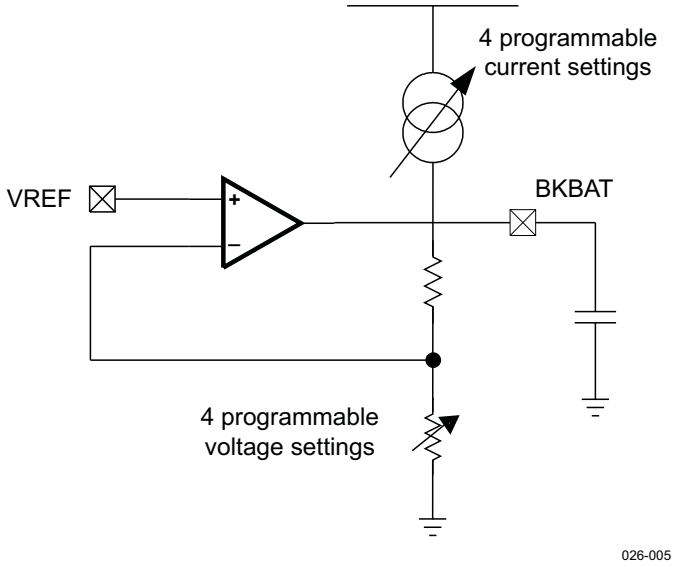
5.4.11.2 Backup Battery Functional Description

This section explains the backup battery charging procedure. It also describes backup battery switching options in the event of the main battery going below 2.7 V. In backup mode, the system is powered only with the backup battery and maintains only the VBRTC supply for the RTC.

5.4.11.2.1 Backup Battery Charger

Figure 5-17 shows the backup battery charger.

Figure 5-17. Backup Battery Charger



The backup battery is rechargeable and can be recharged from the main battery. The backup battery can be charged by setting the BB_CFG[4] BBCHEN bit to 1. Charging starts when two conditions are met:

- Main battery voltage > backup battery voltage
- Main battery > 3.2 V

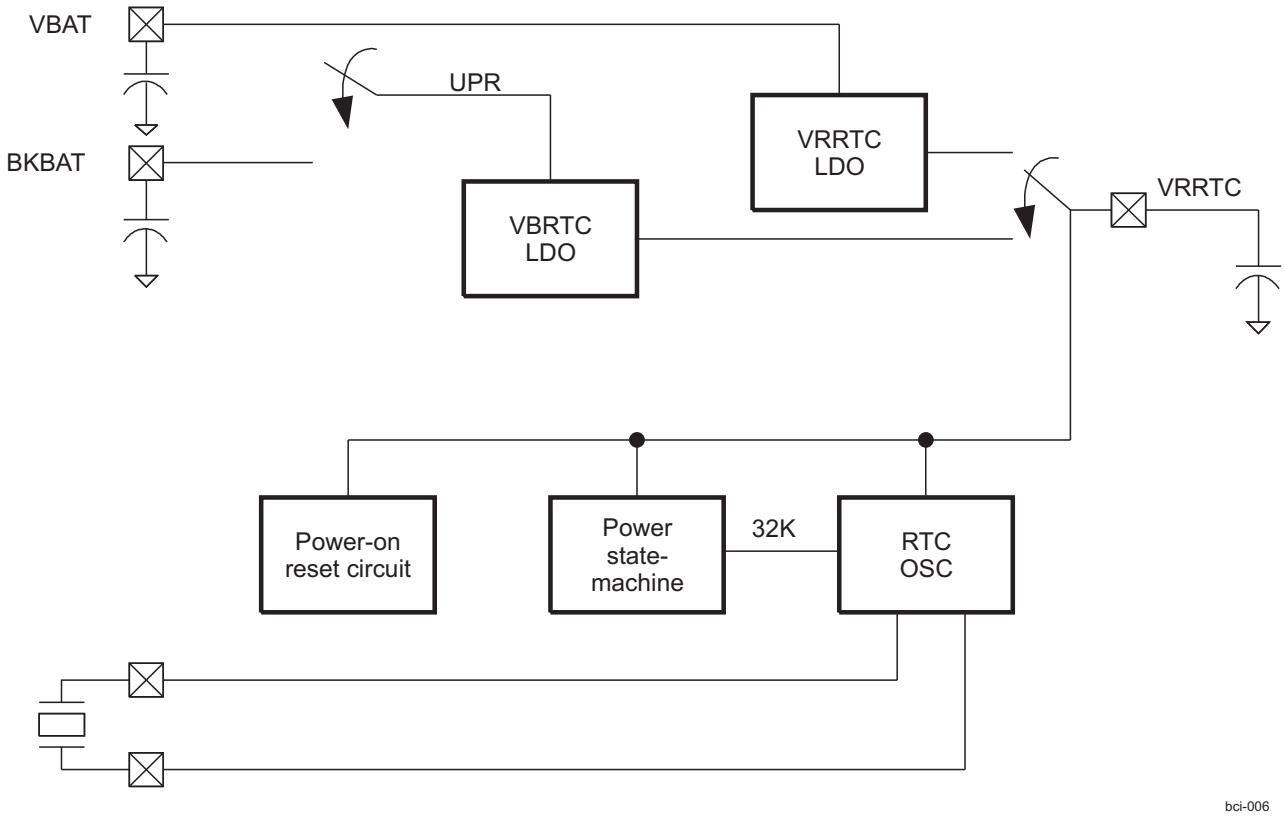
The comparators of the backup battery system (BBS) give the two thresholds of the backup battery charge startup. The voltage can be set with the BB_CFG[3:2] BBSEL bit field; this gives the end-of-charge threshold. The current can be set with the BB_CFG[1:0] BBISEL bit field; this gives the charge current for the charger. Charge monitoring is automatic when the block is enabled. Backup battery voltage can also be monitored by the MADC, which can indicate to software when the backup battery is charged and can disable the charger (thus reducing IDDQ). The MADC can also monitor backup battery voltage if it is required to charge to a voltage other than the four programmable values when the value is lower than the maximum charge value available.

In the boot sequence for the device, going from wait-on to active mode, the backup battery charging sequence must be initiated by setting the BB_CFG[4] BBCHEN bit to 1.

5.4.11.2.2 VRRTC and VBRTC Regulators

The voltage regulator VRRTC is a programmable low dropout (LDO) linear voltage regulator supplying (1.5 V) the embedded RTC (32.768-kHz oscillator). VRRTC is also the supply voltage of the power-management digital state-machine. The VBRTC is supplied from the uninterrupted power rail (UPR) line, which is connected to the main battery through a clamp circuit or to the backup battery, depending on the battery states. The VRRTC level is active while a valid energy source is present. The VRRTC line is supplied by the VRRTC LDO when VBAT > 2.7 V, and by the VBRTC circuit when in backup mode (see Figure 5-18).

Figure 5-18. Blocks in the RTC Domain



5.4.11.2.3 Backup Battery Switch Control

The backup battery switch uses various comparators to control switching from the main battery to the backup battery to generate a UPR. This supplies the circuitry that generates the supply voltage for the RTC system, the security registers, and the power-on reset (POR) system. The output levels of the comparators also provide information about the state of charge to the power state-machine during the power-up and power-down sequences. The following conditions are required for the UPR to be connected to the main battery:

VBAT > 2.85 V or (VBAT > 2.1 V and VBAT > backup battery voltage [BKBAT])

Otherwise, the UPR is connected to the backup battery if it contains a valid supply.

If no backup battery is used in the system, connect BKBAT to ground; the UPR depends only on the main battery.

5.5 Reset and Power-Management Programming Model

This section includes the information needed to program and write the scripts for the device.

The device has a fixed memory sequence used during bootup (see Table 5-37).

The device has a memory of 64 32-bit sequence words that can be used to program the device. Each 32-bit sequence word is divided into four 8-bit words. Each sequence word begins with a 16-bit ([31:16]) power word, 8 bits ([15:8]) for the delay, and 8 bits ([7:0]) for the next address. The power word can have broadcast or singular message format. The fields for broadcast and singular messages are listed in Table 5-16 and Table 5-17, respectively. The formats for the delay word and the next address are shown in Table 5-27 and Table 5-28, respectively.

The I^2C bus is used to write each word of the sequence. The address and the data are written to the MEMORY_ADDRESS and MEMORY_DATA registers, respectively.

NOTE: The value of MEMORY_ADDRESS is auto-incremented when there is a read/write to the MEMORY_DATA register.

5.5.1 Sequencing

This section explains how to configure the device register to initialize the power features or to configure power-management optimization with voltage scaling. Figure 5-19 indicates the steps for programming the device.

Table 5-37 and Table 5-39 through Table 5-41 show the power-up sequence for each mode in the device. The later sections show the procedure to be used for programming the memory words. Table 5-38 lists the memory structure (binary) for C027 slave mode.

Table 5-37. Power-Up Sequence for MC027S (Master_C027 Mode)(1)

Sequence MC027S	MEM ADD	Memory Word	CLK32K	Minimum Delay Required by Design (2) (µs)	NEXT_ ADD
WAIT-ON 2 PRESENCE	0	Active broadcast for all PR (MAIN_REF)	36	1099	1[1]
WAIT-ON 2 PRESENCE	1	Enable PP VINTDIG and VINTANA1 (Type 1).	20	610	2
WAIT-ON 2 PRESENCE	2	Enable PP VUSB3V1.	20	610	3
WAIT-ON 2 PRESENCE	3	Enable PP VINTANA2.	36	1099	63
PRESENCE 2 ACTIVE	4	Enable Type 2 REGEN.	19	580	5
PRESENCE 2 ACTIVE	5	Enable Type 3 VAUX2, and VIO (VIO CLK3M, then VIO)[1].	32	977	6
PRESENCE 2 ACTIVE	6	Enable Type 4 VDD1 (VDD1 CLK3M, then VDD1), and VAUX2.	55	1709	7
PRESENCE 2 ACTIVE	7	Enable Type 5 VDD2 (VDD2 CLK3M, then VDD2) and HFCLK_EN.	71	2197	8[2]
PRESENCE 2 ACTIVE	8	ACTIVE state broadcast for all PP (VPLL1)	4	122	9
PRESENCE 2 ACTIVE	9	Enable RC CLK32K_OUT.	2	61	10
PRESENCE 2 ACTIVE	10	Enable RC SYSEN and release TRITON_ RESET_NA (Type 6).	94	2930	11
PRESENCE 2 ACTIVE	11	Enable RC HFCLK_OUT.	2	61	12
PRESENCE 2 ACTIVE	12	ACTIVE state broadcast for all subsystems (nRESPWON)	2	61	63
ACTIVE 2 WAIT-ON	13	System reset (Triton force SYSEN, nRESPWON, and stop HFCLK).	40	1221	14
ACTIVE 2 WAIT-ON	14	OFF state broadcast for all RES_GRP	110	3418	63[1]

(1) CLK3M starts 1.1 ms after the clock enable signal, and VIO is active to its defined level 1 ms after the clock is active.
(2) For more information about design delays, see the device data manual.

1: 32K clock cycles
2: 3M clock cycles

Table 5-38. Memory Structure (Binary) for MC027S Mode

MEM ADD	Sequence MC027S			
0	00011000	01111110	00100011	00000001
1	00010010	00011110	00010110	00000010
2	00000001	00111110	00010110	00000011
3	00000000	11001110	00100011	00111111
4	00011110	00101110	00010101	00000101

Table 5-38. Memory Structure (Binary) for MC027S Mode (continued)

MEM ADD	Sequence MC027S			
5	00011110	00111110	00100010	00000110
6	00011110	01001110	00110000	00000111
7	00011110	01011110	00110010	00001000
8	00010010	01111110	00000100	00001001
9	00000001	10101110	00000010	00001010
10	00011110	01101110	00110101	00001011
11	00000001	10011110	00000010	00001100
12	00011110	01111110	00000010	00111111
13	00010100	01110000	00100100	00001110
14	00011110	01110000	00110111	00111111

Table 5-39. Power-Up Sequence for MC027 Mode (Master C027)

Sequence MC027S	MEM ADD	Memory Word	CLK32K	Minimum Delay Required by Design (1) (µs)	NEXT_ ADD
WAIT-ON 2 PRESENCE	0	Active broadcast for all PR (MAIN_REF)	36	1099	1[1]
WAIT-ON 2 PRESENCE	1	Enable PP VINTDIG and VINTANA1 (Type 1).	20	610	2
WAIT-ON 2 PRESENCE	2	Enable PP VUSB3V1.	20	610	3
WAIT-ON 2 PRESENCE	3	Enable PP VINTANA2.	36	1099	63
PRESENCE 2 ACTIVE	4	Enable PP REGEN, VIO (VIO CLK3M, then VIO) (Type 2).	51	1587	6
PRESENCE 2 ACTIVE	5	Not used	32	977	6[2]
PRESENCE 2 ACTIVE	6	Enable PP VDD1 (VDD1 CLK3M, then VDD1) (Type 4).	55	1709	7
PRESENCE 2 ACTIVE	7	Enable RC HFCLK_EN (Type 5).	36	1099	8
PRESENCE 2 ACTIVE	8	ACTIVE state broadcast for all PP (VPLL1)	4	122	9
PRESENCE 2 ACTIVE	9	Enable RC CLK32K_OUT.	20	610	10
PRESENCE 2 ACTIVE	10	Enable RC SYSEN and release TRITON_ RESET_NA (Type 6).	110	3418	11
PRESENCE 2 ACTIVE	11	Enable RC HFCLK_OUT.	2	61	12
PRESENCE 2 ACTIVE	12	ACTIVE state broadcast for all subsystems (nRESPWON)	2	61	63
ACTIVE 2 WAIT-ON	13	System reset (Triton force SysActiv, nRESPWON and stop HFCLK)	40	1221	14
ACTIVE 2 WAIT-ON	14	OFF state broadcast for all RES_GRP	110	3418	63[1]

(1) For more information about design delays, see the device data manual.

1: 32K clock cycles
2: 3M clock cycles

Table 5-40. Power-Up Sequence for MC021 Mode (Master C021)

Sequence MC027S	MEM ADD	Memory Word	CLK32K	Minimum Delay Required by Design (1) (µs)	NEXT_ ADD
WAIT-ON 2 PRESENCE	0	ACTIVE broadcast for all PR (MAIN_REF)	36	1099	1
WAIT-ON 2 PRESENCE	1	Enable PP VINTDIG and VINTANA1 (Type 1).	20	610	2
WAIT-ON 2 PRESENCE	2	Enable PP VUSB3V1.	36	1098	3
WAIT-ON 2 PRESENCE	3	Enable PP VINTANA2.	36	1099	63
PRESENCE 2 ACTIVE	4	Enable PP EXT_REGEN, VIO (VIO CLK3M, then VIO) (Type 2).	74	2686	5
PRESENCE 2 ACTIVE	5	Enable PP VPLL1, VDD2 (VDD2 CLK3M, then VDD2), and RC HFCLK_EN (Type 3).	34	1099	6
PRESENCE 2 ACTIVE	6	Enable PP VDD1 (VDD1 CLK3M, then VDD1) (Type 4).	71	2197	9
PRESENCE 2 ACTIVE	7	Not used	71	2197	8
PRESENCE 2 ACTIVE	8	Not used	4	122	9
PRESENCE 2 ACTIVE	9	Enable RC CLK32K_OUT.	2	61	10

(1) For more information about design delays, see the device data manual.

Table 5-40. Power-Up Sequence for MC021 Mode (Master C021) (continued)

Sequence MC027S	MEM ADD	Memory Word	CLK32K	Minimum Delay Required by Design [1] (µs)	NEXT_ ADD
PRESENCE 2 ACTIVE	10	Enable RC SYSEN and release TRITON_ RESET_NA (Type 6).	36	1099	11
PRESENCE 2 ACTIVE	11	Enable RC HFCLK_OUT.	2	61	12
PRESENCE 2 ACTIVE	12	ACTIVE state broadcast for all subsystems (nRESPWON)	2	61	63
ACTIVE 2 WAIT-ON	13	System reset (Triton force SYSEN, nRESPWON, and stop HFCLK)	40	1221	14
ACTIVE 2 WAIT-ON	14	OFF state broadcast for all RES_GRP	110	3418	63

Table 5-41. Power-Up Sequence for SC021 Mode (Slave C021)

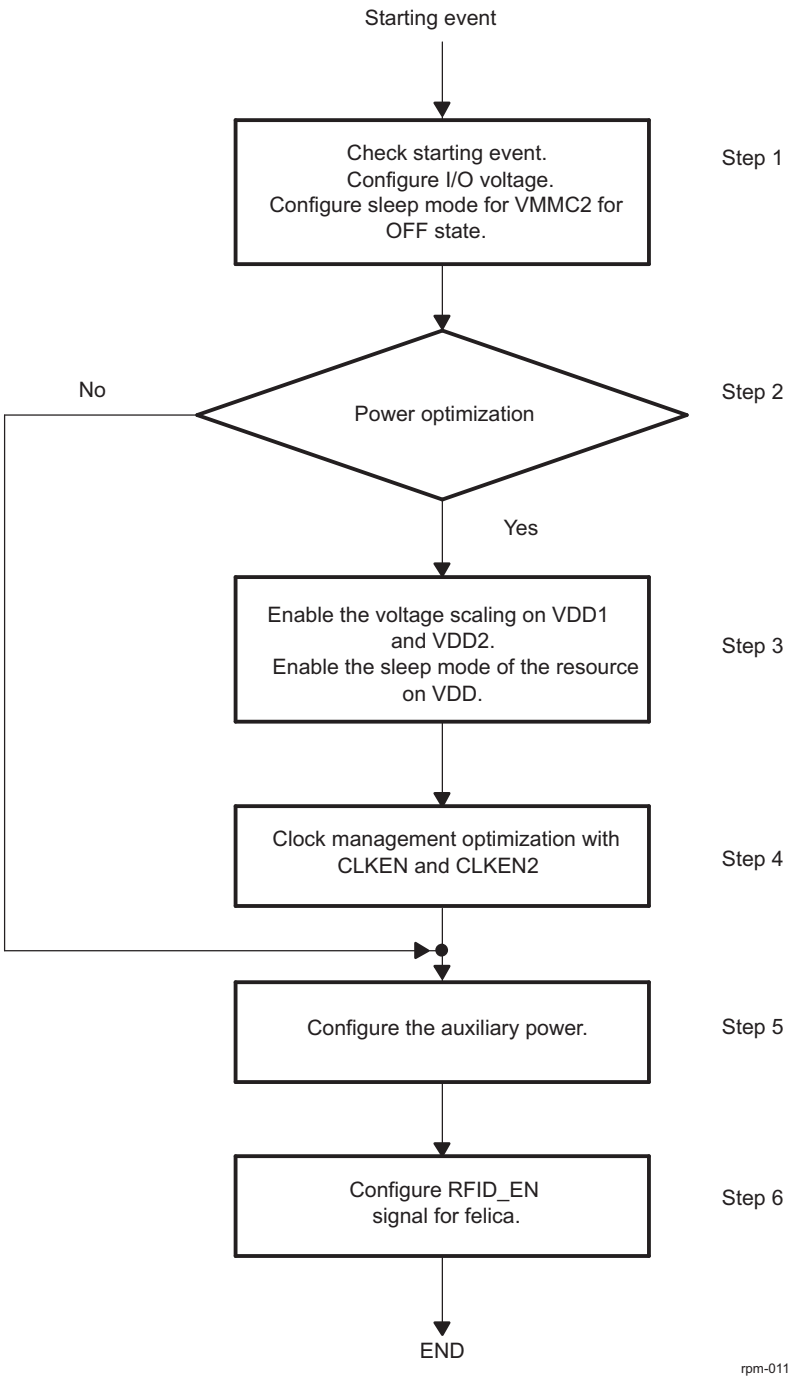
Sequence MC027S	MEM ADD	Memory Word	CLK32K	Minimum Delay Required by Design [1] (µs)	NEXT_ ADD
WAIT-ON 2 PRESENCE	0	ACTIVE broadcast for all PR (MAIN_REF)	36	1099	1
WAIT-ON 2 PRESENCE	1	Enable PP VINTDIG and VINTANA1 (Type 1).	20	610	2
WAIT-ON 2 PRESENCE	2	Enable PP VUSB3V1.	20	610	3
WAIT-ON 2 PRESENCE	3	Enable PP VINTANA2.	36	1099	63
PRESENCE 2 ACTIVE	4	Enable PP EXT_REGEN, VIO (VIO CLK3M, then VIO) (Type 2).	94	2930	5
PRESENCE 2 ACTIVE	5	Enable PP VPLL1, VDD2 (VDD2 CLK3M, then VDD2), and RC HFCLK_EN (Type 3).	34	1099	6
PRESENCE 2 ACTIVE	6	Enable PP VDD1 (VDD1 CLK3M, then VDD1) (Type 4).	71	2197	9
PRESENCE 2 ACTIVE	7	Not used	71	2197	8
PRESENCE 2 ACTIVE	8	Not used	4	122	9
PRESENCE 2 ACTIVE	9	Enable RC CLK32K_OUT.	2	61	10
PRESENCE 2 ACTIVE	10	Enable RC SYSEN and release TRITON_ RESET_NA (Type 6).	36	1099	11
PRESENCE 2 ACTIVE	11	Enable RC HFCLK_OUT.	2	61	12
PRESENCE 2 ACTIVE	12	ACTIVE state broadcast for all subsystems (nRESPWON)	2	61	63
ACTIVE 2 WAIT-ON [2]	13	System reset (Triton force SYSEN, nRESPWON, and stop HFCLK)	40	1221	14
ACTIVE 2 WAIT-ON [2]	14	OFF state broadcast for all RES_GRP	110	3418	63

(1) For more information about design delays, see the device data manual.

(2) ACTIVE 2 WAIT-ON delays can be reduced to 0 (keep only state-machine transition delay, no timer delay) by software after a first boot: VIO must be ON and switch-off delays must be programmed to their minimum values

Figure 5-19 is the sequencing flow chart.

Figure 5-19. Sequencing Flow Chart



1. Check the starting origin:
   (a) If an interrupt is coming, read the interrupt status register.
   (b) If there is an interrupt on the power block, read the STS_P123_STATE status register of power to determine the origin of the starting of the system.
   (c) Read the interrupt source in the corresponding block and clear it.
   (d) Read the STS_BOOT register to determine whether an event reset some part of the device.
2. Disable emulation and configure I/O voltage:
   (a) If no emulation is required, VDD2 can be shut down.

(b) To shut down the VDD2, remove the VDD2 from the group and write the VDD2_DEV_GRP register with the value 0x0.
(c) If VIO_VSEL must be set to 1.85 V, set the value to 0x1.
(d) Configure sleep mode on VMMC2 for the system off mode: Set the VMMC2_REMAP OFF_STATE bit field to 0x8.1.

3. Enable the system without power optimization:
   (a) If no power-management optimization is required (no DVFS or sleep management), go to Step 5 to enable the required LDOs for peripherals; otherwise, go to Step 4.
4. Enable system with power optimization:
   (a) Enable voltage scaling on VDD1: Set the values of VROOF and VFLOOR in the VDD1_VROOF and VDD1_VFLOOR registers.
   (b) Enable VMODE: Set the bit VDD1_VMODE_CFG = 0x1. When VMODE1 signal goes low, the voltage goes low.
   (c) Enable the voltage scaling on VDD2: Set the values of VROOF and VFLOOR in the VDD2_VROOF and VDD2_VFLOOR registers.
   (d) Enable VMODE: Set the bit VDD2_VMODE_CFG = 0x1. When the VMODE2 signal goes low, the voltage goes low.
   (e) Enable the SLEEP of resource on DC/DC1: Set the P1_SW_EVENTS[3] LVL_WAKEUP bit. This lets VDD1 go to sleep mode when the nSLEEP1 pin of the device goes low.
5. Enable clock-management optimization:
   (a) Because the CLKEN resource signal is associated with P1, P2, and P3, when the CLKREQ, nSLEEP1, and nSLEEP2 signals go low, the CLKEN resource goes low. By default, CLKREQ is not considered; thus, CLKEN cannot go to active or sleep mode. To let the CLKEN resource go to active or sleep mode, the P3_SW_EVENTS[3] LVL_WAKEUP bit must be set to 1.
   (b) CLKEN2 is controlled by the MISC_CFG CLKEN2_CFG bit. If CLKEN2_CFG = 0, CLKEN2_ENABLE is a toggle bit. If CLKEN2_ENABLE = 0, CLKEN2 is disabled; if it is 1, CLKEN2 is enabled. If CLKEN2_CFG = 1 and CLKEN2_ENABLE = 0, CLKEN2 is low; if CLKEN2_ENABLE = 1, CLKEN2 is high.
6. Configure the auxiliary power (VAUX2 is shown here as an example):
   (a) Set VAUX2 voltage: Set the VAUX2_DEDICATED[3;0] VSEL bit field.
   (b) Set the state of the LDO when P3 is in SLEEP: Set the VAUX2_REMAP[3:0] SLEEP_STATE bit field to 0x0. This shuts down the LDO when an input signal for P3 goes high.
   (c) Map VAUX2 for a processor: Set the VAUX2_DEV_GRP[7:5] DEV_GRP bit field to 0x4. The 8-bit register value is 0x80.
   (d) Put resource VAUX2 to SLEEP: VAUX2 ID is 0x02. Write the command to be sent to the resource in the PB_WORD_MSB and PB_WORD_LSB registers. The 16-bit power bus word is:

   DEV_GRP[15:13] 0x4

   MT[12] 0x1

   Res_ID[4:11] 0x1

   STATE[0:3] 0x8

   The command is sent when the LSB is written.

5.5.2 Programming Example for Assigning a Resource to a Processor

Writing the value 0x20 to the VUSB1v5_DEV_GRP register sets DEV_GRP to 001, indicating that the resource is assigned to P1.

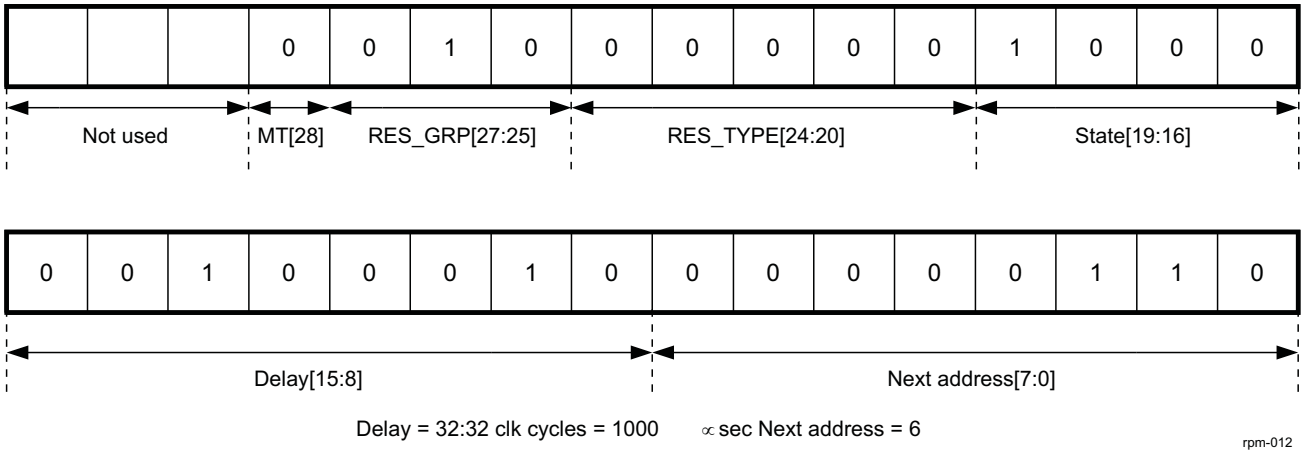
5.5.3 Programming Example for Skipping an Address

To bypass a word in memory, the NEXT_ADDRESS bits ([7:0] in a sequence word) must be written with the address to be executed next. An example follows.

The sequence to be executed is shown in Figure 5-20. In this sequence, the memory address 6 is skipped. This means that the sequence must skip from memory address 5 to memory address 7.

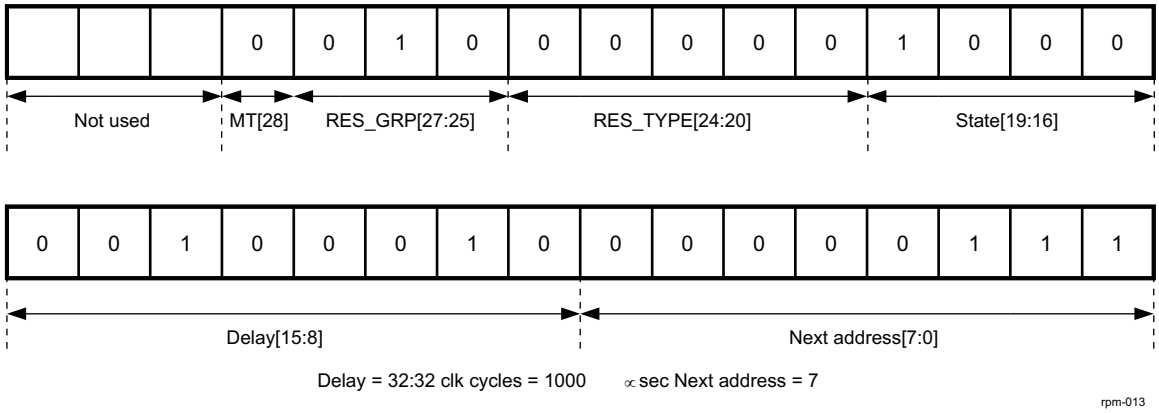
The original 32-bit word is shown in Figure 5-20.

Figure 5-20. Skipping an Address—Original Address = 6



To change the sequential execution and skip address 7, modify the NEXT_ ADDRESS field of sequence word 5. The new 32-bit sequence word is shown in Figure 5-21.

Figure 5-21. Skipping an Address—Modified Value = 7



The values are written directly by the I^2C registers.

The MEMORY_ADDRESS register selects the 8-bit word of a sequence word (one of the 64 memories in the device) to be changed. The first 6 bits (MSB) address a specific memory (one of the 64), and the last 2 bits (LSB) define which 8-bit word (in that particular memory) is being accessed.

Figure 5-21 shows sequence word 5. To set NEXT_ADDRESS to be sequence word 7 (instead of 6 as shown in Figure 5-20), 0x00010111 is put into the MEMORY_ADDRESS register; that selects NEXT_ADDRESS to be written to. The first 6 bits define sequence word 5 (000101), and the last 2 bits (11) select NEXT_ADDRESS (in each 32-bit sequence word, the last 8-bit word is NEXT_ADDRESS; with four 8-bit words, the last is defined by 0x11).

When the MEMORY_ADDRESS register is written to, the device writes the 8 bits in the MEMORY_DATA register to the selected 8-bit word in the selected sequence word (defined by what was put into MEMORY_ADDRESS). For sequence word 7 to execute after sequence word 5, the NEXT_ADDRESS value (8 bits wide) in sequence word 5 is 0x00000111 (value = 7).

Table 5-42 shows this sequence.

Table 5-42. Memory Skip

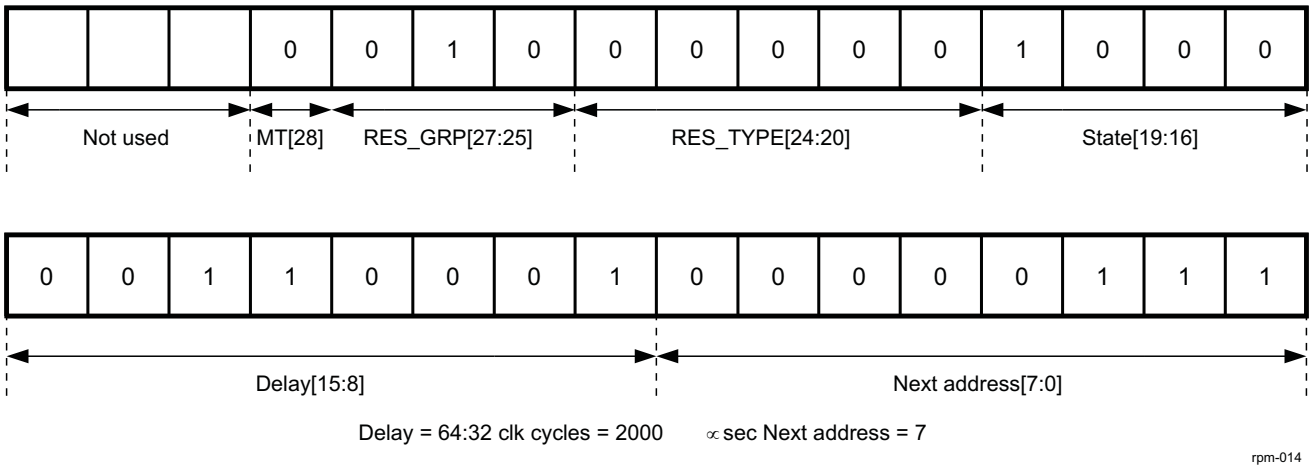
Sequence MC027S	MEM ADD	Memory Word	Delay (μs)	NEXT_ ADD
WAIT-ON-to-ACTIVE	5	Enable PR group 5 (CHECK VBAT_presence).	1000	7
WAIT-ON-to-ACTIVE	7	Enable PP group 4 (VAUX2, DC/DC_3M_CLK_EN).	1200	8

5.5.4 Programming Example for Adding a Delay

Because the delay field of the memory sequences is read-only, spare words are used to add a delay between words. To do this, the next address executed should be a spare word instead of the next sequential word. The spare word executed should have the same command as the next sequential word except with the required delay and the next address changed accordingly.

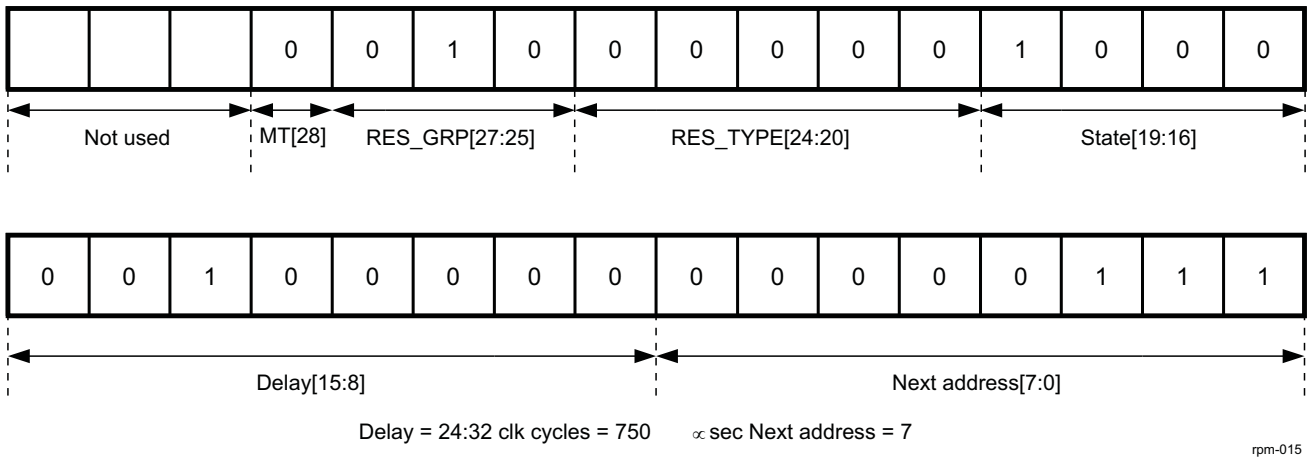
The next address of the previous word should be changed as shown in Section 5.5.3, *Programming Example for Skipping an Address*. The original word with a delay of 2000 μs has the format shown in Figure 5-22.

Figure 5-22. Adding a Delay—Original Delay = 2000 μs



The spare word written for changing the delay has the format shown in Figure 5-23.

Figure 5-23. Adding a Delay—Modified Delay = 750 μs



The values are written directly by the I^2C registers.

The MEMORY_ADDRESS register selects the memory location to be updated. The memory address to be changed in the previous example is 0x10100010. This address is calculated using Table 5-26. The 6 MSBs correspond to the address 40 and the 2 LSBs correspond to the delay address field.

The MEMORY_DATA register is used to write the new delay value at the selected location. The new delay value selected in the previous example corresponds to the binary value of 24 (24 32-kHz clock cycles delayed = 750 μs; see Table 5-38. The corresponding value to be written in the delay register is 0x00 100000.

The next address value in the spare word is written as shown in Section 5.5.3, *Programming Example for Skipping an Address*. If the next address value is 63, it indicates termination of the sequence.

Table 5-43 lists this sequence. The delay between REGEN and VMMC2, VAUX4, VPLL2, and VAUX2 is changed from 2000 μs to 750 μs.

Table 5-43. Memory Delay Modification

Sequence	MEM ADD	Memory Word	Delay(μs)	NEXT ADD
WAIT-ON-to-ACTIVE	0	Enable PR group 1 (LBG).	600	1
WAIT-ON-to-ACTIVE	1	Enable PR group 2 (MBG in FAST MODE).	60	2
WAIT-ON-to-ACTIVE	2	Enable PR group 3 (BIAS).	600	3
WAIT-ON-to-ACTIVE	3	Enable PR group 4 (CHECK VBAT_LEVEL and Thermal_Sense).	1000	4
WAIT-ON-to-ACTIVE	4	Enable PP group 1 (device Internal LDOs: VINTDIG, VINTANA1, and VINTANA2).	600	5
WAIT-ON-to-ACTIVE	5	Enable PR group 5 (CHECK VBAT_presence).	1000	43
WAIT-ON-to-ACTIVE	7	Enable PP group 4 (VAUX2, DC/DC_3M_CLK_EN).	1200	8
WAIT-ON-to-ACTIVE	8	Enable PP group 5 (Enable VIO DC/DC).	1000	9
WAIT-ON-to-ACTIVE	9	Enable PP group 6 (Enable DC/DC1 and HFCLK_EN).	1000	10
WAIT-ON-to-ACTIVE	10	Enable PP group 6 (Enable VPLL1).	100	11
WAIT-ON-to-ACTIVE	11	PR ACTIVE broadcast (device MBG in ACTIVE accurate mode)	100	12
WAIT-ON-to-ACTIVE	12	Enable RC group 1 (SYSEN).	2000	13
WAIT-ON-to-ACTIVE	13	Enable RC group 2 (HFCLK_OUT).	64	14
WAIT-ON-to-ACTIVE	14	ACTIVE state broadcast for all subsystems (nRESPWRON)	64	63
ACTIVE-to-SLEEP	15	Clock management DISABLE (device disables the clock function, CLK_EN low)	64	16
ACTIVE-to-SLEEP	16	SLEEP BROADCAST for PP	64	17
ACTIVE-to-SLEEP	17	SLEEP BROADCAST for PR	64	18
ACTIVE-to-SLEEP	18	SLEEP state broadcast for all subsystems	64	63
		...		
SPARE	43	Enable PP group 3 (EXT_REGEN).	750	7
	44	Spare word	0	63
	....	Spare word	0	63
	61	Spare word	0	63
	62	Spare word	0	63
	63	End of any sequence	0	63

5.5.5 Device Power-Down Registers

This section describes the power-down registers for each module in the device. The power-down registers can be programmed for power consumption. For details about register information, see the individual chapters. Table 5-44 lists the status (on/off) of the internal LDOs of the device in three states of the device (BACKUP, WAIT-ON, and ACTIVE). The resources not shown in ON state can be turned on during the power-on sequence or controlled by software.

Table 5-44. Internal LDO States

T2 Use Cases	VBRTC (~1.3V)	VRRTC	VIO (1.85V)	VINTDIG (1.5V)	VINTANA1 (1.5V)	VINTANA2 (2.75V)	VPRECH	VDD1 (2430)	VDD2 (N3G)	VSIM	VMIC1 (MIC)	VAUX2 (LCD)	VMMC1 (MMC)	VPLL1 (C027S)	VUSB_3P1V	VUSB_1P8V	VUSB_1P5V	VUSB-CP
BACKUP	•						√											
WAIT-ON	•	•					√											
ACTIVE	•	•	•	•	•	•	√											

√ VPRECH is on in any mode if there is a charger or a USB plug on T2; otherwise, this regulator is in power down.

• Resource is on in the specified mode.
Resource is powered down in the specified mode

5.5.5.1 Power-Down Registers for INTERFACE_SC Module

- GPIO
  Writing 0 to the GPIO_CTRL[2] GPIO_ON bit powers down the GPIO.
- GP bank register
  Writing 0 to the GPBR1[4] DEFAULT_MADC_CLK_EN bit lets the MADC clock be based on the value in the CFG_BOOT register. If DEFAULT_MADC_CLK_EN is set to 1 (the default value), the MADC clock equals HFCLK divided by 26, and the clock is always on, even when there is no request for the MADC clock. Because this can lead to undesired current drain, it may be necessary to set DEFAULT_MADC_CLK_EN to 0 (the MADC clock follows the CFG_BOOT register) to reduce current consumption while in low-power states.
  Writing 0 to the GPBR1[3] PWM1_ENABLE bit disables the PWM1 output.
  Writing 0 to the GPBR1[2] PWM0_ENABLE bit disables the PWM0 output.

5.5.5.2 Power-Down Registers for AUXILIARY_SC Module

- KEYPAD
  Writing 0 to the KEYP_CTRL_REG[6] KBD_ON bit powers down the keypad module.
- MADC
  Writing 0 to the CTRL1[0] MADCON bit powers down the MADC.
- Battery-control interface (BCI)
  Writing a correct EKEY value to the BCIMDKEY register disables the linear charge mode, pulsed charge mode, accessory supply mode, AC path, and USB path. This powers down the BCI.
  Similarly, writing a correct MFKEY value to the BCMFKEY register disables the monitoring functions of the BCI and powers down the module.

The BOOT_BCI[0] BCIAUTOAC, BOOT_BCI[1] BCIAUTOUSB, and BOOT_BCI[2] CVENAC bits in the backup domain should also be forced to 0.

- LED

  Control modes of LED operation

  Writing 0 to the LEDEN[0] LEDAON bit disables LEDA on the device. Writing 0 to the LEDEN[1] LEDBON bit disables LEDB on the device.

  Writing 0 to the LEDEN[4] LEDAPWM bit disables PWM for LEDA on the device. Writing 0 to the LEDEN[5] LEDBPWM bit disables PWM for LEDB on the device.

5.5.5.3 Power-Down Registers for the AUDIO_SC Module (TPS65930 Only)

Writing 0 to the CODEC_MODE[1] CODECPDZ bit powers down the audio codec.

- Audio/voice digital filter power control

  Writing 0 to the OPTION[7] ARXR2_EN bit disables the second right audio receiver. Writing 0 to the OPTION[6] ARXL2_EN bit disables the second left audio receiver.

  Writing 0 to the OPTION[5] ARXR1_EN bit disables the first right audio receiver. Writing 0 to the OPTION[4] ARXL1_VRX_EN bit disables the first left audio receiver. The field ARXL1_VRX_EN can also be used for voice receiver (see AUDIO register details for more information).

  Writing 0 to the OPTION[3] ATXR2_VTXR_EN bit disables the second right audio transmitter. Writing 0 to the OPTION[2] ATXL2_VTXL_EN bit disables the second left audio transmitter. The ATXR2_VTXR_EN and ATXL2_VTXL_EN bit fields can also be used as a voice transmitter.

  Writing 0 to the OPTION[1] ATXR1_EN bit disables the first right audio transmitter. Writing 0 to the OPTION[0] ATXL2_EN bit disables the second left audio transmitter.
- Audio interface

  Writing 1 to the AUDIO_IF[2] AIF_TRI_EN bit puts the output pins of the voice interface in high impedance state. Writing 0 to the AUDIO_IF[0] AIF_EN bit disables the audio serial interface on the device.
- Microphone bias and analog Mic amplifier power control

  Writing 0 to the MICBIAS_CTL[0] MICBIAS1EN bit disables the main microphone bias.
- Analog microphone left control register

  Writing 0 to the ANAMICL[4] MICAMPL_EN bit powers down the left microphone amplifier. Writing 0 to the ANAMICL[3] CKMIC_EN bit disables the carkit microphone input. Writing 0 to the ANAMICL[2] AUXL_EN bit disables the left auxiliary input. Writing 0 to the ANAMICL[0] MAINMIC_EN bit disables the main microphone input.
- Analog microphone right control register

  Writing 0 to the ANAMICR[4] MICAMPR_EN bit powers down the right microphone amplifier. Writing 0 to the ANAMICLR[2] AUXR_EN bit disables the right auxiliary input.
- Audio/voice ADC control register

  Writing 0 to the AVADC_CTL[3] ADCL_EN bit disables the left audio/voice ADC. Writing 0 to the AVADC_CTL[1] ADCR_EN bit disables the right audio/voice ADC.
- ALC control register

  Writing 0 to the ALC_CTL[4] SUBMIC_ALC_EN bit powers off the submicrophone automatic level control (ALC). Writing 0 to the ALC_CTL[3] MAINMIC_ALC_EN bit powers off the main microphone ALC.
- Audio DAC and voice DAC power control register

  Writing 0 to the AVDAC_CTL[4] VDAC_EN bit disables the voice ADC. Writing 0 to the AVDAC_CTL[1] ADACL1_EN bit disables the first left audio DAC. Writing 0 to the AVDAC_CTL[0] ADACR1_EN bit disables the first right audio DAC.

  Writing 0 to the AVDAC_CTL[3] ADACL2_EN bit disables the left audio DAC. Writing 0 to the AVDAC_CTL[2] ADACR2_EN bit disables the right audio DAC.
- Audio RXL1 analog PGA control register

  Writing 0 to the ARXL1_APGA_CTL[0] ARXL1_PDZ bit puts the first audio left receiver analog PGA in power-down mode.
- Audio RXR1 analog PGA control register

Writing 0 to the ARXR1_APGA_CTL[0] ARXR1_PDZ bit puts the first audio right receiver analog PGA in power-down mode.

- Audio RXL2 analog PGA control register

  Writing 0 to the ARXL2_APGA_CTL[0] ARXL2_PDZ bit puts the second audio left receiver analog PGA in power-down mode.
- Audio RXR2 analog PGA control register

  Writing 0 to the ARXR2_APGA_CTL[0] ARXR2_PDZ bit puts the second audio right receiver analog PGA in power-down mode.
- Voice downlink analog PGA control register

  Writing 0 to the VDL_APGA_CTL[0] VDL_PDZ bit puts the voice downlink analog PGA in power-down mode.
- Earphone amplifier control register

  Writing 0 to the EAR_CTL[5:4] EAR_GAIN bit field puts the earphone in power-down mode.
- Predriver class D left amplifier control register

  Writing 0 to the PREDL_CTL[5:4] PREDL_GAIN bit field puts the predriver class D left amplifier in power-down mode.
- Predriver class D right amplifier control register

  Writing 0 to the PREDR_CTL[5:4] PREDR_GAIN bit field puts the predriver class D right amplifier in power-down mode.
- Preamplifier carkit left control register

  Writing 0 to the PRECKL_CTL[5:4] PRECKL_GAIN bit field puts the preamplifier carkit left amplifier in power-down mode.
- Preamplifier carkit right control register

  Writing 0 to the PRECKR_CTL[5:4] PRECKR_GAIN bit field puts the preamplifier carkit right amplifier in power-down mode.
- DTMF generator control

  Writing 0 to the DTMF_CTL[0] TONE_EN bit disables the tone generator.
- Audio PLL control register

  Writing 0 to the APLL_CTL[4] APLL_EN bit disables the audio PLL.

5.5.5.4 Power-Down Registers for USB_SC Module

- Controls UTMI+ on-the-go (OTG) functions of the PHY

  Writing 0 to the OTG_CTRL[5] DRVVBUS bit signals the internal charge pump not to drive the 5 V on VBUS.
- Controls OTG power section of the USB

  Writing 0 to the POWER_CTRL OTG_EN bit disables all the OTG comparators and reference circuitry in the VRUSB_3V1 supply domain.
- USB carkit

  Writing 0 to the CARKIT_ANA_CTRL[6] CR_INT_EN bit disables the USB carkit comparator.

  Writing 0 to the CARKIT_CTRL[0] CARKITPWR bit powers down the carkit circuitry.
- Controls UTMI function settings of the PHY

  Writing 0 to the FUNC_CTRL[6] SUSPENDM bit puts PHY in low-power mode. If SUSPENDM is used to enable low-power mode, the FUNC_CTRL register must be programmed last in the programming sequence, because when the device is in low-power mode, the ULPI clock is stopped and further register access is prevented.

5.5.5.5 Power-Down Registers for POWER_SC Module

- Power providers

  Twenty power resources are categorized as power providers in the device (see Table 5-7). Each power resource can be enabled and disabled by programming the corresponding registers. Writing 000 in the <resource name>_DEV_GRP[7:5] DEV_GRP bit field disables this resource.
- Vibrator module

Writing 0 to the VIBRATOR_CFG[3] VIB_ENABLE bit disables the vibrator.

- H-bridge vibrator control register
  Writing 0 to theVIBRA_CTL[0] VIVRA_EN bit powers off the H-bridge vibrator control.

5.6 Reset and Power-Management Registers

This section summarizes the registers for the hardware interface for power management.

NOTE: The names Triton 1 and Triton 2 are direct references to the device, indicating that the originating source material is from TI's product-development organization.

NOTE: For the state values, see Table 5-5.

5.6.1 Instance Summary

Table 5-45 lists the base address and address space for the power module instances.

Table 5-45. Instance Summary

Module Name	Base Address	Size
PM_MASTER	0x0000 0036	37 bytes
PM_RECEIVER	0x0000 005B	151 bytes

5.6.2 PM_Master Module Instance

This section provides information about the PM_MASTER module instance in this product. Table 5-50 through Table 5-122 describe the register bits

Table 5-46. PM_MASTER Mode Overview

Address Offset	Registers			
	ONNOFF		POR	
	READ	WRITE	READ	WRITE
0x00	CFG_P1_TRANSITION	CFG_P1_TRANSITION	CFG_P1_TRANSITION	CFG_P1_TRANSITION
0x01	CFG_P2_TRANSITION	CFG_P2_TRANSITION	CFG_P2_TRANSITION	CFG_P2_TRANSITION
0x02	CFG_P3_TRANSITION	CFG_P3_TRANSITION	CFG_P3_TRANSITION	CFG_P3_TRANSITION
0x03	CFG_P123_TRANSITION	CFG_P123_TRANSITION	CFG_P123_TRANSITION	CFG_P123_TRANSITION
0x04	STS_BOOT	STS_BOOT	STS_BOOT	STS_BOOT
0x05	CFG_BOOT	CFG_BOOT	CFG_BOOT	CFG_BOOT
0x06	SHUNDAN	SHUNDAN	SHUNDAN	SHUNDAN
0x07	BOOT_BCI	BOOT_BCI	BOOT_BCI	BOOT_BCI
0x08	CFG_PWRANA1	CFG_PWRANA1	CFG_PWRANA1	CFG_PWRANA1
0x09	CFG_PWRANA2	CFG_PWRANA2	CFG_PWRANA2	CFG_PWRANA2
0x0A	BGAP_TRIM	BGAP_TRIM	BGAP_TRIM	BGAP_TRIM
0x0B	BACKUP_MISC_STS	-	BACKUP_MISC_STS	-
0x0C	BACKUP_MISC_CFG	-	BACKUP_MISC_CFG	-
0x0D	BACKUP_MISC_TST	-	BACKUP_MISC_TST	-
0x0E	PROTECT_KEY	PROTECT_KEY	PROTECT_KEY	PROTECT_KEY
0x0F	STS_HW_CONDITIONS	STS_HW_CONDITIONS	STS_HW_CONDITIONS	STS_HW_CONDITIONS
0x10	P1_SW_EVENTS	P1_SW_EVENTS	P1_SW_EVENTS	P1_SW_EVENTS
0x11	P2_SW_EVENTS	P2_SW_EVENTS	P2_SW_EVENTS	P2_SW_EVENTS

Table 5-46. PM_MASTER Mode Overview (continued)

Address Offset	Registers			
	ONNOFF		POR	
	READ	WRITE	READ	WRITE
0x12	P3_SW_EVENTS	P3_SW_EVENTS	P3_SW_EVENTS	P3_SW_EVENTS
0x13	STS_P123_STATE	-	STS_P123_STATE	-
0x14	PB_CFG	PB_CFG	PB_CFG	PB_CFG
0x15	PB_WORD_MSB	PB_WORD_MSB	PB_WORD_MSB	PB_WORD_MSB
0x16	PB_WORD_LSB	PB_WORD_LSB	PB_WORD_LSB	PB_WORD_LSB
0x17	RESERVED_A	-	RESERVED_A	-
0x18	RESERVED_B	-	RESERVED_B	-
0x19	RESERVED_C	-	RESERVED_C	-
0x1A	RESERVED_D	-	RESERVED_D	-
0x1B	RESERVED_E	-	RESERVED_E	-
0x1C	SEQ_ADD_W2P	SEQ_ADD_W2P	SEQ_ADD_W2P	SEQ_ADD_W2P
0x1D	SEQ_ADD_P2A	SEQ_ADD_P2A	SEQ_ADD_P2A	SEQ_ADD_P2A
0x1E	SEQ_ADD_A2W	SEQ_ADD_A2W	SEQ_ADD_A2W	SEQ_ADD_A2W
0x1F	SEQ_ADD_A2S	SEQ_ADD_A2S	SEQ_ADD_A2S	SEQ_ADD_A2S
0x20	SEQ_ADD_S2A12	SEQ_ADD_S2A12	SEQ_ADD_S2A12	SEQ_ADD_S2A12
0x21	SEQ_ADD_S2A3	SEQ_ADD_S2A3	SEQ_ADD_S2A3	SEQ_ADD_S2A3
0x22	SEQ_ADD_WARM	SEQ_ADD_WARM	SEQ_ADD_WARM	SEQ_ADD_WARM
0x23	MEMORY_ADDRESS	MEMORY_ADDRESS	MEMORY_ADDRESS	MEMORY_ADDRESS
0x24	MEMORY_DATA	MEMORY_DATA	MEMORY_DATA	MEMORY_DATA

Table 5-47. PM_MASTER Mode Summary

Mode Name	Condition
ONNOFF	P(ONNOFF) = 0
POR	P(POR) = 0

Table 5-48. PM_MASTER Register Summary for ONNOFF Mode Active Condition: P(ONNOFF) = 0

Register Name	Type	Register Width (Bits)	Physical Address
CFG_P1_TRANSITION	RW	8	0x0000 0036-0x0000 0036
CFG_P2_TRANSITION	RW	8	0x0000 0037-0x0000 0037
CFG_P3_TRANSITION	RW	8	0x0000 0038-0x0000 0038
CFG_P123_TRANSITION	RW	8	0x0000 0039-0x0000 0039
STS_BOOT	RW	8	0x0000 003A-0x0000 003A
CFG_BOOT	RW	8	0x0000 003B-0x0000 003B
SHUNDAN	RW	8	0x0000 003C-0x0000 003C
BOOT_BCI	RW	8	0x0000 003D-0x0000 003D
CFG_PWRANA1	RW	8	0x0000 003E-0x0000 003E
CFG_PWRANA2	RW	8	0x0000 003F-0x0000 003F
BGAP_TRIM	RW	8	0x0000 0040-0x0000 0040
BACKUP_MISC_STS	R	8	0x0000 0041-0x0000 0041
BACKUP_MISC_CFG	R	8	0x0000 0042-0x0000 0042
BACKUP_MISC_TST	R	8	0x0000 0043-0x0000 0043
PROTECT_KEY	RW	8	0x0000 0044-0x0000 0044
STS_HW_CONDITIONS	RW	8	0x0000 0045-0x0000 0045
P1_SW_EVENTS	RW	8	0x0000 0046-0x0000 0046

Table 5-48. PM_MASTER Register Summary for ONNOFF Mode Active Condition: P(ONNOFF) = 0 (continued)

Register Name	Type	Register Width (Bits)	Physical Address
P2_SW_EVENTS	RW	8	0x0000 0047-0x0000 0047
P3_SW_EVENTS	RW	8	0x0000 0048-0x0000 0048
STS_P123_STATE	R	8	0x0000 0049-0x0000 0049
PB_CFG	RW	8	0x0000 004A-0x0000 004A
PB_WORD_MSB	RW	8	0x0000 004B-0x0000 004B
PB_WORD_LSB	RW	8	0x0000 004C-0x0000 004C
RESERVED_A	R	8	0x0000 004D-0x0000 004D
RESERVED_B	R	8	0x0000 004E-0x0000 004E
RESERVED_C	R	8	0x0000 004F-0x0000 004F
RESERVED_D	R	8	0x0000 0050-0x0000 0050
RESERVED_E	R	8	0x0000 0051-0x0000 0051
SEQ_ADD_W2P	RW	8	0x0000 0052-0x0000 0052
SEQ_ADD_P2A	RW	8	0x0000 0053-0x0000 0053
SEQ_ADD_A2W	RW	8	0x0000 0054-0x0000 0054
SEQ_ADD_A2S	RW	8	0x0000 0055-0x0000 0055
SEQ_ADD_S2A12	RW	8	0x0000 0056-0x0000 0056
SEQ_ADD_S2A3	RW	8	0x0000 0057-0x0000 0057
SEQ_ADD_WARM	RW	8	0x0000 0058-0x0000 0058
MEMORY_ADDRESS	RW	8	0x0000 0059-0x0000 0059
MEMORY_DATA	RW	8	0x0000 005A-0x0000 005A

Table 5-49. PM_MASTER Register Summary for POR Mode Active Condition: P(POR) = 0

Register Name	Type	Register Width (Bits)	Physical Address
CFG_P1_TRANSITION	RW	8	0x0000 0036-0x0000 0036
CFG_P2_TRANSITION	RW	8	0x0000 0037-0x0000 0037
CFG_P3_TRANSITION	RW	8	0x0000 0038-0x0000 0038
CFG_P123_TRANSITION	RW	8	0x0000 0039-0x0000 0039
STS_BOOT	RW	8	0x0000 003A-0x0000 003A
CFG_BOOT	RW	8	0x0000 003B-0x0000 003B
SHUNDAN	RW	8	0x0000 003C-0x0000 003C
BOOT_BCI	RW	8	0x0000 003D-0x0000 003D
CFG_PWRANA1	RW	8	0x0000 003E-0x0000 003E
CFG_PWRANA2	RW	8	0x0000 003F-0x0000 003F
BGAP_TRIM	RW	8	0x0000 0040-0x0000 0040
BACKUP_MISC_STS	R	8	0x0000 0041-0x0000 0041
BACKUP_MISC_CFG	R	8	0x0000 0042-0x0000 0042
BACKUP_MISC_TST	R	8	0x0000 0043-0x0000 0043
PROTECT_KEY	RW	8	0x0000 0044-0x0000 0044
STS_HW_CONDITIONS	RW	8	0x0000 0045-0x0000 0045
P1_SW_EVENTS	RW	8	0x0000 0046-0x0000 0046
P2_SW_EVENTS	RW	8	0x0000 0047-0x0000 0047
P3_SW_EVENTS	RW	8	0x0000 0048-0x0000 0048
STS_P123_STATE	R	8	0x0000 0049-0x0000 0049
PB_CFG	RW	8	0x0000 004A-0x0000 004A
PB_WORD_MSB	RW	8	0x0000 004B-0x0000 004B
PB_WORD_LSB	RW	8	0x0000 004C-0x0000 004C

Table 5-49. PM_MASTER Register Summary for POR Mode Active Condition: P(POR) = 0 (continued)

Register Name	Type	Register Width (Bits)	Physical Address
RESERVED_A	R	8	0x0000 004D-0x0000 004D
RESERVED_B	R	8	0x0000 004E-0x0000 004E
RESERVED_C	R	8	0x0000 004F-0x0000 004F
RESERVED_D	R	8	0x0000 0050-0x0000 0050
RESERVED_E	R	8	0x0000 0051-0x0000 0051
SEQ_ADD_W2P	RW	8	0x0000 0052-0x0000 0052
SEQ_ADD_P2A	RW	8	0x0000 0053-0x0000 0053
SEQ_ADD_A2W	RW	8	0x0000 0054-0x0000 0054
SEQ_ADD_A2S	RW	8	0x0000 0055-0x0000 0055
SEQ_ADD_S2A12	RW	8	0x0000 0056-0x0000 0056
SEQ_ADD_S2A3	RW	8	0x0000 0057-0x0000 0057
SEQ_ADD_WARM	RW	8	0x0000 0058-0x0000 0058
MEMORY_ADDRESS	RW	8	0x0000 0059-0x0000 0059
MEMORY_DATA	RW	8	0x0000 005A-0x0000 005A

Table 5-50. CFG_P1_TRANSITION

Address Offset	0x00-0x00 in 0xE byte increments		
Physical Address	0x0000 0036-0x0000 0036	**Instance**	PM_MASTER
Description	Configuration register for P1 transition (backup domain) Write-protected with the KEY_CFG		
Type	See Table 5-46, *PM_MASTER Mode Overview.*		
Write Latency			

7	6	5	4	3	2	1	0
STARTON_SWBUG	RESERVED	STARTON_VBUS	STARTON_VBAT	STARTON_RTC	STARTON_USB	STARTON_CHG	STARTON_PWON

Bits	Field Name	Description	Type	Reset
7	STARTON_SWBUG	Indicates whether a restart is performed by the watchdog 0: A restart is not performed when the watchdog expires. 1: A restart is performed when the watchdog expires.	RW	1
6	RESERVED		RW	1
5	STARTON_VBUS	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P1 is affected by a VBUS voltage detection 0: Transition is not affected by a VBUS voltage detection. 1: Transition is affected by a VBUS voltage detection.	RW	1
4	STARTON_VBAT	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P1 is affected when a battery is plugged in 0: Transition is not affected when a battery is plugged in. 1: Transition is affected when a battery is plugged in.	RW	1

Bits	Field Name	Description	Type	Reset
3	STARTON_RTC	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P1 is affected when an RTC request occurs 0: Transition is not affected when an RTC request occurs. 1: Transition is affected when an RTC request occurs.	RW	1
2	STARTON_USB	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P1 is affected when a USB plug is detected 0: Transition is not affected when a USB plug is detected. 1: Transition is affected when a USB plug is detected.	RW	1
1	STARTON_CHG	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P1 is affected when a charger is inserted. 0: Transition is not affected when a charger is inserted. 1: Transition is affected when a charger is inserted.	RW	1
0	STARTON_PWON	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P1 is affected when a keypad button is pressed. 0: Transition is not affected when a keypad button is pressed. 1: Transition is affected when a keypad button is pressed.	RW	1

Table 5-51. Register Call Summary for Register CFG_P1_TRANSITION

Reset and Power Management Functional Description
- Hardware Events for State Changes: [0]

Reset and Power-Management Registers
- PM_Master Module Instance: [1] [2] [3] [4] [5] [6]
- PM_RECEIVER Module Instance: [7] [8] [9] [10] [11] [12]

Table 5-52. CFG_P2_TRANSITION

Address Offset	0x01-0x01 in 0xE byte increments		
Physical Address	0x0000 0037-0x0000 0037	**Instance**	PM_MASTER
Description	Configuration register for P2 transition (backup domain) Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
STARTON_SWBUG	RESERVED	STARTON_VBUS	STARTON_VBAT	STARTON_RTC	STARTON_USB	STARTON_CHG	STARTON_PWON

Bits	Field Name	Description	Type	Reset
7	STARTON_SWBUG	Indicates whether a restart is performed by the watchdog 0: A restart is not performed when the watchdog expires. 1: A restart is performed when the watchdog expires.	RW	1
6	RESERVED			

Bits	Field Name	Description	Type	Reset
5	STARTON_VBUS	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P2 is affected by a VBUS voltage detection 0: Transition is not affected by a VBUS voltage detection. 1: Transition is affected by a VBUS voltage detection.	RW	1
4	STARTON_VBAT	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P2 is affected when a battery is plugged in 0: Transition is not affected when a battery is plugged in. 1: Transition is affected when a battery is plugged in.	RW	1
3	STARTON_RTC	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P2 is affected when an RTC request occurs 0: Transition is not affected when an RTC request occurs. 1: Transition is affected when an RTC request occurs.	RW	1
2	STARTON_USB	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P2 is affected when a USB plug is detected 0: Transition is not affected when a USB plug is detected. 1: Transition is affected when a USB plug is detected.	RW	1
1	STARTON_CHG	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P2 is affected when a charger is inserted 0: Transition is not affected when a charger is inserted. 1: Transition is affected when a charger is inserted.	RW	1
0	STARTON_PWON	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P2 is affected when a keypad button is pressed 0: Transition is not affected when a keypad button is pressed. 1: Transition is affected when a keypad button is pressed.	RW	1

Table 5-53. Register Call Summary for Register CFG_P2_TRANSITION

Reset and Power Management Functional Description • Hardware Events for State Changes: [0]
Reset and Power-Management Registers • PM_Master Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-54. CFG_P3_TRANSITION

Address Offset	0x02-0x02 in 0xE byte increments		
Physical Address	0x0000 0038-0x0000 0038	**Instance**	PM_MASTER
Description	Configuration register for P3 transition (backup domain) Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
STARTON_SWBUG	RESERVED	STARTON_VBUS	STARTON_VBAT	STARTON_RTC	STARTON_USB	STARTON_CHG	STARTON_PWON

Bits	Field Name	Description	Type	Reset
7	STARTON_SWBUG	Indicates whether a restart is performed by the watchdog 0: A restart is not performed when the watchdog expires. 1: A restart is performed when the watchdog expires.	RW	1
6	RESERVED			
5	STARTON_VBUS	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P3 is affected by a VBUS voltage detection 0: Transition is not affected by a VBUS voltage detection. 1: Transition is affected by a VBUS voltage detection.	RW	1
4	STARTON_VBAT	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P3 is affected when a battery is plugged in 0: Transition is not affected when a battery is plugged in. 1: Transition is affected when a battery is plugged in.	RW	1
3	STARTON_RTC	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P3 is affected when an RTC request occurs 0: Transition is not affected when an RTC request occurs. 1: Transition is affected when an RTC request occurs.	RW	1
2	STARTON_USB	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P3 is affected when a USB plug is detected 0: Transition is not affected when a USB plug is detected. 1: Transition is affected when a USB plug is detected.	RW	1
1	STARTON_CHG	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P3 is affected when a charger is inserted 0: Transition is not affected when a charger is inserted. 1: Transition is affected when a charger is inserted.	RW	1
0	STARTON_PWON	Indicates whether an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition for P3 is affected when a keypad button is pressed 0: Transition is not affected when a keypad button is pressed. 1: Transition is affected when a keypad button is pressed.	RW	1

Table 5-55. Register Call Summary for Register CFG_P3_TRANSITION

Reset and Power Management Functional Description • Hardware Events for State Changes: [0]
Reset and Power-Management Registers • PM_Master Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-56. CFG_P123_TRANSITION

Address Offset	0x03-0x03 in 0xE byte increments		
Physical Address	0x0000 0039-0x0000 0039	**Instance**	PM_MASTER
Description	Configuration register for transition processors 1, 2 and 3 (backup domain)		
	Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
MSK_THERMAL_SHUTDOWN	MSK_MBLO	SEQ_MSK_BAT_PRESENCE	SEQ_MSK_BAT_LEVEL	SEQ_MSK_THERM_HD	SEQ_FREEZE	SEQ_ONSYNC	SEQ_OFFSYNC

Bits	Field Name	Description	Type	Reset
7	MSK_THERMAL_SHUTDOWN	0: PMC is reset when TS = 1. 1: PMC is not reset when TS = 1.	RW	1
6	MSK_MBLO	0: PMC is reset when MBLO = 1. 1: PMC is not reset when MBLO = 1.	RW	0
5	SEQ_MSK_BAT_PRESENCE	0: Vbat presence comparator checks a valid OFF-to-ACTIVE transition. 1: Vbat presence comparator does not check a valid OFF-to-ACTIVE transition; the comparator status is seen as equal to 1.	RW	1
4	SEQ_MSK_BAT_LEVEL	0: Vbat voltage comparator checks a valid OFF-to-ACTIVE transition. 1: Vbat voltage comparator does not check a valid OFF-to-ACTIVE transition; the comparator status is seen as equal to 1.	RW	0
3	SEQ_MSK_THERM_HD	0: Therm HD checks a valid OFF-to-ACTIVE transition. 1: Therm HD does not check a valid OFF-to-ACTIVE transition.	RW	1
2	SEQ_FREEZE	1: Freeze all sequencers in their current states; every sequencer finishes its current transition if one is ongoing. 0: All sequencers can initiate new transitions.	RW	0
1	SEQ_ONSYNC	1: All sequencers wait for each other before any P[123]_OFF-to-ACTIVE transition. Any switch-on on one sequencer is applied on all sequencers. (Has priority over switch-on mask condition) 0: All sequencers do not wait for each other before any P[123]_OFF-to-ACTIVE transition. This register can switch on one part of the design by software and not with a hardware condition.	RW	1
0	SEQ_OFFSYNC	1: All sequencers wait for each other before any P[123]_ACT2WAITON transition. Any write in P[123]_DEVOFF also writes the value in P[123]_DEVOFF.	RW	1

Bits	Field Name	Description	Type	Reset
		0: All sequencers do not wait for each other before any P[123]_ACT2WAITON transition. This register can switch off one part of the design by software.		

Table 5-57. Register Call Summary for Register CFG_P123_TRANSITION

Reset and Power-Management Registers
- PM_Master Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-58. STS_BOOT

Address Offset	0x04-0x04 in 0xE byte increments		
Physical Address	0x0000 003A-0x0000 003A	**Instance**	PM_MASTER
Description	Backup domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
BACKUP	TS	WATCHDOG_RESET	ITCHECK_RESET	PWRON_8S	SETUP_ DONE_BCK	SETUP_ DONE_PMC	SYSEN_RESET

Bits	Field Name	Description	Type	Reset
7	BACKUP	1: Triton2 entered backup mode since last register clear. 0: Triton2 did not reach backup mode since last register clear.	RW	0
6	TS	1: A thermal shutdown occurred since last register clear. 0: No thermal shutdown occurred since last register clear.	RW	0
5	WATCHDOG_RESET	1: Reset caused by a warm reset occurred since last register clear. 0: No reset caused by a warm reset occurred since last register clear.	RW	0
4	ITCHECK_RESET	1: Reset caused by an IT_Check since last register clear. 0: No reset caused by an IT_Check occurred since last register clear.	RW	0
3	PWRON_8S	1: Restart caused by a PWRON low for more than 8s occurred since last register clear. 0: No restart caused by a PWRON low for more than 8s occurred since last register clear.	RW	0
2	SETUP_ DONE_BCK	Backup configuration is done (RTC, BACKUP registers, etc.). This bit can be set to 1 by the user when backup domain configuration completes. This bit is automatically reset to 0 when the backup configuration is lost.	RW	0
1	SETUP_ DONE_PMC	PMC configuration is done. This bit can be set to 1 by the user when PMC configuration completes. This bit is automatically reset to 0 when the PMC configuration is lost.	RW	0

Bits	Field Name	Description	Type	Reset
0	SYSEN_RESET	1: SYSEN was driven low by an external device since last register clear. 0: SYSEN was not driven low by an external device since last register clear.	RW	0

Table 5-59. Register Call Summary for Register STS_BOOT

Reset and Power-Management Integration • Resets: [0]
Reset and Power Management Functional Description • Event Definition: [1]
Reset and Power-Management Programming Model • Sequencing: [2]
Reset and Power-Management Registers • PM_Master Module Instance: [3] [4] [5] [6] [7] [8]

Table 5-60. CFG_BOOT

Address Offset	0x05-0x05 in 0xE byte increments		
Physical Address	0x0000 003B-0x0000 003B	**Instance**	PM_MASTER
Description	Boot configuration register (backup domain) Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
CK32K_LOWPWR_EN	BOOT_CFG			HIGH_PERF_SQ	SLICER_BYPASS	HFCLK_FREQ	

Bits	Field Name	Description	Type	Reset
7	CK32K_LOWPWR_EN	0: The 32-kHz oscillator never goes to low-power mode. 1: The 32-kHz oscillator goes to low-power mode if main battery voltage is low.	RW	0
6:4	BOOT_CFG	BOOT_CFG = (TEST.RESET, BOOT1, BOOT0)	R	0x0
3	HIGH_PERF_SQ	0: Slicer not in high-performance mode 1: Slicer in high-performance mode	RW	1
2	SLICER_BYPASS	0: Slicer not bypassed 1: Slicer bypassed	RW	0
1: 0	HFCLK_FREQ	00: Not programmed 01: 19.2 MHz 10: 26 MHz 11: 38.4 MHz The software should program this register during the boot sequence.	RW	0x0

Bits	Field Name	Description	Type	Reset
		If this register remains at 00: • The internal clock_OK from the slicer is tied to 1. • The DC/DCs cannot use the divided HF clock (they remain on their internal oscillator). • The main clock generator cannot provide the clock to the MADC and the USB.		

Table 5-61. Register Call Summary for Register CFG_BOOT

Reset and Power-Management Programming Model • Power-Down Registers for INTERFACE_SC Module: [0] [1]
Reset and Power-Management Registers • PM_Master Module Instance: [2] [3] [4] [5] [6] [7]

Table 5-62. SHUNDAN

Address Offset	0x06-0x06 in 0xE byte increments		
Physical Address	0x0000 003C-0x0000 003C	**Instance**	PM_MASTER
Description	Backup domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		CNT					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:0	CNT	When Vbat is low, count up to 2 seconds using a 32 Hz clock (32.768 kHz/1024). The default value of this register is 0x3F after the first main battery insertion. The maximum value is 0x3E. This register can be set back to 0x00 by software.	RW	0x3F

Table 5-63. Register Call Summary for Register SHUNDAN

Reset and Power-Management Registers • PM_Master Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-64. BOOT_BCI

Address Offset	0x07-0x07 in 0xE byte increments		
Physical Address	0x0000 003D-0x0000 003D	**Instance**	POWERPM_MASTER
Description	Boot BCI register (backup domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		BCIAUTOWEN	CONFIG_DONE	Reserved	CVENAC	BCIAUTOUSB	BCIAUTOAC

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5	BCIAUTOWEN	0: PI_BCIAUTOWEN is low. 1: PI_BCIAUTOWEN is high.	R	0
4	CONFIG_DONE	If CONFIG_DONE = 0 and the device is powered up by a charger plug (VAC or USB), BCIAUTOAC and CVENAC are updated with the boot pad value. If CONFIG_DONE = 1, BCIAUTOAC and CVENAC are not updated by the BOOT pad.	RW	1
3	Reserved		R	0
2	CVENAC	AC constant voltage boot mode. Boot value can be updated by a boot pad. (See BCI specification) (active high) Must have PI_BCIAUTOWEN = 1 to enable the write access.	RW	1
1	BCIAUTOUSB	USB automatic charge boot mode (active high). Must have PI_BCIAUTOWEN = 1 to enable the write access.	RW	0
0	BCIAUTOAC	AC automatic charge boot mode. Boot value can be updated by a boot pad. (See BCI specification) (active high) Must have PI_BCIAUTOWEN = 1 to enable the write access.	RW	1

Table 5-65. Register Call Summary for Register BOOT_BCI

Reset and Power-Management Programming Model
- Power-Down Registers for AUXILIARY_SC Module: [0] [1] [2]

Reset and Power-Management Registers
- PM_Master Module Instance: [3] [4] [5] [6] [7] [8]

Table 5-66. CFG_PWRANA1

Address Offset	0x08-0x08 in 0xE byte increments		
Physical Address	0x0000 003E-0x0000 003E	**Instance**	PM_MASTER
Description	Configuration for PWRANA1 voltage regulator (backup domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	BGTRIM_LOWV						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	BGTRIM_LOWV		RW	0x40

Table 5-67. Register Call Summary for Register CFG_PWRANA1

Reset and Power-Management Registers
- PM_Master Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-68. CFG_PWRANA2

Address Offset	0x09-0x09 in 0xE byte increments		
Physical Address	0x0000 003F-0x0000 003F	**Instance**	PM_MASTER
Description	Configuration for PWRANA2 voltage regulator (backup domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
VRRTC_DISABLE	VRRTC_SLEEP	VRRTC_TRIEN	VRRTC_TRIM		LOJIT1_LOWV	LOJIT0_LOWV	BYP_32KHZ_ LOWV

Bits	Field Name	Description	Type	Reset
7	VRRTC_DISABLE	0: Functional mode 1: VRRTC LDO is in off mode when it should be in active mode. Protected with KEY_TST.	RW	0
6	VRRTC_SLEEP	0: Functional mode 1: VRRTC LDO is in sleep mode when it should be in active mode.	RW	0
5	VRRTC_TRIEN	0: Functional mode 1: Regulator output is high-impedance. Protected with the KEY_TST.	RW	0
4:3	VRRTC_TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x1
2	LOJIT1_LOWV	Protected with KEY_TST. If used in functional mode, lock back the KEY_TST immediately after register write.	RW	1
1	LOJIT0_LOWV	If LOJIT0 and LOJT1 are low, the 32-kHz oscillator is in high-jitter mode. In all other cases, the 32-kHz oscillator is in low-jitter mode. Protected with KEY_TST. If used in functional mode, lock back the KEY_TST immediately after register write.	RW	1
0	BYP_32KHZ_ LOWV	Protected with KEY_TST. This bit reset value is 1 in slave and test modes.	RW	0

Table 5-69. Register Call Summary for Register CFG_PWRANA2

Reset and Power-Management Registers

- PM_Master Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-70. BGAP_TRIM

Address Offset	0x0A-0x0A in 0xE byte increments		
Physical Address	0x0000 0040-0x0000 0040	**Instance**	PM_MASTER
Description	Backup domain. Protected with the TEST_KEY.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		BG500_TRIM			BG750_TRIM		

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0X0
5:3	BG500_TRIM		RW	0x4
2:0	BG750_TRIM		RW	0x4

Table 5-71. Register Call Summary for Register BGAP_TRIM

Reset and Power-Management Registers

- PM_Master Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-72. BACKUP_MISC_STS

Address Offset	0x0B-0x0B in 0xE byte increments		
Physical Address	0x0000 0041-0x0000 0041	**Instance**	PM_MASTER
Description	Backup domain		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-73. Register Call Summary for Register BACKUP_MISC_STS

Reset and Power-Management Registers

- PM_Master Module Instance: [0] [1] [2] [3]

Table 5-74. BACKUP_MISC_CFG

Address Offset	0x0C-0x0C in 0xE byte increments		
Physical Address	0x0000 0042-0x0000 0042	**Instance**	PM_MASTER
Description	Backup domain		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-75. Register Call Summary for Register BACKUP_MISC_CFG

Reset and Power-Management Registers

- PM_Master Module Instance: [0] [1] [2] [3]

Table 5-76. BACKUP_MISC_TST

Address Offset	0x0D-0x0D in 0xE byte increments		
Physical Address	0x0000 0043-0x0000 0043	**Instance**	PM_MASTER
Description	Backup domain		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-77. Register Call Summary for Register BACKUP_MISC_TST

Reset and Power-Management Registers

- PM_Master Module Instance: [0] [1] [2] [3]

Table 5-78. PROTECT_KEY

Address Offset	0x0E-0x0E in 0xE byte increments
Physical Address	0x0000 0044-0x0000 0044 **Instance** PM_MASTER
Description	Write C0, then 0C enable write access to power configuration registers. (KEY_CFG = 1) Write any other values to disable access to power configuration and test registers. Read 01 when access to power test registers is enabled. Read 10 when access to power configuration registers is enabled. Read 11 when access to power configuration and test registers is enabled. Read 00 when access to power configuration and test registers is disabled. When KEY_CFG = 0, no write in all protected register bits. Read is still possible. When KEY_CFG = 1, read and write possible in protected register bits VRRTC domain
Type	RW
Write Latency	

7	6	5	4	3	2	1	0

Bits	Field Name	Description	Type	Reset
7:0	PROTECT_KEY		RW	0x00

Table 5-79. Register Call Summary for Register PROTECT_KEY

Reset and Power-Management Registers

- PM_Master Module Instance: [0] [1] [2] [3] [4] [5] [6]

Table 5-80. STS_HW_CONDITIONS

Address Offset	0x0F-0x0F in 0xE byte increments		
Physical Address	0x0000 0045-0x0000 0045	**Instance**	PM_MASTER
Description	VRRTC domain		
Type	See Table 5-46, *PM_MASTER Mode Overview.*		
Write Latency			

7	6	5	4	3	2	1	0
STS_VBUS	STS_WAKEUP3	STS_WAKEUP2	STS_WAKEUP1	STS_WARMRESET	STS_USB	STS_CHG	STS_PWON

Bits	Field Name	Description	Type	Reset
7	STS_VBUS	Level status of VBUS port 1: USB is plugged in. 0: USB is unplugged.	R	0
6	STS_WAKEUP3	Level status of WAKEUP3 pad (active high) = CLKREQ	R	0
5	STS_WAKEUP2	Level status of WAKEUP2 pad (active high) = nSLEEP2	R	0
4	STS_WAKEUP1	Level status of WAKEUP1 pad (active high) = nSLEEP1	R	0
3	STS_WARMRESET	0: Warmreset is not active; nRESWARM pad is high. 1: Warmreset is active; nRESWARM pad is low.	R	0
2	STS_USB	Level status of USB port 1: USB is plugged in. 0: USB is unplugged.	R	0
1	STS_CHG	Level status of VAC PAD (charger) 1: Charger is plugged in. 0: Charger is unplugged. Conditions of VAC plugged in: Rising edge: Vbat + 0.3 V minimum, Vbat + 0.4 V Typ, Vbat + 0.6 maximum Falling edge: Vbat - 0.1 minimum, Vbat Typ, Vbat + 0.2 maximum	R	0
0	STS_PWON	Level status of PWRON button (active high), after debouncing	R	0

Table 5-81. Register Call Summary for Register STS_HW_CONDITIONS

Reset and Power-Management Registers

- PM_Master Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-82. P1_SW_EVENTS

Address Offset	0x10-0x10 in 0xE byte increments		
Physical Address	0x0000 0046-0x0000 0046	**Instance**	PM_MASTER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	STOPON_PWRON	STOPON_SYSEN	ENABLE_WARMRESET	LVL_WAKEUP	DEVACT	DEVSLP	DEVOFF

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	STOPON_PWRON	0: The feature is disabled. 1: The registers except backup domain are reset by the PWRON key push lasting longer than 8 seconds, and Triton 2 restarts. This bit is common to all processors and can be updated from the following registers: • P1_SW_EVENTS • P2_SW_EVENTS • P3_SW_EVENTS	RW	0
5	STOPON_SYSEN	0: Disable Triton reset when SYSEN is driven low by an external device. 1: Enable Triton reset when SYSEN is driven low by an external device.	RW	0
4	ENABLE_WARMRESET	0: Disable warm reset for selected processor. 1: Enable warm reset for selected processor.	RW	0
3	LVL_WAKEUP	0: The nSLEEP1 signal cannot set P1 resources in sleep mode. Resources still wake up on the nSLEEP1 rising edge. 1: Resources associated with P1 are in active mode, if nSLEEP1 is high, or in sleep mode, if nSLEEP1 is low.	RW	0
2	DEVACT	Write 1 starts an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition. This bit is cleared automatically.	W	0
1	DEVSLP	Write 1 starts an ACTIVE-to-SLEEP transition. This bit is cleared automatically.	W	0
0	DEVOFF	Write 1 starts an ACTIVE-to-OFF or SLEEP-to-OFF transition. This bit is cleared automatically.	W	0

Table 5-83. Register Call Summary for Register P1_SW_EVENTS

Reset and Power-Management Integration • Resets: [0]
Reset and Power Management Functional Description • Software Events for State Changes: [1]

Table 5-83. Register Call Summary for Register P1_SW_EVENTS (continued)

Reset and Power-Management Programming Model • Sequencing: [2]
Reset and Power-Management Registers • PM_Master Module Instance: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]

Table 5-84. P2_SW_EVENTS

Address Offset	0x11-0x11 in 0xE byte increments		
Physical Address	0x0000 0047-0x0000 0047	**Instance**	PM_MASTER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	STOPON_PWRON	STOPON_SYSEN	ENABLE_WARMRESET	LVL_WAKEUP	DEVACT	DEVSLP	DEVOFF

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	STOPON_PWRON	0: The feature is disabled. 1: The registers except backup domain are reset by the PWRON key push lasting longer than 8 seconds, and Triton 2 restarts. This bit is common to all processors and can be updated from the following registers: • P1_SW_EVENTS • P2_SW_EVENTS • P3_SW_EVENTS	RW	0
5	STOPON_SYSEN	0: Disable Triton reset when SYSEN is driven low by an external device. 1: Enable Triton reset when SYSEN is driven low by an external device. This bit is common to all processors and can be updated from the following registers: • P1_SW_EVENTS • P2_SW_EVENTS • P3_SW_EVENTS	RW	0
4	ENABLE_WARMRESET	0: Disable warm reset for selected processor. 1: Enable warm reset for selected processor.	RW	0
3	LVL_WAKEUP	0: The nSLEEP2 signal cannot set P2 resources in sleep mode. Resources still wake up on the nSLEEP2 rising edge. 1: Resources associated with P2 are in active mode, if nSLEEP2 is high, or in sleep mode, if nSLEEP2 is low.	RW	0
2	DEVACT	Write 1 starts an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition. This bit is cleared automatically.	W	0
1	DEVSLP	Write 1 starts an ACTIVE-to-SLEEP transition.	W	0

Bits	Field Name	Description	Type	Reset
		This bit is cleared automatically.		
0	DEVOFF	Write 1 starts an ACTIVE-to-OFF or SLEEP-to-OFF transition. This bit is cleared automatically.	W	0

Table 5-85. Register Call Summary for Register P2_SW_EVENTS

Reset and Power-Management Integration • Resets: [0]
Reset and Power Management Functional Description • Software Events for State Changes: [1]
Reset and Power-Management Registers • PM_Master Module Instance: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11]

Table 5-86. P3_SW_EVENTS

Address Offset	0x12-0x12 in 0xE byte increments		
Physical Address	0x0000 0048-0x0000 0048	**Instance**	PM_MASTER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	STOPON_PWRON	STOPON_SYSEN	ENABLE_WARMRESET	LVL_WAKEUP	DEVACT	DEVSLP	DEVOFF

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	STOPON_PWRON	0: The feature is disabled. 1: The registers except backup domain are reset by the PWRON key push lasting longer than 8 seconds, and the device restarts. This bit is common to all processors and can be updated from the following registers: • P1_SW_EVENTS • P2_SW_EVENTS • P3_SW_EVENTS	RW	0
5	STOPON_SYSEN	0: Disable Triton reset when SYSEN is driven low by an external device. 1: Enable Triton reset when SYSEN is driven low by an external device.	RW	0
4	ENABLE_WARMRESET	0: Disable warm reset for selected processor. 1: Enable warm reset for selected processor.	RW	0
3	LVL_WAKEUP	0: The CLKREQ signal cannot set P3 resources in sleep mode. Resources still wake up on the CLKREQ rising edge. 1: Resources associated with P3 are in active mode, if CLKREQ is high, or in sleep mode, if CLKREQ is low.	RW	0

Bits	Field Name	Description	Type	Reset
2	DEVACT	Write 1 starts an OFF-to-ACTIVE or SLEEP-to-ACTIVE transition. This bit is cleared automatically.	W	0
1	DEVSLP	Write 1 starts an ACTIVE-to-SLEEP transition. This bit is cleared automatically.	W	0
0	DEVOFF	Write 1 starts an ACTIVE-to-OFF or SLEEP-to-OFF transition. This bit is cleared automatically.	W	0

Table 5-87. Register Call Summary for Register P3_SW_EVENTS

Reset and Power-Management Integration • Resets: [0]
Reset and Power Management Functional Description • Software Events for State Changes: [1]
Reset and Power-Management Programming Model • Sequencing: [2]
Reset and Power-Management Registers • PM_Master Module Instance: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]

Table 5-88. STS_P123_STATE

Address Offset	0x13-0x13 in 0xE byte increments		
Physical Address	0x0000 0049-0x0000 0049	**Instance**	PM_MASTER
Description	VRRTC domain		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	STS_P123_ STATE_STABLE	SEQ_P3_STATE		SEQ_P2_STATE		SEQ_P1_STATE	

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	STS_P123_ STATE_STABLE	Status of P123 state-machine 0: A transition is ongoing on one of the state-machines. 1: No transition is ongoing on the state-machines.	R	0
5:4	SEQ_P3_STATE	Current state of sequencer P3	R	0x0
3:2	SEQ_P2_STATE	Current state of sequencer P2	R	0x0
1: 0	SEQ_P1_STATE	Current state of sequencer P1	R	0x0

Table 5-89. Register Call Summary for Register STS_P123_STATE

Reset and Power-Management Programming Model • Sequencing: [0]
Reset and Power-Management Registers • PM_Master Module Instance: [1] [2] [3] [4]

Table 5-90. PB_CFG

Address Offset	0x14-0x14 in 0xE byte increments		
Physical Address	0x0000 004A-0x0000 004A	**Instance**	PM_MASTER
Description	VRRTC domain		
Type	See Table 5-46, *PM_MASTER Mode Overview.*		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				PB_P123_BW		PB_I2C_BWEN	PB_I2C_BUSY

Bits	Field Name	Description	Type	Reset
7:4	Reserved		R	0x0
3:2	PB_P123_BW	00: P1, P2 , and P3 have equal bandwidth (33 percent if PB_I2C_BWEN is low; 25 percent if PB_I2C_BWEN is high). 01: P1 has 50 percent power bus bandwidth; others share 50 percent bandwidth equally (25 percent if PB_I2C_BWEN is low; 16 percent if PB_I2C_BWEN is high). 10: P2 has 50 percent power bus bandwidth; others share 50 percent bandwidth equally (25 percent if PB_I2C_BWEN is low; 16 percent if PB_I2C_BWEN is high). 11: P3 has 50 percent power bus bandwidth; others share 50 percent bandwidth equally (25 percent if PB_I2C_BWEN is low; 16 percent if PB_I2C_BWEN is high).	RW	0x0
1	PB_I2C_BWEN	0: I^2C has no access on power bus. 1: I^2C has access to power bus (reduced bandwidth for P[123] that does not have 50 percent bandwidth).	RW	0
0	PB_I2C_BUSY	1: PB word is queued and has not been sent on power bus. 0: Buffer empty/ready to send a word on power bus.	R	0

Table 5-91. Register Call Summary for Register PB_CFG

Reset and Power-Management Registers • PM_Master Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-92. PB_WORD_MSB

Address Offset	0x15-0x15 in 0xE byte increments		
Physical Address	0x0000 004B-0x0000 004B	**Instance**	PM_MASTER
Description	VRRTC domain		
Type	See Table 5-46, *PM_MASTER Mode Overview.*		
Write Latency			

7	6	5	4	3	2	1	0

Bits	Field Name	Description	Type	Reset
7:0	PB_WORD_MSB	PB_Word MSB	RW	0xFF

Table 5-93. Register Call Summary for Register PB_WORD_MSB

Reset and Power-Management Integration • Resets: [0] [1]
Reset and Power-Management Programming Model • Sequencing: [2]
Reset and Power-Management Registers • PM_Master Module Instance: [3] [4] [5] [6] [7] [8] [9]

Table 5-94. PB_WORD_LSB

Address Offset	0x16-0x16 in 0xE byte increments		
Physical Address	0x0000 004C-0x0000 004C	**Instance**	PM_MASTER
Description	VRRTC domain		
Type	See Table 5-46, *PM_MASTER Mode Overview.*		
Write Latency			

7	6	5	4	3	2	1	0

Bits	Field Name	Description	Type	Reset
7:0	PB_WORD_LSB	PB_Word LSB. This register write triggers PB word write.	RW	0xFF

Table 5-95. Register Call Summary for Register PB_WORD_LSB

Reset and Power-Management Integration • Resets: [0] [1]
Reset and Power-Management Programming Model • Sequencing: [2]
Reset and Power-Management Registers • PM_Master Module Instance: [3] [4] [5] [6] [7] [8] [9]

Table 5-96. RESERVED_A

Address Offset	0x17-0x17 in 0xE byte increments		
Physical Address	0x0000 004D-0x0000 004D	**Instance**	PM_MASTER
Description	VRRTC domain		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-97. Register Call Summary for Register RESERVED_A

Reset and Power-Management Registers

- PM_Master Module Instance: [0] [1] [2] [3]

Table 5-98. RESERVED_B

Address Offset	0x18-0x18 in 0xE byte increments		
Physical Address	0x0000 004E-0x0000 004E	**Instance**	PM_MASTER
Description	VRRTC domain		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-99. Register Call Summary for Register RESERVED_B

Reset and Power-Management Registers

- PM_Master Module Instance: [0] [1] [2] [3]

Table 5-100. RESERVED_C

Address Offset	0x19-0x19 in 0xE byte increments		
Physical Address	0x0000 004F-0x0000 004F	**Instance**	PM_MASTER
Description	VRRTC domain		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-101. Register Call Summary for Register RESERVED_C

Reset and Power-Management Registers

- PM_Master Module Instance: [0] [1] [2] [3]

Table 5-102. RESERVED_D

Address Offset	0x1A-0x1A in 0xE byte increments		
Physical Address	0x0000 0050-0x0000 0050	**Instance**	PM_MASTER
Description	VRRTC domain		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-103. Register Call Summary for Register RESERVED_D

Reset and Power-Management Registers

- PM_Master Module Instance: [0] [1] [2] [3]

Table 5-104. RESERVED_E

Address Offset	0x1B-0x1B in 0xE byte increments		
Physical Address	0x0000 0051-0x0000 0051	**Instance**	PM_MASTER
Description	Write-protected with the KEY_CFG (VRRTC domain)		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved					CFG_VBUSDEB		

Bits	Field Name	Description	Type	Reset
7:3	Reserved		R	0x00
2:0	CFG_VBUSDEB	Programmable debounce on VBUS and ID for power SC starting event and IT generation 000: 0 ms 001: 14 ms 010: 28 ms 011: 41.9 ms 100: 69.9 ms 101: 93.2 ms 110: 139.7 ms 111: 232.8 ms	RW	0x2

Table 5-105. Register Call Summary for Register RESERVED_E

Reset and Power Management Functional Description • Hardware Events for State Changes: [0]
Reset and Power-Management Registers • PM_Master Module Instance: [1] [2] [3] [4]

Table 5-106. SEQ_ADD_W2P

Address Offset	0x1C-0x1C in 0x9 byte increments		
Physical Address	0x0000 0052-0x0000 0052	**Instance**	PM_MASTER
Description	Memory address of WAIT-ON-to-presence check sequence base add (VRRTC domain) Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				SEQ_ADD			

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:0	SEQ_ADD	Memory address for transition start step	RW	0x00

Table 5-107. Register Call Summary for Register SEQ_ADD_W2P

Reset and Power Management Functional Description • WAIT-ON-to-ACTIVE Transition: [0] [1] • Power-Management Sequencing Memory Structure: [2]
Reset and Power-Management Registers • PM_Master Module Instance: [3] [4] [5] [6] [7] [8]

Table 5-108. SEQ_ADD_P2A

Address Offset	0x1D-0x1D in 0x9 byte increments		
Physical Address	0x0000 0053-0x0000 0053	**Instance**	PM_MASTER
Description	Memory address of presence check-to-active sequence base add (VRRTC domain) Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				SEQ_ADD			

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:0	SEQ_ADD	Memory address for transition start step	RW	0x04

Table 5-109. Register Call Summary for Register SEQ_ADD_P2A

Reset and Power Management Functional Description • WAIT-ON-to-ACTIVE Transition: [0] [1] • Power-Management Sequencing Memory Structure: [2]
Reset and Power-Management Registers • PM_Master Module Instance: [3] [4] [5] [6] [7] [8]

Table 5-110. SEQ_ADD_A2W

Address Offset	0x1E-0x1E in 0x9 byte increments		
Physical Address	0x0000 0054-0x0000 0054	**Instance**	PM_MASTER
Description	Memory address of All-to-WAIT-ON sequence base add (VRRTC domain) Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		SEQ_ADD					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:0	SEQ_ADD	Memory address for transition start step	RW	0x0D

Table 5-111. Register Call Summary for Register SEQ_ADD_A2W

Reset and Power Management Functional Description
- Power-Management Sequencing Memory Structure: [0]
- Switch-On and Switch-Off Transitions: [1] [2] [3]
- SLEEP → ON and SLEEP → OFF Transitions: [4]

Reset and Power-Management Registers
- PM_Master Module Instance: [5] [6] [7] [8] [9] [10]

Table 5-112. SEQ_ADD_A2S

Address Offset	0x1F-0x1F in 0x9 byte increments		
Physical Address	0x0000 0055-0x0000 0055	**Instance**	PM_MASTER
Description	Memory address of ACTIVE-to-SLEEP sequence base add (VRRTC domain) Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		SEQ_ADD					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:0	SEQ_ADD	Memory address for transition start step	RW	0x00

Table 5-113. Register Call Summary for Register SEQ_ADD_A2S

Reset and Power Management Functional Description
- Power-Management Sequencing Memory Structure: [0]
- SLEEP → ON and SLEEP → OFF Transitions: [1] [2] [3]

Reset and Power-Management Registers
- PM_Master Module Instance: [4] [5] [6] [7] [8] [9]

Table 5-114. SEQ_ADD_S2A12

Address Offset	0x20-0x20 in 0x9 byte increments		
Physical Address	0x0000 0056-0x0000 0056	**Instance**	PM_MASTER
Description	Memory address of SLEEP-to-ACTIVE sequence base add (VRRTC domain) Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		SEQ_ADD					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:0	SEQ_ADD	Memory address for transition start step	RW	0x00

Table 5-115. Register Call Summary for Register SEQ_ADD_S2A12

Reset and Power Management Functional Description
- Power-Management Sequencing Memory Structure: [0]
- SLEEP → ON and SLEEP → OFF Transitions: [1]

Reset and Power-Management Registers
- PM_Master Module Instance: [2] [3] [4] [5] [6] [7]

Table 5-116. SEQ_ADD_S2A3

Address Offset	0x21-0x21 in 0x9 byte increments		
Physical Address	0x0000 0057-0x0000 0057	**Instance**	PM_MASTER
Description	Memory address of SLEEP-to-ACTIVE sequence base add (VRRTC domain) Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		SEQ_ADD					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:0	SEQ_ADD	Memory address for transition start step	RW	0x00

Table 5-117. Register Call Summary for Register SEQ_ADD_S2A3

Reset and Power Management Functional Description
- Power-Management Sequencing Memory Structure: [0]
- SLEEP → ON and SLEEP → OFF Transitions: [1]

Reset and Power-Management Registers
- PM_Master Module Instance: [2] [3] [4] [5] [6] [7]

Table 5-118. SEQ_ADD_WARM

Address Offset	0x22-0x22 in 0x9 byte increments		
Physical Address	0x0000 0058-0x0000 0058	**Instance**	PM_MASTER
Description	Memory address of SLEEP-to-ACTIVE sequence base add (VRRTC domain) Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		SEQ_ADD					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:0	SEQ_ADD	Memory address for transition start step	RW	0x00

Table 5-119. Register Call Summary for Register SEQ_ADD_WARM

Reset and Power-Management Integration
- Resets: [0] [1]

Reset and Power-Management Registers
- PM_Master Module Instance: [2] [3] [4] [5] [6] [7]

Table 5-120. MEMORY_ADDRESS

Address Offset	0x23-0x23 in 0x9 byte increments		
Physical Address	0x0000 0059-0x0000 0059	**Instance**	PM_MASTER
Description	Select the memory location to be updated (VRRTC domain). Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ADDRESS							

Bits	Field Name	Description	Type	Reset
7:0	ADDRESS	The first 6 MSBs define which sequence word (memory) is accessed (there are 64 memories). The last 2 LSBs define which 8-bit word (there are four in each sequence word/memory) is addressed.	RW	0x00

Table 5-121. Register Call Summary for Register MEMORY_ADDRESS

Reset and Power-Management Integration
- Resets: [0] [1] [2]

Reset and Power Management Functional Description
- Power-Management Sequencing Memory Structure: [3]

Reset and Power-Management Programming Model
- Reset and Power-Management Programming Model: [4] [5]
- Programming Example for Skipping an Address: [6] [7] [8] [9]
- Programming Example for Adding a Delay: [10]

Reset and Power-Management Registers
- PM_Master Module Instance: [11] [12] [13] [14] [15] [16] [17]

Table 5-122. MEMORY_DATA

Address Offset	0x24-0x24 in 0x9 byte increments		
Physical Address	0x0000 005A-0x0000 005A	**Instance**	PM_MASTER
Description	Data to write in the selected memory address (VRRTC domain)		
	Write-protected with the KEY_CFG		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0

Bits	Field Name	Description	Type	Reset
7:0	MEMORY_DATA	Memory data when accessing the MEMORY_DATA register. The MEMORY_ADDRESS is automatically incremented.	RW	0x18

Table 5-123. Register Call Summary for Register MEMORY_DATA

Reset and Power-Management Integration • Resets: [0] [1]
Reset and Power Management Functional Description • Power-Management Sequencing Memory Structure: [2]
Reset and Power-Management Programming Model • Reset and Power-Management Programming Model: [3] [4] • Programming Example for Skipping an Address: [5] • Programming Example for Adding a Delay: [6]
Reset and Power-Management Registers • PM_Master Module Instance: [7] [8] [9] [10] [11] [12] [13] [14]

5.6.3 PM_RECEIVER Module Instance

This section provides information about the PM_RECEIVER module instance in this product. Table 5-125 summarizes the register access for the different modes, Table 5-126 summarizes the receiver mode, Table 5-127 summarizes the master mode for the secure mode, and Table 5-128 summarizes the master mode for the unsecure mode. Table 5-130 through Table 5-430 describe the register bits.

VRRTC Domain

Table 5-124. PM_RECEIVER Mode Overview

Address Offset	Address Offset			
	SECURE		UNSECURE	
	READ	WRITE	READ	WRITE
0x00	SC_CONFIG	SC_CONFIG	SC_CONFIG	SC_CONFIG
0x01	SC_DETECT1	SC_DETECT1	SC_DETECT1	SC_DETECT1
0x02	SC_DETECT2	SC_DETECT2	SC_DETECT2	SC_DETECT2
0x03	WATCHDOG_CF	WATCHDOG_CF	WATCHDOG_CF	WATCHDOG_CF
0x04	IT_CHECK_CFG	IT_CHECK_CFG	IT_CHECK_CFG	IT_CHECK_CFG
0x05	VIBRATOR_CFG	VIBRATOR_CFG	VIBRATOR_CFG	VIBRATOR_CFG
0x06	dc-to-dc_GLOBAL_CFG	dc-to-dc_GLOBAL_CFG	dc-to-dc_GLOBAL_CFG	dc-to-dc_GLOBAL_CFG
0x07	VDD1_TRIM1	VDD1_TRIM1	VDD1_TRIM1	VDD1_TRIM1
0x08	VDD1_TRIM2	VDD1_TRIM2	VDD1_TRIM2	VDD1_TRIM2
0x09	VDD2_TRIM1	VDD2_TRIM1	VDD2_TRIM1	VDD2_TRIM1

Table 5-124. PM_RECEIVER Mode Overview (continued)

Address Offset	Address Offset			
	SECURE		UNSECURE	
	READ	WRITE	READ	WRITE
0x0A	VDD2_TRIM2	VDD2_TRIM2	VDD2_TRIM2	VDD2_TRIM2
0x0B	VIO_TRIM1	VIO_TRIM1	VIO_TRIM1	VIO_TRIM1
0x0C	VIO_TRIM2	VIO_TRIM2	VIO_TRIM2	VIO_TRIM2
0x0D	MISC_CFG	MISC_CFG	MISC_CFG	MISC_CFG
0x0E	LS_TST_A	LS_TST_A	LS_TST_A	LS_TST_A
0x0F	LS_TST_B	LS_TST_B	LS_TST_B	LS_TST_B
0x10	LS_TST_C	LS_TST_C	LS_TST_C	LS_TST_C
0x11	LS_TST_D	LS_TST_D	LS_TST_D	LS_TST_D
0x12	BB_CFG	BB_CFG	BB_CFG	BB_CFG
0x13	MISC_TST	MISC_TST	MISC_TST	MISC_TST
0x14	TRIM1	TRIM1	TRIM1	TRIM1
0x15	TRIM2	TRIM2	TRIM2	TRIM2
0x16	DC/DC_TIMEOUT	DC/DC_TIMEOUT	DC/DC_TIMEOUT	DC/DC_TIMEOUT
0x17	VAUX1_DEV_GRP	VAUX1_DEV_GRP	VAUX1_DEV_GRP	VAUX1_DEV_GRP
0x18	VAUX1_TYPE	VAUX1_TYPE	VAUX1_TYPE	VAUX1_TYPE
0x19	VAUX1_REMAP	VAUX1_REMAP	VAUX1_REMAP	VAUX1_REMAP
0x1A	VAUX1_DEDICATED	VAUX1_DEDICATED	VAUX1_DEDICATED	VAUX1_DEDICATED
0x1B	VAUX2_DEV_GRP	-	VAUX2_DEV_GRP	VAUX2_DEV_GRP
0x1C	VAUX2_TYPE	VAUX2_TYPE	VAUX2_TYPE	VAUX2_TYPE
0x1D	VAUX2_REMAP	VAUX2_REMAP	VAUX2_REMAP	VAUX2_REMAP
0x1E	VAUX2_DEDICATED	VAUX2_DEDICATED	VAUX2_DEDICATED	VAUX2_DEDICATED
0x1F	VAUX3_DEV_GRP	VAUX3_DEV_GRP	VAUX3_DEV_GRP	VAUX3_DEV_GRP
0x20	VAUX3_TYPE	VAUX3_TYPE	VAUX3_TYPE	VAUX3_TYPE
0x21	VAUX3_REMAP	VAUX3_REMAP	VAUX3_REMAP	VAUX3_REMAP
0x22	VAUX3_DEDICATED	VAUX3_DEDICATED	VAUX3_DEDICATED	VAUX3_DEDICATED
0x23	VAUX4_DEV_GRP	VAUX4_DEV_GRP	VAUX4_DEV_GRP	VAUX4_DEV_GRP
0x24	VAUX4_TYPE	VAUX4_TYPE	VAUX4_TYPE	VAUX4_TYPE
0x25	VAUX4_REMAPv	VAUX4_REMAPv	VAUX4_REMAPv	VAUX4_REMAPv
0x26	VAUX4_DEDICATED	VAUX4_DEDICATED	VAUX4_DEDICATED	VAUX4_DEDICATED
0x27	VMMC1_DEV_GRP	VMMC1_DEV_GRP	VMMC1_DEV_GRP	VMMC1_DEV_GRP
0x28	VMMC1_TYPE	VMMC1_TYPE	VMMC1_TYPE	VMMC1_TYPE
0x29	VMMC1_REMAP	VMMC1_REMAP	VMMC1_REMAP	VMMC1_REMAP
0x2A	VMMC1_DEDICATED	VMMC1_DEDICATED	VMMC1_DEDICATED	VMMC1_DEDICATED
0x2B	VMMC2_DEV_GRP	VMMC2_DEV_GRP	VMMC2_DEV_GRP	VMMC2_DEV_GRP
0x2C	VMMC2_TYPE	VMMC2_TYPE	VMMC2_TYPE	VMMC2_TYPE
0x2D	MMC2_REMAP	MMC2_REMAP	MMC2_REMAP	MMC2_REMAP
0x2E	VMMC2_DEDICATED	VMMC2_DEDICATED	VMMC2_DEDICATED	VMMC2_DEDICATED
0x2F	VPLL1_DEV_GRP	VPLL1_DEV_GRP	VPLL1_DEV_GRP	VPLL1_DEV_GRP
0x30	VPLL1_TYPE	VPLL1_TYPE	VPLL1_TYPE	VPLL1_TYPE
0x31	VPLL1_REMAP	VPLL1_REMAP	VPLL1_REMAP	VPLL1_REMAP
0x32	VPLL1_DEDICATED	VPLL1_DEDICATED	VPLL1_DEDICATED	VPLL1_DEDICATED
0x33	VPLL2_DEV_GRP	VPLL2_DEV_GRP	VPLL2_DEV_GRP	VPLL2_DEV_GRP
0x34	VPLL2_TYPE	VPLL2_TYPE	VPLL2_TYPE	VPLL2_TYPE
0x35	VPLL2_REMAP	VPLL2_REMAP	VPLL2_REMAP	VPLL2_REMAP
0x36	VPLL2_DEDICATED	VPLL2_DEDICATED	VPLL2_DEDICATED	VPLL2_DEDICATED

Table 5-124. PM_RECEIVER Mode Overview (continued)

Address Offset	Address Offset			
	SECURE		UNSECURE	
	READ	WRITE	READ	WRITE
0x37	VSIM_DEV_GRP	VSIM_DEV_GRP	VSIM_DEV_GRP	VSIM_DEV_GRP
0x38	VSIM_TYPE	VSIM_TYPE	VSIM_TYPE	VSIM_TYPE
0x39	VSIM_REMAP	VSIM_REMAP	VSIM_REMAP	VSIM_REMAP
0x3A	VSIM_DEDICATED	VSIM_DEDICATED	VSIM_DEDICATED	VSIM_DEDICATED
0x3B	VDAC_DEV_GRP	VDAC_DEV_GRP	VDAC_DEV_GRP	VDAC_DEV_GRP
0x3C	VDAC_TYPE	VDAC_TYPE	VDAC_TYPE	VDAC_TYPE
0x3D	VDAC_REMAP	VDAC_REMAP	VDAC_REMAP	VDAC_REMAP
0x3E	VDAC_DEDICATED	VDAC_DEDICATED	VDAC_DEDICATED	VDAC_DEDICATED
0x3F	VINTANA1_DEV_GRP	VINTANA1_DEV_GRP	VINTANA1_DEV_GRP	VINTANA1_DEV_GRP
0x40	VINTANA1_TYPE	VINTANA1_TYPE	VINTANA1_TYPE	VINTANA1_TYPE
0x41	VINTANA1_REMAP	VINTANA1_REMAP	VINTANA1_REMAP	VINTANA1_REMAP
0x42	VINTANA1_DEDICATED	VINTANA1_DEDICATED	VINTANA1_DEDICATED	VINTANA1_DEDICATED
0x43	VINTANA2_DEV_GRP	VINTANA2_DEV_GRP	VINTANA2_DEV_GRP	VINTANA2_DEV_GRP
0x44	VINTANA2_TYPE	VINTANA2_TYPE	VINTANA2_TYPE	VINTANA2_TYPE
0x45	VINTANA2_REMAP	VINTANA2_REMAP	VINTANA2_REMAP	VINTANA2_REMAP
0x46	VINTANA2_DEDICATED	VINTANA2_DEDICATED	VINTANA2_DEDICATED	VINTANA2_DEDICATED
0x47	VINTDIG_DEV_GRP	VINTDIG_DEV_GRP	VINTDIG_DEV_GRP	VINTDIG_DEV_GRP
0x48	VINTDIG_TYPE	VINTDIG_TYPE	VINTDIG_TYPE	VINTDIG_TYPE
0x49	VINTDIG_REMAP	VINTDIG_REMAP	VINTDIG_REMAP	VINTDIG_REMAP
0x4A	VINTDIG_DEDICATED	VINTDIG_DEDICATED	VINTDIG_DEDICATED	VINTDIG_DEDICATED
0x4B	VIO_DEV_GRP	VIO_DEV_GRP	VIO_DEV_GRP	VIO_DEV_GRP
0x4C	VIO_TYPE	VIO_TYPE	VIO_TYPE	VIO_TYPE
0x4D	VIO_REMAP	VIO_REMAP	VIO_REMAP	VIO_REMAP
0x4E	VIO_CFG	VIO_CFG	VIO_CFG	VIO_CFG
0x4F	VIO_MISC_CFG	VIO_MISC_CFG	VIO_MISC_CFG	VIO_MISC_CFG
0x50	VIO_TEST1	VIO_TEST1	VIO_TEST1	VIO_TEST1
0x51	VIO_TEST2	VIO_TEST2	VIO_TEST2	VIO_TEST2
0x52	VIO_OSC	VIO_OSC	VIO_OSC	VIO_OSC
0x53	VIO_RESERVED	VIO_RESERVED	VIO_RESERVED	VIO_RESERVED
0x54	VIO_VSEL	VIO_VSEL	VIO_VSEL	VIO_VSEL
0x55	VDD1_DEV_GRP	VDD1_DEV_GRP	VDD1_DEV_GRP	VDD1_DEV_GRP
0x56	VDD1_TYPE	VDD1_TYPE	VDD1_TYPE	VDD1_TYPE
0x57	VDD1_REMAP	VDD1_REMAP	VDD1_REMAP	VDD1_REMAP
0x58	VDD1_CFG	VDD1_CFG	VDD1_CFG	VDD1_CFG
0x59	VDD1_MISC_CFG	VDD1_MISC_CFG	VDD1_MISC_CFG	VDD1_MISC_CFG
0x5A	VDD1_TEST1	VDD1_TEST1	VDD1_TEST1	VDD1_TEST1
0x5B	VDD1_TEST2	VDD1_TEST2	VDD1_TEST2	VDD1_TEST2
0x5C	VDD1_OSC	VDD1_OSC	VDD1_OSC	VDD1_OSC
0x5D	VDD1_RESERVED	VDD1_RESERVED	VDD1_RESERVED	VDD1_RESERVED
0x5E	VDD1_VSEL	VDD1_VSEL	VDD1_VSEL	VDD1_VSEL
0x5F	VDD1_VMODE_CFG	VDD1_VMODE_CFG	VDD1_VMODE_CFG	VDD1_VMODE_CFG
0x60	VDD1_VFLOOR	VDD1_VFLOOR	VDD1_VFLOOR	VDD1_VFLOOR
0x61	VDD1_VROOF	VDD1_VROOF	VDD1_VROOF	VDD1_VROOF

Table 5-124. PM_RECEIVER Mode Overview (continued)

Address Offset	Address Offset			
	SECURE		UNSECURE	
	READ	WRITE	READ	WRITE
0x62	VDD1_STEP	VDD1_STEP	VDD1_STEP	VDD1_STEP
0x63	VDD2_DEV_GRP	VDD2_DEV_GRP	VDD2_DEV_GRP	VDD2_DEV_GRP
0x64	VDD2_TYPE	VDD2_TYPE	VDD2_TYPE	VDD2_TYPE
0x65	VDD2_REMAP	VDD2_REMAP	VDD2_REMAP	VDD2_REMAP
0x66	VDD2_CFG	VDD2_CFG	VDD2_CFG	VDD2_CFG
0x67	VDD2_MISC_CFG	VDD2_MISC_CFG	VDD2_MISC_CFG	VDD2_MISC_CFG
0x68	VDD2_TEST1	VDD2_TEST1	VDD2_TEST1	VDD2_TEST1
0x69	VDD2_TEST2	VDD2_TEST2	VDD2_TEST2	VDD2_TEST2
0x6A	VDD2_OSC	VDD2_OSC	VDD2_OSC	VDD2_OSC
0x6B	VDD2_RESERVED	VDD2_RESERVED	VDD2_RESERVED	VDD2_RESERVED
0x6C	VDD2_VSEL	VDD2_VSEL	VDD2_VSEL	VDD2_VSEL
0x6D	VDD2_VMODE_CFG	VDD2_VMODE_CFG	VDD2_VMODE_CFG	VDD2_VMODE_CFG
0x6E	VDD2_VFLOOR	VDD2_VFLOOR	VDD2_VFLOOR	VDD2_VFLOOR
0x6F	VDD2_VROOF	VDD2_VROOF	VDD2_VROOF	VDD2_VROOF
0x70	VDD2_STEP	VDD2_STEP	VDD2_STEP	VDD2_STEP
0x71	VUSB1V5_DEV_GRP	VUSB1V5_DEV_GRP	VUSB1V5_DEV_GRP	VUSB1V5_DEV_GRP
0x72	VUSB1V5_TYPE	VUSB1V5_TYPE	VUSB1V5_TYPE	VUSB1V5_TYPE
0x73	VUSB1V5_REMAP	VUSB1V5_REMAP	VUSB1V5_REMAP	VUSB1V5_REMAP
0x74	VUSB1V8_DEV_GRP	VUSB1V8_DEV_GRP	VUSB1V8_DEV_GRP	VUSB1V8_DEV_GRP
0x75	VUSB1V8_TYPE	VUSB1V8_TYPE	VUSB1V8_TYPE	VUSB1V8_TYPE
0x76	VUSB1V8_REMAP	VUSB1V8_REMAP	VUSB1V8_REMAP	VUSB1V8_REMAP
0x77	VUSB3V1_DEV_GRP	VUSB3V1_DEV_GRP	VUSB3V1_DEV_GRP	VUSB3V1_DEV_GRP
0x78	VUSB3V1_TYPE	VUSB3V1_TYPE	VUSB3V1_TYPE	VUSB3V1_TYPE
0x79	VUSB3V1_REMAP	VUSB3V1_REMAP	VUSB3V1_REMAP	VUSB3V1_REMAP
0x7A	VUSBCP_DEV_GRP	VUSBCP_DEV_GRP	VUSBCP_DEV_GRP	VUSBCP_DEV_GRP
0x7B	VUSBCP_TYPE	VUSBCP_TYPE	VUSBCP_TYPE	VUSBCP_TYPE
0x7C	VUSBCP_REMAP	VUSBCP_REMAP	VUSBCP_REMAP	VUSBCP_REMAP
0x7D	VUSB_DEDICATED1	VUSB_DEDICATED1	VUSB_DEDICATED1	VUSB_DEDICATED1
0x7E	VUSB_DEDICATED2	VUSB_DEDICATED2	VUSB_DEDICATED2	VUSB_DEDICATED2
0x7F	REGEN_DEV_GRP	REGEN_DEV_GRP	REGEN_DEV_GRP	REGEN_DEV_GRP
0x80	REGEN_TYPE	REGEN_TYPE	REGEN_TYPE	REGEN_TYPE
0x81	REGEN_REMAP	REGEN_REMAP	REGEN_REMAP	REGEN_REMAP
0x82	NRESPWRON_DEV_GRP	NRESPWRON_DEV_GRP	NRESPWRON_DEV_GRP	NRESPWRON_DEV_GRP
0x83	NRESPWRON_TYPE	NRESPWRON_TYPE	NRESPWRON_TYPE	NRESPWRON_TYPE
0x84	NRESPWRON_REMAP	NRESPWRON_REMAP	NRESPWRON_REMAP	NRESPWRON_REMAP
0x85	CLKEN_DEV_GRP	CLKEN_DEV_GRP	CLKEN_DEV_GRP	CLKEN_DEV_GRP
0x86	CLKEN_TYPE	CLKEN_TYPE	CLKEN_TYPE	CLKEN_TYPE
0x87	CLKEN_REMAP	CLKEN_REMAP	CLKEN_REMAP	CLKEN_REMAP
0x88	SYSEN_DEV_GRP	SYSEN_DEV_GRP	SYSEN_DEV_GRP	SYSEN_DEV_GRP
0x89	SYSEN_TYPE	SYSEN_TYPE	SYSEN_TYPE	SYSEN_TYPE
0x8A	SYSEN_REMAP	SYSEN_REMAP	SYSEN_REMAP	SYSEN_REMAP
0x8B	HFCLKOUT_DEV_GRP	HFCLKOUT_DEV_GRP	HFCLKOUT_DEV_GRP	HFCLKOUT_DEV_GRP
0x8C	HFCLKOUT_TYPE	HFCLKOUT_TYPE	HFCLKOUT_TYPE	HFCLKOUT_TYPE

Table 5-124. PM_RECEIVER Mode Overview (continued)

Address Offset	Address Offset			
	SECURE		UNSECURE	
	READ	WRITE	READ	WRITE
0x8D	HFCLKOUT_REMAP	HFCLKOUT_REMAP	HFCLKOUT_REMAP	HFCLKOUT_REMAP
0x8E	32KCLKOUT_DEV_GRP	32KCLKOUT_DEV_GRP	32KCLKOUT_DEV_GRP	32KCLKOUT_DEV_GRP
0x8F	32KCLKOUT_TYPE	32KCLKOUT_TYPE	32KCLKOUT_TYPE	32KCLKOUT_TYPE
0x90	32KCLKOUT_REMAP	32KCLKOUT_REMAP	32KCLKOUT_REMAP	32KCLKOUT_REMAP
0x91	TRITON_RESET_DEV_GRP	TRITON_RESET_DEV_GRP	TRITON_RESET_DEV_GRP	TRITON_RESET_DEV_GRP
0x92	TRITON_RESET_TYPE	TRITON_RESET_TYPE	TRITON_RESET_TYPE	TRITON_RESET_TYPE
0x93	TRITON_RESET_REMAP	TRITON_RESET_REMAP	TRITON_RESET_REMAP	TRITON_RESET_REMAP
0x94	MAINREF_DEV_GRP	MAINREF_DEV_GRP	MAINREF_DEV_GRP	MAINREF_DEV_GRP
0x95	MAINREF_TYPE	MAINREF_TYPE	MAINREF_TYPE	MAINREF_TYPE
0x96	MAINREF_REMAP	MAINREF_REMAP	MAINREF_REMAP	MAINREF_REMAP

Table 5-125. PM_RECEIVER Mode Summary

Mode Name	Condition
SECURE	
UNSECURE	

Table 5-126. PM_RECEIVER Register Summary for SECURE Mode Active

Register Name	Type	Register Width (Bits)	Physical Address
SC_CONFIG	RW	8	0x0000 005B-0x0000 005B
SC_DETECT1	RW	8	0x0000 005C-0x0000 005C
SC_DETECT2	RW	8	0x0000 005D-0x0000 005D
WATCHDOG_CFG	RW	8	0x0000 005E-0x0000 005E
IT_CHECK_CFG	RW	8	0x0000 005F-0x0000 005F
VIBRATOR_CFG	RW	8	0x0000 005F-0x0000 005F
dc-to-dc_GLOBAL_CFG	RW	8	0x0000 0061-0x0000 0061
VDD1_TRIM1	RW	8	0x0000 0062-0x0000 0062
VDD1_TRIM2	RW	8	0x0000 0063-0x0000 0063
VDD2_TRIM1	RW	8	0x0000 0064-0x0000 0064
VDD2_TRIM2	RW	8	0x0000 0065-0x0000 0065
VIO_TRIM1	RW	8	0x0000 0066-0x0000 0066
VIO_TRIM2	RW	8	0x0000 0067-0x0000 0067
MISC_CFG	RW	8	0x0000 0068-0x0000 0068
LS_TST_A	RW	8	0x0000 0069-0x0000 0069
LS_TST_B	RW	8	0x0000 006A-0x0000 006A
LS_TST_C	RW	8	0x0000 006B-0x0000 006B
LS_TST_D	RW	8	0x0000 006C-0x0000 006C
BB_CFG	RW	8	0x0000 006D-0x0000 006D
MISC_TST	RW	8	0x0000 006E-0x0000 006E
TRIM1	RW	8	0x0000 006F-0x0000 006F
TRIM2	RW	8	0x0000 0070-0x0000 0070
DC/DC_TIMEOUT	RW	8	0x0000 0071-0x0000 0071

Table 5-126. PM_RECEIVER Register Summary for SECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
VAUX1_DEV_GRP	RW	8	0x0000 0072-0x0000 0072
VAUX1_TYPE	RW	8	0x0000 0073-0x0000 0073
VAUX1_REMAP	RW	8	0x0000 0074-0x0000 0074
VAUX1_DEDICATED	RW	8	0x0000 0075-0x0000 0075
VAUX2_DEV_GRP	R	8	0x0000 0076-0x0000 0076
VAUX2_TYPE	RW	8	0x0000 0077-0x0000 0077
VAUX2_REMAP	RW	8	0x0000 0078-0x0000 0078
VAUX2_DEDICATED	RW	8	0x0000 0079-0x0000 0079
VAUX3_DEV_GRP	RW	8	0x0000 007A-0x0000 007A
VAUX3_TYPE	RW	8	0x0000 007B-0x0000 007B
VAUX3_REMAP	RW	8	0x0000 007C-0x0000 007C
VAUX3_DEDICATED	RW	8	0x0000 007D-0x0000 007D
VAUX4_DEV_GRP	RW	8	0x0000 007E-0x0000 007E
VAUX4_TYPE	RW	8	0x0000 007F-0x0000 007F
VAUX4_REMAP	RW	8	0x0000 0080-0x0000 0080
VAUX4_DEDICATED	RW	8	0x0000 0081-0x0000 0081
VMMC1_DEV_GRP	RW	8	0x0000 0082-0x0000 0082
VMMC1_TYPE	RW	8	0x0000 0083-0x0000 0083
VMMC1_REMAP	RW	8	0x0000 0084-0x0000 0084
VMMC1_DEDICATED	RW	8	0x0000 0085-0x0000 0085
VMMC2_DEV_GRP	RW	8	0x0000 0086-0x0000 0086
VMMC2_TYPE	RW	8	0x0000 0087-0x0000 0087
VMMC2_REMAP	RW	8	0x0000 0088-0x0000 0088
VMMC2_DEDICATED	RW	8	0x0000 0089-0x0000 0089
VPLL1_DEV_GRP	RW	8	0x0000 008A-0x0000 008A
VPLL1_TYPE	RW	8	0x0000 008B-0x0000 008B
VPLL1_REMAP	RW	8	0x0000 008C-0x0000 008C
VPLL1_DEDICATED	RW	8	0x0000 008D-0x0000 008D
VPLL2_DEV_GRP	RW	8	0x0000 008D-0x0000 008D
VPLL2_TYPE	RW	8	0x0000 008F-0x0000 008F
VPLL2_REMAP	RW	8	0x0000 0090-0x0000 0090
VPLL2_DEDICATED	RW	8	0x0000 0091-0x0000 0091
VSIM_DEV_GRP	RW	8	0x0000 0092-0x0000 0092
VSIM_TYPE	RW	8	0x0000 0093-0x0000 0093
VSIM_REMAP	RW	8	0x0000 0094-0x0000 0094
VSIM_DEDICATED	RW	8	0x0000 0095-0x0000 0095
VDAC_DEV_GRP	RW	8	0x0000 0096-0x0000 0096
VDAC_TYPE	RW	8	0x0000 0097-0x0000 0097
VDAC_REMAP	RW	8	0x0000 0098-0x0000 0098
VDAC_DEDICATED	RW	8	0x0000 0099-0x0000 0099
VINTANA1_DEV_GRP	RW	8	0x0000 009A-0x0000 009A
VINTANA1_TYP	RW	8	0x0000 009B-0x0000 009B
VINTANA1_REMAP	RW	8	0x0000 009C-0x0000 009C
VINTANA1_DEDICATED	RW	8	0x0000 009D-0x0000 009D
VINTANA2_DEV_GRP	RW	8	0x0000 009E-0x0000 009E
VINTANA2_TYPE	RW	8	0x0000 009F-0x0000 009F
VINTANA2_REMAP	RW	8	0x0000 00A0-0x0000 00A0

Table 5-126. PM_RECEIVER Register Summary for SECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
VINTANA2_DEDICATED	RW	8	0x0000 00A1-0x0000 00A1
VINTDIG_DEV_GRP	RW	8	0x0000 00A2-0x0000 00A2
VINTDIG_TYPE	RW	8	0x0000 00A3-0x0000 00A3
VINTDIG_REMAP	RW	8	0x0000 00A4-0x0000 00A4
VINTDIG_DEDICATED	RW	8	0x0000 00A5-0x0000 00A5
VIO_DEV_GRP	RW	8	0x0000 00A6-0x0000 00A6
VIO_TYPE	RW	8	0x0000 00A7-0x0000 00A7
VIO_REMAP	RW	8	0x0000 00A8-0x0000 00A8
VIO_CFG	RW	8	0x0000 00A9-0x0000 00A9
VIO_MISC_CFG	RW	8	0x0000 00AA-0x0000 00AA
VIO_TEST1	RW	8	0x0000 00AB-0x0000 00AB
VIO_TEST2	RW	8	0x0000 00AC-0x0000 00AC
VIO_OSC	RW	8	0x0000 00AD-0x0000 00AD
VIO_RESERVED	RW	8	0x0000 00AE-0x0000 00AE
VIO_VSEL	RW	8	0x0000 00AF-0x0000 00AF
VDD1_DEV_GRP	RW	8	0x0000 00B0-0x0000 00B0
VDD1_TYPE	RW	8	0x0000 00B1-0x0000 00B1
VDD1_REMAP	RW	8	0x0000 00B2-0x0000 00B2
VDD1_CFG	RW	8	0x0000 00B3-0x0000 00B3
VDD1_MISC_CFG	RW	8	0x0000 00B4-0x0000 00B4
VDD1_TEST1	RW	8	0x0000 00B5-0x0000 00B5
VDD1_TEST2	RW	8	0x0000 00B6-0x0000 00B6
VDD1_OSC	RW	8	0x0000 00B7-0x0000 00B7
VDD1_RESERVED	RW	8	0x0000 00B8-0x0000 00B8
VDD1_VSEL	RW	8	0x0000 00B9-0x0000 00B9
VDD1_VMODE_CFG	RW	8	0x0000 00BA-0x0000 00BA
VDD1_VFLOOR	RW	8	0x0000 00BB-0x0000 00BB
VDD1_VROOF	RW	8	0x0000 00BC-0x0000 00BC
VDD1_STEP	RW	8	0x0000 00BD-0x0000 00BD
VDD2_DEV_GRP	RW	8	0x0000 00BE-0x0000 00BE
VDD2_TYPE	RW	8	0x0000 00BF-0x0000 00BF
VDD2_REMAP	RW	8	0x0000 00C0-0x0000 00C0
VDD2_CFG	RW	8	0x0000 00C1-0x0000 00C1
VDD2_MISC_CFG	RW	8	0x0000 00C2-0x0000 00C2
VDD2_TEST1	RW	8	0x0000 00C3-0x0000 00C3
VDD2_TEST2	RW	8	0x0000 00C4-0x0000 00C4
VDD2_TEST2	RW	8	0x0000 00C5-0x0000 00C5
VDD2_RESERVED	RW	8	0x0000 00C6-0x0000 00C6
VDD2_VSEL	RW	8	0x0000 00C7-0x0000 00C7
VDD2_VMODE_CFG	RW	8	0x0000 00C8-0x0000 00C8
VDD2_VFLOOR	RW	8	0x0000 00C9-0x0000 00C9
VDD2_VROOF	RW	8	0x0000 00CA-0x0000 00CA
VDD2_STEP	RW	8	0x0000 00CB-0x0000 00CB
VUSB1V5_DEV_GRP	RW	8	0x0000 00CC-0x0000 00CC
VUSB1V5_TYPE	RW	8	0x0000 00CD-0x0000 00CD
VUSB1V5_REMAP	RW	8	0x0000 00CE-0x0000 00CE
VUSB1V8_DEV_GRP	RW	8	0x0000 00CF-0x0000 00CF

Table 5-126. PM_RECEIVER Register Summary for SECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
VUSB1V8_TYPE	RW	8	0x0000 00D0-0x0000 00D0
VUSB1V8_REMAP	RW	8	0x0000 00D1-0x0000 00D1
VUSB3V1_DEV_GRP	RW	8	0x0000 00D2-0x0000 00D2
VUSB3V1_TYPE	RW	8	0x0000 00D3-0x0000 00D3
VUSB3V1_REMAP	RW	8	0x0000 00D4-0x0000 00D4
VUSBCP_DEV_GRP	RW	8	0x0000 00D5-0x0000 00D5
VUSBCP_TYPE	RW	8	0x0000 00D6-0x0000 00D6
VUSBCP_REMAP	RW	8	0x0000 00D7-0x0000 00D7
VUSB_DEDICATED1	RW	8	0x0000 00D8-0x0000 00D8
VUSB_DEDICATED2	RW	8	0x0000 00D9-0x0000 00D9
REGEN_DEV_GRP	RW	8	0x0000 00DA-0x0000 00DA
REGEN_TYPE	RW	8	0x0000 00DB-0x0000 00DB
REGEN_REMAP	RW	8	0x0000 00DC-0x0000 00DC
NRESPWRON DEV_GRP	RW	8	0x0000 00DD-0x0000 00DD
NRESPWRON_TYPE	RW	8	0x0000 00DE-0x0000 00DE
NRESPWRON_REMAP	RW	8	0x0000 00DF-0x0000 00DF
CLKEN_DEV_GRP	RW	8	0x0000 00E0-0x0000 00E0
CLKEN_TYPE	RW	8	0x0000 00E1-0x0000 00E1
CLKEN_REMAP	RW	8	0x0000 00E2-0x0000 00E2
SYSEN_DEV_GRP	RW	8	0x0000 00E3-0x0000 00E3
SYSEN_TYPE	RW	8	0x0000 00E4-0x0000 00E4
SYSEN_REMAP	RW	8	0x0000 00E5-0x0000 00E5
HFCLKOUT_DEV_GRP	RW	8	0x0000 00E6-0x0000 00E6
HFCLKOUT_TYPE	RW	8	0x0000 00E7-0x0000 00E7
HFCLKOUT_REMAP	RW	8	0x0000 00E8-0x0000 00E8
32KCLKOUT_DEV_GRP	RW	8	0x0000 00E9-0x0000 00E9
32KCLKOUT_TYPE	RW	8	0x0000 00EA-0x0000 00EA
32KCLKOUT_REMAP	RW	8	0x0000 00EB-0x0000 00EB
TRITON_RESET_DEV_GRP	RW	8	0x0000 00EC-0x0000 00EC
TRITON_RESET_TYPE	RW	8	0x0000 00ED-0x0000 00ED
TRITON_RESET_REMAP	RW	8	0x0000 00EE-0x0000 00EE
MAINREF_DEV_GRP	RW	8	0x0000 00EF-0x0000 00EF
MAINREF_TYPE	RW	8	0x0000 00F0-0x0000 00F0
MAINREF_REMAP	RW	8	0x0000 00F1-0x0000 00F1

Table 5-127. PM_RECEIVER Register Summary for UNSECURE Mode Active

Register Name	Type	Register Width (Bits)	Physical Address
SC_CONFIG	RW	8	0x0000 005B-0x0000 005B
SC_DETECT1	RW	8	0x0000 005C-0x0000 005C
SC_DETECT2	RW	8	0x0000 005D-0x0000 005D
WATCHDOG_CFG	RW	8	0x0000 005E-0x0000 005E
IT_CHECK_CFG	RW	8	0x0000 005F-0x0000 005F
VIBRATOR_CFG	RW	8	0x0000 0060-0x0000 0060
dc-to-dc_GLOBAL_CFG	RW	8	0x0000 0061-0x0000 0061
VDD1_TRIM1	RW	8	0x0000 0062-0x0000 0062
VDD1_TRIM2	RW	8	0x0000 0063-0x0000 0063

Table 5-127. PM_RECEIVER Register Summary for UNSECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
VDD2_TRIM1	RW	8	0x0000 0064-0x0000 0064
VDD2_TRIM2	RW	8	0x0000 0065-0x0000 0065
VIO_TRIM1	RW	8	0x0000 0066-0x0000 0066
VIO_TRIM2	RW	8	0x0000 0067-0x0000 0067
MISC_CFG	RW	8	0x0000 0068-0x0000 0068
LS_TST_A	RW	8	0x0000 0069-0x0000 0069
LS_TST_B	RW	8	0x0000 006A-0x0000 006A
LS_TST_C	RW	8	0x0000 006B-0x0000 006B
LS_TST_D	RW	8	0x0000 006C-0x0000 006C
BB_CFG	RW	8	0x0000 006D-0x0000 006D
MISC_TST	RW	8	0x0000 006E-0x0000 006E
TRIM1	RW	8	0x0000 006F-0x0000 006F
TRIM2	RW	8	0x0000 0070-0x0000 0070
DC/DC_TIMEOUT	RW	8	0x0000 0071-0x0000 0071
VAUX1_DEV_GRP	RW	8	0x0000 0072-0x0000 0072
VAUX1_TYPE	RW	8	0x0000 0073-0x0000 0073
VAUX1_REMAP	RW	8	0x0000 0074-0x0000 0074
VAUX1_DEDICATED	RW	8	0x0000 0075-0x0000 0075
VAUX2_DEV_GRP	RW	8	0x0000 0076-0x0000 0076
VAUX2_TYPE	RW	8	0x0000 0077-0x0000 0077
VAUX2_REMAP	RW	8	0x0000 0078-0x0000 0078
VAUX2_DEDICATED	RW	8	0x0000 0079-0x0000 0079
VAUX3_DEV_GRP	RW	8	0x0000 007A-0x0000 007A
VAUX3_TYPE	RW	8	0x0000 007B-0x0000 007B
VAUX3_REMAP	RW	8	0x0000 007C-0x0000 007C
VAUX3_DEDICATED	RW	8	0x0000 007D-0x0000 007D
VAUX4_DEV_GRP	RW	8	0x0000 007E-0x0000 007E
VAUX4_TYPE	RW	8	0x0000 007F-0x0000 007F
VAUX4_REMAP	RW	8	0x0000 0080-0x0000 0080
VAUX4_DEDICATED	RW	8	0x0000 0081-0x0000 0081
VMMC1_DEV_GRP	RW	8	0x0000 0082-0x0000 0082
VMMC1_TYPE	RW	8	0x0000 0083-0x0000 0083
VMMC1_REMAP	RW	8	0x0000 0084-0x0000 0084
VMMC1_DEDICATED	RW	8	0x0000 0085-0x0000 0085
VMMC2_DEV_GRP	RW	8	0x0000 0086-0x0000 0086
VMMC2_TYPE	RW	8	0x0000 0087-0x0000 0087
VMMC2_REMAP	RW	8	0x0000 0088-0x0000 0088
VMMC2_DEDICATED	RW	8	0x0000 0089-0x0000 0089
VPLL1_DEV_GRP	RW	8	0x0000 008A-0x0000 008A
VPLL1_TYPE	RW	8	0x0000 008B-0x0000 008B
VPLL1_REMAP	RW	8	0x0000 008C-0x0000 008C
VPLL1_DEDICATED	RW	8	0x0000 008D-0x0000 008D
VPLL2_DEV_GRP	RW	8	0x0000 008E-0x0000 008E
VPLL2_TYPE	RW	8	0x0000 008F-0x0000 008F
VPLL2_REMAP	RW	8	0x0000 0090-0x0000 0090
VPLL2_DEDICATED	RW	8	0x0000 0091-0x0000 0091
VSIM_DEV_GRP	RW	8	0x0000 0092-0x0000 0092

Table 5-127. PM_RECEIVER Register Summary for UNSECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
VSIM_TYPE	RW	8	0x0000 0093-0x0000 0093
VSIM_REMAP	RW	8	0x0000 0094-0x0000 0094
VSIM_DEDICATED	RW	8	0x0000 0095-0x0000 0095
VDAC_DEV_GRP	RW	8	0x0000 0096-0x0000 0096
VDAC_TYPE	RW	8	0x0000 0097-0x0000 0097
VDAC_REMAP	RW	8	0x0000 0098-0x0000 0098
VDAC_DEDICATED	RW	8	0x0000 0099-0x0000 0099
VINTANA1_DEV_GRP	RW	8	0x0000 009A-0x0000 009A
VINTANA1_TYPE	RW	8	0x0000 009B-0x0000 009B
VINTANA1_REMAP	RW	8	0x0000 009C-0x0000 009C
VINTANA1_DEDICATED	RW	8	0x0000 009D-0x0000 009D
VINTANA2_DEV_GRP	RW	8	0x0000 009E-0x0000 009E
VINTANA2_TYPE	RW	8	0x0000 009F-0x0000 009F
VINTANA2_REMAP	RW	8	0x0000 00A0-0x0000 00A0
VINTANA2_DEDICATED	RW	8	0x0000 00A1-0x0000 00A1
VINTDIG_DEV_GRP	RW	8	0x0000 00A2-0x0000 00A2
VINTDIG_TYPE	RW	8	0x0000 00A3-0x0000 00A3
VINTDIG_REMAP	RW	8	0x0000 00A4-0x0000 00A4
VINTDIG_DEDICATED	RW	8	0x0000 00A5-0x0000 00A5
VIO_DEV_GRP	RW	8	0x0000 00A6-0x0000 00A6
VIO_TYPE	RW	8	0x0000 00A7-0x0000 00A7
VIO_REMAP	RW	8	0x0000 00A8-0x0000 00A8
VIO_CFG	RW	8	0x0000 00A9-0x0000 00A9
VIO_MISC_CFG	RW	8	0x0000 00AA-0x0000 00AA
VIO_TEST1	RW	8	0x0000 00AB-0x0000 00AB
VIO_TEST2	RW	8	0x0000 00AC-0x0000 00AC
VIO_OSC	RW	8	0x0000 00AD-0x0000 00AD
VIO_RESERVED	RW	8	0x0000 00AE-0x0000 00AE
VIO_VSEL	RW	8	0x0000 00AF-0x0000 00AF
VDD1_DEV_GRP	RW	8	0x0000 00B0-0x0000 00B0
VDD1_TYPE	RW	8	0x0000 00B1-0x0000 00B1
VDD1_REMAP	RW	8	0x0000 00B2-0x0000 00B2
VDD1_CFG	RW	8	0x0000 00B3-0x0000 00B3
VDD1_MISC_CFG	RW	8	0x0000 00B4-0x0000 00B4
VDD1_TEST1	RW	8	0x0000 00B5-0x0000 00B5
VDD1_TEST2	RW	8	0x0000 00B6-0x0000 00B6
VDD1_OSC	RW	8	0x0000 00B7-0x0000 00B7
VDD1_RESERVED	RW	8	0x0000 00B8-0x0000 00B8
VDD1_VSEL	RW	8	0x0000 00B9-0x0000 00B9
VDD1_VMODE_CFG	RW	8	0x0000 00BA-0x0000 00BA
VDD1_VFLOOR	RW	8	0x0000 00BB-0x0000 00BB
VDD1_VROOF	RW	8	0x0000 00BC-0x0000 00BC
VDD1_STEP	RW	8	0x0000 00BD-0x0000 00BD
VDD2_DEV_GRP	RW	8	0x0000 00BE-0x0000 00BE
VDD2_TYPE	RW	8	0x0000 00BF-0x0000 00BF
VDD2_REMAP	RW	8	0x0000 00C0-0x0000 00C0
VDD2_CFG	RW	8	0x0000 00C1-0x0000 00C1

Table 5-127. PM_RECEIVER Register Summary for UNSECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
VDD2_MISC_CFG	RW	8	0x0000 00C2-0x0000 00C2
VDD2_TEST1	RW	8	0x0000 00C3-0x0000 00C3
VDD2_TEST2	RW	8	0x0000 00C4-0x0000 00C4
VDD2_OSC	RW	8	0x0000 00C5-0x0000 00C5
VDD2_RESERVED	RW	8	0x0000 00C6-0x0000 00C6
VDD2_VSEL	RW	8	0x0000 00C7-0x0000 00C7
VDD2_VMODE_CFG	RW	8	0x0000 00C8-0x0000 00C8
VDD2_VFLOOR	RW	8	0x0000 00C9-0x0000 00C9
VDD2_VROOF	RW	8	0x0000 00CA-0x0000 00CA
VDD2_STEP	RW	8	0x0000 00CB-0x0000 00CB
VUSB1V5_DEV_GRP	RW	8	0x0000 00CC-0x0000 00CC
VUSB1V5_TYPE	RW	8	0x0000 00CD-0x0000 00CD
VUSB1V5_REMAP	RW	8	0x0000 00CE-0x0000 00CE
VUSB1V8_DEV_GRP	RW	8	0x0000 00CF-0x0000 00CF
VUSB1V8_TYPE	RW	8	0x0000 00D0-0x0000 00D0
VUSB1V8_REMAP	RW	8	0x0000 00D1-0x0000 00D1
VUSB3V1_DEV_GRP	RW	8	0x0000 00D2-0x0000 00D2
VUSB3V1_TYPE	RW	8	0x0000 00D3-0x0000 00D3
VUSB3V1_REMAP	RW	8	0x0000 00D4-0x0000 00D4
VUSBCP_DEV_GRP	RW	8	0x0000 00D5-0x0000 00D5
VUSBCP_TYPE	RW	8	0x0000 00D6-0x0000 00D6
VUSBCP_REMAP	RW	8	0x0000 00D7-0x0000 00D7
VUSB_DEDICATED1	RW	8	0x0000 00D8-0x0000 00D8
VUSB_DEDICATED2	RW	8	0x0000 00D9-0x0000 00D9
REGEN_DEV_GRP	RW	8	0x0000 00DA-0x0000 00DA
REGEN_TYPE	RW	8	0x0000 00DB-0x0000 00DB
REGEN_REMAP	RW	8	0x0000 00DC-0x0000 00DC
NRESPWRON_DEV_GRP	RW	8	0x0000 00DD-0x0000 00DD
NRESPWRON_TYPE	RW	8	0x0000 00DE-0x0000 00DE
NRESPWRON_REMAP	RW	8	0x0000 00DF-0x0000 00DF
CLKEN_DEV_GRP	RW	8	0x0000 00E0-0x0000 00E0
CLKEN_TYPE	RW	8	0x0000 00E1-0x0000 00E1
CLKEN_REMAP	RW	8	0x0000 00E2-0x0000 00E2
SYSEN_DEV_GRP	RW	8	0x0000 00E3-0x0000 00E3
SYSEN_TYPE	RW	8	0x0000 00E4-0x0000 00E4
SYSEN_REMAP	RW	8	0x0000 00E5-0x0000 00E5
HFCLKOUT_DEV_GRP	RW	8	0x0000 00E6-0x0000 00E6
HFCLKOUT_TYPE	RW	8	0x0000 00E7-0x0000 00E7
HFCLKOUT_REMAP	RW	8	0x0000 00E8-0x0000 00E8
32KCLKOUT_DEV_GRP	RW	8	0x0000 00E9-0x0000 00E9
32KCLKOUT_TYPE	RW	8	0x0000 00EA-0x0000 00EA
32KCLKOUT_REMAP	RW	8	0x0000 00EB-0x0000 00EB
TRITON_RESET_DEV_GRP	RW	8	0x0000 00EC-0x0000 00EC
TRITON_RESET_TYPE	RW	8	0x0000 00ED-0x0000 00ED
TRITON_RESET_REMAP	RW	8	0x0000 00EE-0x0000 00EE
MAINREF_DEV_GRP	RW	8	0x0000 00EF-0x0000 00EF
MAINREF_TYPE	RW	8	0x0000 00F0-0x0000 00F0

Table 5-127. PM_RECEIVER Register Summary for UNSECURE Mode Active (continued)

Register Name	Type	Register Width (Bits)	Physical Address
MAINREF_REMAP	RW	8	0x0000 00F1-0x0000 00F1

Table 5-128. SC_CONFIG

Address Offset	0x00-0x00 in 0x17 byte increments		
Physical Address	0x0000 005B-0x0000 005B	**Instance**	PM_RECEIVER
Description	Short-circuit configuration register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ENABLE	MODE	AUTOCUT	TEN_SEL				

Bits	Field Name	Description	Type	Reset
7	ENABLE	0: OFF 1: ACTIVE Reset when signal triton_reset_na is low (WAIT-ON state).	RW	0
6	MODE	Mode 0: sc_sel is updated every 0.083 s (from 1 to 12; 0 = Unused). 1: TEN_SEL is updated by a software write. Reset when signal triton_reset_na is low (WAIT-ON state).	RW	0
5	AUTOCUT	0: No AUTOCUT 1: LDOs/DC/DCs can be put in sleep mode or the system can go to WAIT-ON state. See the SC_DETECT1 and SC_DETECT2 registers. Reset when signal triton_reset_na is low (WAIT-ON state).	RW	0
4:0	TEN_SEL	00000: TEST_AUX1_LOWV 00001: TEST_AUX2_LOWV 00010: TEST_AUX3_LOWV 00011: TEST_AUX4_LOWV 00100: TEST_MMC1_LOWV 00101: TEST_MMC2_LOWV 00110: TEST_INTDIG_LOWV 00111: TEST_VINTANA2_LOWV 01000: TEST_PLL2_LOWV 01001: TEST_VDD1_LOWV(0) 01010: TEST_VDD2_LOWV(0) 01011: TEST_VIO_LOWV(0) 01100: TEST_VDAC_LOWV 01101: TEST_VUSB1V5_LOWV 01110: TEST_VUSB1V8_LOWV 01111: TEST_VUSB3V1_LOWV 01101: TEST_VINTANA_LOWV 01110: TEST_PLL1_LOWV 01111: TEST_POR_LOWV	RW	0x00

Bits	Field Name	Description	Type	Reset
		10000: TEST_SIM_LOWV 10001: TEST_TSHUT_LOWV 10010: TEST_TSHUT_REG_LOWV 10011: TEST_UPR_LOWV 10100: TEST_VRRTC_LOWV 10101: TEST_HFCLK_LOWV 10110: No output driven high ... 11110: No output driven high 11111: Testv_sw_ctrl (drive the TESTV pad to GND) Reset when signal triton_reset_na is low (WAIT-ON state).		

Table 5-129. Register Call Summary for Register SC_CONFIG

Reset and Power-Management Integration
- Resets: [0] [1] [2] [3] [4]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [5] [6] [7] [8] [9] [10]

Table 5-130. SC_DETECT1

Address Offset	0x01-0x01 in 0x17 byte increments		
Physical Address	0x0000 005C-0x0000 005C	**Instance**	PM_RECEIVER
Description	Short-circuit detect 1 register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_VINTANA2	RESERVED	SC_VMMC2	SC_VMMC1	SC_VAUX4	SC_VAUX3	SC_VAUX2	SC_VAUX1

Bits	Field Name	Description	Type	Reset
7	SC_VINTANA2	0: Normal operation 1: Short-circuit present; regulator goes to sleep mode if SC AUTOCUT = 1. This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	RW	0
6	RESERVED		RW	0
5	SC_VMMC2	0: Normal operation 1: Short-circuit present; regulator goes to sleep mode if SC AUTOCUT = 1. This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	RW	0
4	SC_VMMC1	0: Normal operation 1: Short-circuit present; regulator goes to sleep mode if SC AUTOCUT = 1. This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	RW	0

Bits	Field Name	Description	Type	Reset
3	SC_VAUX4	0: Normal operation 1: Short-circuit present; regulator goes to sleep mode if SC AUTOCUT = 1. This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	RW	0
2	SC_VAUX3	0: Normal operation 1: Short-circuit present; regulator goes to sleep mode if SC AUTOCUT = 1. This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	RW	0
1	SC_VAUX2	0: Normal operation 1: Short-circuit present; regulator goes to sleep mode if SC AUTOCUT = 1. This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	RW	0
0	SC_VAUX1	0: Normal operation 1: Short-circuit present; regulator goes to sleep mode if SC AUTOCUT = 1. This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	RW	0

Table 5-131. Register Call Summary for Register SC_DETECT1

Reset and Power-Management Integration • Resets: [0]
Reset and Power-Management Registers • PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6] [7] [8]

Table 5-132. SC_DETECT2

Address Offset	0x02-0x02 in 0x17 byte increments		
Physical Address	0x0000 005D-0x0000 005D	**Instance**	PM_RECEIVER
Description	Short-circuit detect 2 (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_VUSB3V1	SC_VUSB1V8	SC_VUSB1V5	SC_VDAC	SC_VIO	SC_VDD2	SC_VDD1	SC_VPLL2

Bits	Field Name	Description	Type	Reset
7	SC_VUSB3V1	0: Normal operation 1: Short-circuit present; regulator goes to sleep mode if SC AUTOCUT = 1. This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	R	0x0

Bits	Field Name	Description	Type	Reset
6	SC_VUSB1V8	0: Normal operation 1: Short-circuit present; regulator goes to off mode if SC AUTOCUT = 1. This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	R	0x0
5	SC_VUSB1V5	0: Normal operation 1: Short-circuit present; regulator goes to sleep mode if SC AUTOCUT = 1. This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	R	0x0
4	SC_VDAC	0: Normal operation 1: Short-circuit present; regulator goes to off mode if SC AUTOCUT = 1 This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	RW	0
3	SC_VIO	0: Normal operation 1: Short-circuit present; T2 goes to WAIT-ON state if SC AUTOCUT = 1 This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	RW	0
2	SC_VDD2	0: Normal operation 1: Short-circuit present; T2 goes to WAIT-ON state if SC AUTOCUT = 1 This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	RW	0
1	SC_VDD1	0: Normal operation 1: Short-circuit present; T2 goes to WAIT-ON state if SC AUTOCUT = 1 This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	RW	0
0	SC_VPLL2	0: Normal operation 1: Short-circuit present; regulator goes to sleep mode if SC AUTOCUT = 1. This bit stays 1 until the user writes it to 0. Real-time short-circuit detection value can be read from this register when SC_STATUS of the IT_CHECK_CFG register = 1.	RW	0

Table 5-133. Register Call Summary for Register SC_DETECT2

Reset and Power-Management Integration • Resets: [0]
Reset and Power-Management Registers • PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6] [7] [8]

Table 5-134. WATCHDOG_CFG

Address Offset	0x03-0x03 in 0x17 byte increments		
Physical Address	0x0000 005E-0x0000 005E	**Instance**	PM_RECEIVER
Description	Watchdog configuration register (VRRTC domain) Reset when the triton_reset_na is low (WAIT-ON state). This watchdog can stop or restart the system when there is a software or hardware issue. Reset when the triton_reset_na signal is low (WAIT-ON state). The counter is set to a value (1 to 30 seconds) and if the software does not write back a value on the counter or disable the counter (writing 0 on the watchdog), the system is reset after the specified delay. If the STARTON_SWBUG bit of any of the following registers is set to 1, the system restarts automatically: • CFG_P1_TRANSITION • CFG_P1_TRANSITION • CFG_P1_TRANSITION		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			WATCHDOG				

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:0	WATCHDOG	00000: Watchdog disabled 00001: Triton goes to WAIT-ON state. 00010: Triton goes to WAIT-ON state in 1 second. 00011: Triton goes to WAIT-ON state in 2 seconds. 00100: Triton goes to WAIT-ON state in 3 seconds. 11110: Triton goes to WAIT-ON state in 29 seconds. 11111: Triton goes to WAIT-ON state in 30 seconds. This register is updated every second: Watchdog <= Watchdog – 1 every second Reset when signal triton_reset_na is low (WAIT-ON state).	RW	0x00

Table 5-135. Register Call Summary for Register WATCHDOG_CFG

Reset and Power-Management Integration • Resets: [0] [1]
Reset and Power Management Functional Description • Event Definition: [2]
Reset and Power-Management Registers • PM_RECEIVER Module Instance: [3] [4]

Table 5-136. IT_CHECK_CFG

Address Offset	0x04-0x04 in 0x17 byte increments		
Physical Address	0x0000 005F-0x0000 005F	**Instance**	PM_RECEIVER
Description	Interrupt check configuration register (VRRTC domain) This PWRON interrupt check can stop the system when there is a software or hardware issue. When the IT check is enabled, if the PWRON interrupt is present and not cleared by the software during the IT_CHECK_DELAY (3 to 6 seconds), the system (device) restarts. If the STARTON_SWBUG bit of the one of the following registers is set to 1, the system restarts automatically: • CFG_P1_TRANSITION • CFG_P1_TRANSITION • CFG_P1_TRANSITION		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	SC_VREFA_SEL_LOWV	SC_VREFB_SEL_LOWV		SC_STATUS	IT_CHECK_DELAY		ITCHECK_ ENABLE

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	SC_VREFA_SEL_LOWV	Set short-circuit detection threshold for resources connected on channel A. Protected by power KEY_TST. 0: 0.5 V 1: 0.75 V	RW	0
5:4	SC_VREFB_SEL_LOWV	Set short-circuit detection threshold for resources connected on channel B. Protected by power KEY_TST. 00: 0.5 V 01: 0.75 V 10: 1.5 V 11: 2.0 V	RW	0x0
3	SC_STATUS	Set SC_DETECT register behavior (see SC_DETECT1 and SC_DETECT2 register descriptions). Reset when signal triton_reset_na is low (WAIT-ON state).	RW	0
2:1	IT_CHECK_DELAY	00: IT_CHECK DELAY = 3 seconds 01: IT_CHECK DELAY = 4 seconds 10: IT_CHECK DELAY = 5 seconds 11: IT_CHECK DELAY = 6 seconds Reset when signal triton_reset_na is low (WAIT-ON state).	RW	0x0
0	ITCHECK_ ENABLE	0: PWRON IT check disabled 1: PWRON IT check enabled. The device restarts if the PWRON is pressed for 4 seconds and the interrupt is not cleared by the software during the IT_CHECK_DELAY (3 to 6 seconds). Reset when signal triton_reset_na is low (WAIT-ON state).	RW	0

Table 5-137. Register Call Summary for Register IT_CHECK_CFG

Reset and Power-Management Integration • Resets: [0] [1] [2]
Reset and Power Management Functional Description • Event Definition: [3] [4]
Reset and Power-Management Registers • PM_RECEIVER Module Instance: [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25]

Table 5-138. VIBRATOR_CFG

Address Offset	0x05-0x05 in 0x17 byte increments		
Physical Address	0x0000 0060-0x0000 0060	**Instance**	PM_RECEIVER
Description	Vibrator configuration register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				VIB_CFG	VIB_PWM	VIB_DSEL	

Bits	Field Name	Description	Type	Reset
7:4	Reserved		R	0x0
3	VIB_CFG	0: VAUX1 in regulator mode. 1: VAUX1 in vibrator mode. Vibrator is enabled when VAUX1 is enabled.	RW	0
2	VIB_PWM	0: Vibrator uses the vibra_sync input. 1: Vibrator uses the PWM.	RW	0
1: 0	VIB_DSEL	00: VIB duty cycle = 100 percent 01: VIB duty cycle = 75 percent; vibrator is on for 0.1875 seconds of every 0.25 seconds. 10: VIB duty cycle = 50 percent; vibrator is on for 0.125 seconds of every 0.25 seconds. 11: VIB duty cycle = 25 percent; vibrator is on for 0.0625 seconds of every 0.25 seconds.	RW	0x0

Table 5-139. Register Call Summary for Register VIBRATOR_CFG

Reset and Power-Management Integration • Resets: [0] [1] [2]
Reset and Power-Management Programming Model • Power-Down Registers for POWER_SC Module: [3]
Reset and Power-Management Registers • PM_RECEIVER Module Instance: [4] [5] [6] [7] [8] [9]

Table 5-140. DCDC_GLOBAL_CFG

Address Offset	0x06-0x06 in 0x17 byte increments		
Physical Address	0x0000 0061-0x0000 0061	**Instance**	PM_RECEIVER
Description	DC/DC voltage regulator configuration registers (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
CARD_DETECT_ 2_LEVEL	CARD_DETECT_ 1_LEVEL	REGEN_PU_ DISABLE	SYSEN_PU_ DISABLE	SMARTREFLEX_ ENABLE	CARD_DETECT_ CFG	CLK_32K_DEGATE	CLK_HF_DEGATE

Bits	Field Name	Description	Type	Reset
7	CARD_DETECT_ 2_LEVEL	0: CD2 is active high. Card detected at high level. 1: CD2 is active low. Card detected at low level.	RW	0
6	CARD_DETECT_ 1_LEVEL	0: CD1 is active high. Card detected at high level. 1: CD1 is active low. Card detected at low level.	RW	0
5	REGEN_PU_ DISABLE	0: REGEN pullup enabled when the open drain is not driven 1: REGEN pullup never enabled	RW	0
4	SYSEN_PU_ DISABLE	0: SYSEN pullup enabled when the open drain is not driven 1: SYSEN pullup never enabled	RW	0
3	SMARTREFLEX_ ENABLE	0: SmartReflex is disabled. 1: SmartReflex is enabled. By default, pads used by SmartReflex and Vmode are assigned to Vmode. They are assigned to the SmartReflex I^2S bus only when SMARTREFLEX_ ENABLE is high.	RW	0
2	CARD_DETECT_ CFG	0: The SIM card is plugged in on GPIO1/INT1 (CD2). 1: The MMC2 card is plugged in on GPIO1/INT1 (CD2).	RW	0
1	CLK_32K_DEGATE	0: clk32kout gating is controlled by the PMC STM (default). 1: clk32kout gating is disabled. Write access to these bits only in secure mode. (MSECURE pad = 1) These bits are sync reset to 0 when NRESPWRON is driven low (usual PMC_RESET async reset).	RW	0
0	CLK_HF_DEGATE	0: clk32kout gating is controlled by the PMC STM (default). 1: clk32kout gating is disabled. Write access to these bits only in secure mode. (MSECURE pad = 1) These bits are sync reset to 0 when NRESPWRON is driven low (usual PMC_RESET async reset).	RW	0

Table 5-141. VDD1_TRIM1

Address Offset	0x07-0x07 in 0x17 byte increments		
Physical Address	0x0000 0062-0x0000 0062	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	BUCK_TRIM_ILIM			FREQ_TRIM			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:5	BUCK_TRIM_ILIM		RW	0x1
4:0	FREQ_TRIM		RW	0x0F

Table 5-142. Register Call Summary for Register VDD1_TRIM1

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-143. VDD1_TRIM2

Address Offset	0x08-0x08 in 0x17 byte increments		
Physical Address	0x0000 0063-0x0000 0063	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		BUCK_TRIM_SS		BUCK_TRIM			

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:4	BUCK_TRIM_SS		RW	0x1
3:0	BUCK_TRIM		RW	0x8

Table 5-144. Register Call Summary for Register VDD1_TRIM2

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-145. VDD2_TRIM1

Address Offset	0x09-0x09 in 0x17 byte increments		
Physical Address	0x0000 0064-0x0000 0064	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	BUCK_TRIM_ILIM		FREQ_TRIM				

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0x0
6:5	BUCK_TRIM_ILIM		RW	0x0
4:0	FREQ_TRIM		RW	0xF

Table 5-146. Register Call Summary for Register VDD2_TRIM1

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-147. VDD2_TRIM2

Address Offset	0x0A-0x0A in 0x17 byte increments		
Physical Address	0x0000 0065-0x0000 0065	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		BUCK_TRIM_SS		BUCK_TRIM			

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:4	BUCK_TRIM_SS		RW	0x0
3:0	BUCK_TRIM		RW	0x8

Table 5-148. Register Call Summary for Register VDD2_TRIM2

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-149. VIO_TRIM1

Address Offset	0x0B-0x0B in 0x17 byte increments		
Physical Address	0x0000 0066-0x0000 0066	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	BUCK_TRIM_ILIM			FREQ_TRIM			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:5	BUCK_TRIM_ILIM		RW	0x0
4:0	FREQ_TRIM		RW	0xF

Table 5-150. Register Call Summary for Register VIO_TRIM1

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-151. VIO_TRIM2

Address Offset	0x0C-0x0C in 0x17 byte increments		
Physical Address	0x0000 0067-0x0000 0067	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		BUCK_TRIM_SS		BUCK_TRIM			

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:4	BUCK_TRIM_SS		RW	0x0
3:0	BUCK_TRIM		RW	0x8

Table 5-152. Register Call Summary for Register VIO_TRIM2

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-153. MISC_CFG

Address Offset	0x0D-0x0D in 0x17 byte increments		
Physical Address	0x0000 0068-0x0000 0068	**Instance**	PM_RECEIVER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
TEMP_SEL		VINTANA2_SWITCH_AUTO	CLK_HF_DRV	RFID_EN_PU_DISABLE	RFID_EN	CLKEN2_CFG	CLKEN2_ENABLE

Bits	Field Name	Description	Type	Reset
7:6	TEMP_SEL	Hot-die interrupt temperature selection	RW	0X0
5	VINTANA2_SWITCH_AUTO	0: Switch from 2.75 V to 2.5 V if battery voltage is below 3 V is manual. 1: Automatic switch is enabled.	RW	0
4	CLK_HF_DRV	Drive capability of the pad 0: 10 pF 1: 40 pF Default value for PG 1.0 is 0.	RW	1
3	RFID_EN_PU_DISABLE	0: RFID_EN pullup enabled when the open drain is not driven 1: RFID_EN pullup never enabled (Was CLK_32K_DRV; not used.)	RW	0
2	RFID_EN	0: RFID_EN pad is set to 0. 1: RFID_EN pad is set to 1.	RW	0
1	CLKEN2_CFG	0: The CLKEN clock enable is output on CLKEN2. 1: CLKEN2 pad is a GPIO.	RW	1
0	CLKEN2_ENABLE	If CLKEN2_CFG = 1: 0: CLKEN2 = 0 1: CLKEN2 = 1 If CLKEN2_CFG = 0: No action	RW	0

Table 5-154. Register Call Summary for Register MISC_CFG

Reset and Power-Management Programming Model
- Sequencing: [0]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-155. LS_TST_A

Address Offset	0x0E-0x0E in 0x17 byte increments		
Physical Address	0x0000 0069-0x0000 0069	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
LS_VDIG_VBAT_VALUE	LS_VDIG_VBAT_FORCE	LS_VDIG_STS_USB_VALUE	LS_VDIG_STS_USB_FORCE	LS_VDIG_STS_BCI_VALUE	LS_VDIG_STS_BCI_FORCE	LS_ANA1_STS_BCI_VALUE	LS_ANA1_STS_BCI_FORCE

Bits	Field Name	Description	Type	Reset
7	LS_VDIG_VBAT_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
6	LS_VDIG_VBAT_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0
5	LS_VDIG_STS_USB_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
4	LS_VDIG_STS_USB_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0
3	LS_VDIG_STS_BCI_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
2	LS_VDIG_STS_BCI_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0
1	LS_ANA1_STS_BCI_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
0	LS_ANA1_STS_BCI_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0

Table 5-156. Register Call Summary for Register LS_TST_A

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-157. LS_TST_B

Address Offset	0x0F-0x0F in 0x17 byte increments		
Physical Address	0x0000 006A-0x0000 006A	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
LS_VUSB1V8_VBUS_RESET_VALUE	LS_VUSB1V8_VBUS_RESET_FORCE	LS_VUSB1V5_VBUS_RESET_VALUE	LS_VUSB1V5_VBUS_RESET_FORCE	LS_VANA1_VDIG_VALUE	LS_VANA1_VDIG_FORCE	LS_ANA1_VBAT_RESET_VALUE	LS_ANA1_VBAT_RESET_FORCE

Bits	Field Name	Description	Type	Reset
7	LS_VUSB1V8_VBUS_RESET_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
6	LS_VUSB1V8_VBUS_RESET_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0
5	LS_VUSB1V5_VBUS_RESET_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
4	LS_VUSB1V5_VBUS_RESET_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0
3	LS_VANA1_VDIG_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
2	LS_VANA1_VDIG_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0
1	LS_ANA1_VBAT_RESET_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
0	LS_ANA1_VBAT_RESET_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0

Table 5-158. Register Call Summary for Register LS_TST_B

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-159. LS_TST_C

Address Offset	0x10-0x10 in 0x17 byte increments		
Physical Address	0x0000 006B-0x0000 006B	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
LS_VUSB3V_VDIG_RESET_VALUE	LS_VUSB3V_VDIG_RESET_FORCE	LS_VUSB1V8_VDIG_RESET_VALUE	LS_VUSB1V8_VDIG_RESET_FORCE	LS_VUSB1V5_VDIG_RESET_VALUE	LS_VUSB1V5_VDIG_RESET_FORCE	LS_VUSB3V_VBUS_RESET_VALUE	LS_VUSB3V_ BUS_RESET_FORCE

Bits	Field Name	Description	Type	Reset
7	LS_VUSB3V_VDIG_RESET_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
6	LS_VUSB3V_VDIG_RESET_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0
5	LS_VUSB1V8_VDIG_RESET_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
4	LS_VUSB1V8_VDIG_RESET_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0
3	LS_VUSB1V5_VDIG_RESET_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
2	LS_VUSB1V5_VDIG_RESET_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0
1	LS_VUSB3V_VBUS_RESET_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
0	LS_VUSB3V_ BUS_RESET_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0

Table 5-160. Register Call Summary for Register LS_TST_C

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-161. LS_TST_D

Address Offset	0x11-0x11 in 0x17 byte increments		
Physical Address	0x0000 006C-0x0000 006C	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				LS_VOI_VDIG_RESET_VALUE	LS_VIO_VDIG_RESET_FORCE	LS_VDIG_VRRTC_RESET_VALUE	LS_VDIG_VRRTC_RESET_FORCE

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RW	0x0
3	LS_VOI_VDIG_RESET_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
2	LS_VIO_VDIG_RESET_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0
1	LS_VDIG_VRRTC_RESET_VALUE	0: LS enable/reset is set to 0 in force mode. 0: LS enable/reset is set to 1 in force mode.	RW	0
0	LS_VDIG_VRRTC_RESET_FORCE	0: No action (auto mode) 1: Force LS enable/reset with the xx_VALUE register.	RW	0

Table 5-162. Register Call Summary for Register LS_TST_D

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-163. BB_CFG

Address Offset	0x12-0x12 in 0x17 byte increments		
Physical Address	0x0000 006D-0x0000 006D	**Instance**	PM_RECEIVER
Description	Backup battery configuration register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			BBCHEN	BBSEL		BBISEL	

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4	BBCHEN	Backup battery charger enable Reset when signal triton_reset_na is low (WAIT-ON state).	RW	0
3:2	BBSEL	Backup battery charging voltage 00: 2.5 V 01: 3.0 V 10: 3.1 V 11: 3.2 V	RW	0x0
1: 0	BBISEL	Backup battery charging current 00: 25 μA 01: 150 μA 10: 500 μA 11: 1 mA	RW	0x0

Table 5-164. Register Call Summary for Register BB_CFG

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-165. TRIM1

Address Offset	0x14-0x14 in 0x17 byte increments		
Physical Address	0x0000 006F-0x0000 006F	**Instance**	PM_RECEIVER
Description	TRIM 1 configuration register (VRRTC domain) Protected with the KEY_TST		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		TRIM_VUSB3V		TRIM_VUSB1V8		TRIM_VUSB1V5	

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5:4	TRIM_VUSB3V	These bits select the USB3V1 LDO output voltage. 00: 3.12 V 01: 3.21 V 10: 3.31 V 11: 3.41 V These bits are protected with the KEY_TST. If they are used in functional mode, the user must lock back the KEY_TST immediately after register write.	RW	0x0
3:2	TRIM_VUSB1V8	2 trim bits. Protected with the KEY_TST. 00: 1.84 V 01: 1.84 V 10: 1.92 V 11: 2.02 V	RW	0x0
1: 0	TRIM_VUSB1V5	2 trim bits. Protected with the KEY_TST. 00: 1.52 V 01: 1.52 V 10: 1.65 V	RW	0x0

Bits	Field Name	Description	Type	Reset
		11: 1.78 V		

Table 5-166. Register Call Summary for Register TRIM1

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-167. TRIM2

Address Offset	0x15-0x15 in 0x17 byte increments		
Physical Address	0x0000 0070-0x0000 0070	**Instance**	PM_RECEIVER
Description	TRIM 2 configuration register (VRRTC domain)		
	Protected with the KEY_TST		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	ITRIM			Reserved			

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6:4	ITRIM	Bias current generator trim	RW	0x0
3:0	Reserved		R	0x0

Table 5-168. Register Call Summary for Register TRIM2

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-169. DCDC_TIMEOUT

Address Offset	0x16-0x16 in 0x17 byte increments		
Physical Address	0x0000 0071-0x0000 0071	**Instance**	PM_RECEIVER
Description	DC/DC time-out register (VRRTC domain)		
	Not implemented for PG 1.0		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED		RESERVED					

Bits	Field Name	Description	Type	Reset
7:6	RESERVED		R	0x0
5:0	RESERVED		R	0

Table 5-170. VAUX1_DEV_GRP

Address Offset	0x17-0x17 in 0x10 byte increments		
Physical Address	0x0000 0072-0x0000 0072	**Instance**	PM_RECEIVER
Description	Voltage regulator: VAUX1 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x0
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-171. Register Call Summary for Register VAUX1_DEV_GRP

Resets and Power-Management Environment
- nSLEEP1: [0]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-172. VAUX1_TYPE

Address Offset	0x18-0x18 in 0x10 byte increments		
Physical Address	0x0000 0073-0x0000 0073	**Instance**	PM_RECEIVER
Description	VAUX1 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-173. Register Call Summary for Register VAUX1_TYPE

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-174. VAUX1_REMAP

Address Offset	0x19-0x19 in 0x10 byte increments		
Physical Address	0x0000 0074-0x0000 0074	**Instance**	PM_RECEIVER
Description	When the VAUX1 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-175. Register Call Summary for Register VAUX1_REMAP

Reset and Power Management Functional Description

- PMB Message to Resource State Registers: [0] [1]

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [2] [3] [4] [5] [6] [7]

Table 5-176. VAUX1_DEDICATED

Address Offset	0x1A-0x1A in 0x10 byte increments		
Physical Address	0x0000 0075-0x0000 0075	**Instance**	PM_RECEIVER
Description	Voltage regulator: VAUX1 basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved	VSEL		

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode 1: Regulator output is high-impedance. Protected with the KEY_TST.	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3	Reserved		R	0
2:0	VSEL	Select LDO output voltage. VSEL 000 1.5 typical	RW	0x2 (1)

(1) This reset value is for boot mode SC021. For the reset values of the other boot modes, see Table 6-1, *Summary of the Power Provider*, in Chapter 6.1, *Power Provider*, in the device data manual.

Bits	Field Name	Description	Type	Reset
		001 1.8 typical		
		010 2.5		
		011 2.8		
		100 3.0		
		101 3.0		
		110 3.0		
		111 3.0		

Table 5-177. Register Call Summary for Register VAUX1_DEDICATED

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-178. VAUX2_DEV_GRP

Address Offset	0x1B-0x1B in 0x10 byte increments		
Physical Address	0x0000 0076-0x0000 0076	**Instance**	PM_RECEIVER
Description	Voltage regulator: VAUX2 device group register (VRRTC domain)		
Type	See Table 5-124, *PM_RECEIVER Mode Overview.*		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group	RW	0x4
		000: Belongs to no device group		
		001: Belongs to P1 device group		
		010: Belongs to P2 device group		
		011: Belongs to P1 and P2 device group		
		100: Belongs to P3 device group		
		101: Belongs to P1 and P3 device group		
		110: Belongs to P2 and P3 device group		
		111: Belongs to all device group		
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value.	RW	0
		0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.		
3:0	STATE	Current state of the resource	R	0x0

Table 5-179. Register Call Summary for Register VAUX2_DEV_GRP

Reset and Power-Management Programming Model
- Sequencing: [0]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [1] [2] [3] [4] [5]

Table 5-180. VAUX2_TYPE

Address Offset	0x1C-0x1C in 0x10 byte increments		
Physical Address	0x0000 0077-0x0000 0077	**Instance**	PM_RECEIVER
Description	VAUX2 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x3

Table 5-181. Register Call Summary for Register VAUX2_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-182. VAUX2_REMAP

Address Offset	0x1D-0x1D in 0x10 byte increments		
Physical Address	0x0000 0078-0x0000 0078	**Instance**	PM_RECEIVER
Description	When the VAUX2 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-183. Register Call Summary for Register VAUX2_REMAP

Reset and Power-Management Programming Model
- Sequencing: [0]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-184. VAUX2_DEDICATED

Address Offset	0x1E-0x1E in 0x10 byte increments		
Physical Address	0x0000 0079-0x0000 0079	**Instance**	PM_RECEIVER
Description	Voltage regulator: VAUX2 basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		VSEL			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode	RW	0
		1: Regulator output is high-impedance. Protected with the KEY_TST.		
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3:0	VSEL	Select LDO output voltage.	RW	0x9 (1)
		VSE		
		0000 1.70 1.00 typical		
		0001 1.70 1.00 typical		
		0010 1.90 1.20 typical		
		0011 1.30		
		0100 1.50		
		0101 1.80		
		0110 2.00 1.85 typical		
		0111 2.50		
		1000 2.10 2.60 typical		
		1001 2.80		
		1010 2.20 2.85 typical		
		1011 2.30 3.00 typical		
		1100 2.40 3.15 typical		
		1101 2.40 3.15 typical		
		1110 2.40 3.15 typical		
		1111 2.40 3.15 typical		

(1) This reset value is for boot mode SC021. For the reset values of the other boot modes, see Table 6-1, *Summary of the Power Provider*, in Chapter 6.1, *Power Provider*, in the device data manual.

Table 5-185. Register Call Summary for Register VAUX2_DEDICATED

Reset and Power-Management Programming Model
- Sequencing: [0]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-186. VAUX3_DEV_GRP

Address Offset	0x1F-0x1F in 0x10 byte increments		
Physical Address	0x0000 007A-0x0000 007A	**Instance**	PM_RECEIVER
Description	Voltage regulator: VAUX3 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x0
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-187. Register Call Summary for Register VAUX3_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-188. VAUX3_TYPE

Address Offset	0x20-0x20 in 0x10 byte increments		
Physical Address	0x0000 007B-0x0000 007B	**Instance**	PM_RECEIVER
Description	VAUX3 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-189. Register Call Summary for Register VAUX3_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-190. VAUX3_REMAP

Address Offset	0x21-0x21 in 0x10 byte increments		
Physical Address	0x0000 007C-0x0000 007C	**Instance**	PM_RECEIVER
Description	When the VAUX3 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-191. Register Call Summary for Register VAUX3_REMAP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-192. VAUX3_DEDICATED

Address Offset	0x22-0x22 in 0x10 byte increments		
Physical Address	0x0000 007D-0x0000 007D	**Instance**	PM_RECEIVER
Description	Voltage regulator: VAUX3 basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved	VSEL		

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode	RW	0
		1: Regulator output is high-impedance. Protected with the KEY_TST.		
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3	Reserved		R	0
2:0	VSEL	Select LDO output voltage.	RW	0x3 (1)
		000 1.5		
		001 1.8		
		010 2.5		
		011 2.8		
		100 3.0 typical		
		101 3.0 typical		
		110 3.0 typical		
		111 3.0 typical		

(1) This reset value is for boot mode SC021. For the reset values of the other boot modes, see Table 6-1, *Summary of the Power Provider*, in Chapter 6.1, *Power Provider*, in the device data manual.

Table 5-193. Register Call Summary for Register VAUX3_DEDICATED

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-194. VAUX4_DEV_GRP

Address Offset	0x23-0x23 in 0x10 byte increments		
Physical Address	0x0000 007E-0x0000 007E	**Instance**	PM_RECEIVER
Description	Voltage regulator: VAUX4 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x4
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-195. Register Call Summary for Register VAUX4_DEV_GRP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-196. VAUX4_TYPE

Address Offset	0x24-0x24 in 0x10 byte increments		
Physical Address	0x0000 007F-0x0000 007F	**Instance**	PM_RECEIVER
Description	VAUX4 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x3

Table 5-197. Register Call Summary for Register VAUX4_TYPE

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-198. VAUX4_REMAP

Address Offset	0x25-0x25 in 0x10 byte increments		
Physical Address	0x0000 0080-0x0000 0080	**Instance**	PM_RECEIVER
Description	When the VAUX4 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-199. Register Call Summary for Register VAUX4_REMAP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1]

Table 5-200. VAUX4_DEDICATED

Address Offset	0x26-0x26 in 0x10 byte increments		
Physical Address	0x0000 0081-0x0000 0081	**Instance**	PM_RECEIVER
Description	Voltage regulator: VAUX4 basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		VSEL			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode 1: Regulator output is high-impedance. Protected with the KEY_TST.	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3:0	VSEL	Select LDO output voltage. 0000 0.70	RW	0x2 (1)

(1) This reset value is for boot mode SC021. For the reset values of the other boot modes, see Table 6-1, *Summary of the Power Provider*, in Chapter 6.1, *Power Provider*, in the device data manual.

Bits	Field Name	Description	Type	Reset
		0001 1.00		
		0010 1.20		
		0011 1.30 typical		
		0100 1.50		
		0101 1.80		
		0110 1.85 typical		
		0111 2.50		
		1000 2.60 typical		
		1001 2.80		
		1010 2.85 typical		
		1011 3.00 typical		
		1100 3.15 typical		
		1101 3.15 typical		
		1110 3.15 typical		
		1111 3.15 typical		

Table 5-201. Register Call Summary for Register VAUX4_DEDICATED

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-202. VMMC1_DEV_GRP

Address Offset	0x27-0x27 in 0x8 byte increments		
Physical Address	0x0000 0082-0x0000 0082	**Instance**	PM_RECEIVER
Description	Voltage regulator: VMMC1 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group	RW	0x0
		000: Belongs to no device group		
		001: Belongs to P1 device group		
		010: Belongs to P2 device group		
		011: Belongs to P1 and P2 device groups		
		100: Belongs to P3 device group		
		101: Belongs to P1 and P3 device groups		
		110: Belongs to P2 and P3 device groups		
		111: Belongs to all device groups		
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value.	RW	0
		0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.		
3:0	STATE	Current state of the resource	R	0x0

Table 5-203. Register Call Summary for Register VMMC1_DEV_GRP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-204. VMMC1_TYPE

Address Offset	0x28-0x28 in 0x8 byte increments		
Physical Address	0x0000 0083-0x0000 0083	**Instance**	PM_RECEIVER
Description	VMMC1 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-205. Register Call Summary for Register VMMC1_TYPE

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-206. VMMC1_REMAP

Address Offset	0x29-0x29 in 0x8 byte increments		
Physical Address	0x0000 0084-0x0000 0084	**Instance**	PM_RECEIVER
Description	When the VMMC1 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-207. Register Call Summary for Register VMMC1_REMAP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-208. VMMC1_DEDICATED

Address Offset	0x2A-0x2A in 0x8 byte increments		
Physical Address	0x0000 0085-0x0000 0085	**Instance**	PM_RECEIVER
Description	Voltage regulator: VMMC1 basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved		VSEL	

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode 1: Regulator output is high-impedance. Protected with the KEY_TST.	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3:2	Reserved		R	0x0
1: 0	VSEL	Select LDO output voltage. 00 1.85 01 2.85 10 3.00 11 3.15	RW	0x0 (1)

(1) This reset value is for boot mode SC021. For the reset values of the other boot modes, see Table 6-1, *Summary of the Power Provider*, in Chapter 6.1, *Power Provider*, in the device data manual.

Table 5-209. Register Call Summary for Register VMMC1_DEDICATED

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-210. VMMC2_DEV_GRP

Address Offset	0x2B-0x2B in 0x8 byte increments		
Physical Address	0x0000 0086-0x0000 0086	**Instance**	PM_RECEIVER
Description	Voltage regulator: VMMC2 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x4

Bits	Field Name	Description	Type	Reset
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-211. Register Call Summary for Register VMMC2_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-212. VMMC2_TYPE

Address Offset	0x2C-0x2C in 0x8 byte increments		
Physical Address	0x0000 0087-0x0000 0087	**Instance**	PM_RECEIVER
Description	VMMc2 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x3

Table 5-213. Register Call Summary for Register VMMC2_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-214. VMMC2_REMAP

Address Offset	0x2D-0x2D in 0x8 byte increments		
Physical Address	0x0000 0088-0x0000 0088	**Instance**	PM_RECEIVER
Description	When the VMMC2 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-215. Register Call Summary for Register VMMC2_REMAP

Reset and Power-Management Programming Model • Sequencing: [0]
Reset and Power-Management Registers • PM_RECEIVER Module Instance: [1] [2]

Table 5-216. VMMC2_DEDICATED

Address Offset	0x2E-0x2E in 0x8 byte increments		
Physical Address	0x0000 0089-0x0000 0089	**Instance**	PM_RECEIVER
Description	Voltage regulator: VMMC2 basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		VSEL			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode 1: Regulator output is high-impedance. Protected with the KEY_TST.	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3:0	VSEL	Select LDO output voltage. 0000 1.00 typical 0001 1.00 typical 0010 1.20 typical 0011 1.30 typical 0100 1.50 typical 0101 1.80 typical 0110 1.85 0111 2.50 typical 1000 2.60 1001 2.80 1010 2.85 1011 3.00 1100 3.15 1101 3.15 1110 3.15 1111 3.15	RW	0x8[1]

(1) This reset value is for boot mode SC021. For the reset values of the other boot modes, see Table 6-1, *Summary of the Power Provider*, in Chapter 6.1, *Power Provider*, in the device data manual.

Table 5-217. Register Call Summary for Register VMMC2_DEDICATED

Reset and Power-Management Registers • PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-218. VPLL1_DEV_GRP

Address Offset	0x2F-0x2F in 0x8 byte increments		
Physical Address	0x0000 008A-0x0000 008A	**Instance**	PM_RECEIVER
Description	Voltage regulator: VPLL1 device groups register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x1
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-219. Register Call Summary for Register VPLL1_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-220. VPLL1_TYPE

Address Offset	0x30-0x30 in 0x8 byte increments		
Physical Address	0x0000 008B-0x0000 008B	**Instance**	PM_RECEIVER
Description	VPLL1 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-221. Register Call Summary for Register VPLL1_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-222. VPLL1_REMAP

Address Offset	0x31-0x31 in 0x8 byte increments		
Physical Address	0x0000 008C-0x0000 008C	**Instance**	PM_RECEIVER
Description	When the VPLL1 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x0

Table 5-223. Register Call Summary for Register VPLL1_REMAP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-224. VPLL1_DEDICATED

Address Offset	0x32-0x32 in 0x8 byte increments		
Physical Address	0x0000 008D-0x0000 008D	**Instance**	PM_RECEIVER
Description	Voltage regulator: VPLL1 basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved	VSEL		

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode 1: Regulator output is high-impedance. Protected with the KEY_TST.	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3	Reserved		R	0
2:0	VSEL	Select LDO output voltage. 000 1.0 001 1.2 010 1.3 011 1.8 100 2.8 typical 101 3.0 typical 110 3.0 typical 111 3.0 typical	RW	0x2 (1)

(1) This reset value is for boot mode SC021. For the reset values of the other boot modes, see Table 6-1, *Summary of the Power Provider*, in Chapter 6.1, *Power Provider*, in the device data manual.

Table 5-225. Register Call Summary for Register VPLL1_DEDICATED

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-226. VPLL2_DEV_GRP

Address Offset	0x33-0x33 in 0x8 byte increments		
Physical Address	0x0000 008E-0x0000 008E	**Instance**	PM_RECEIVER
Description	Voltage regulator: VPLL2 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x4
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-227. Register Call Summary for Register VPLL2_DEV_GRP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-228. VPLL2_TYPE

Address Offset	0x34-0x34 in 0x8 byte increments		
Physical Address	0x0000 008F-0x0000 008F	**Instance**	PM_RECEIVER
Description	VPLL2 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x4

Table 5-229. Register Call Summary for Register VPLL2_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-230. VPLL2_REMAP

Address Offset	0x35-0x35 in 0x8 byte increments		
Physical Address	0x0000 0090-0x0000 0090	**Instance**	PM_RECEIVER
Description	When the VPLL2 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-231. Register Call Summary for Register VPLL2_REMAP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-232. VPLL2_DEDICATED

Address Offset	0x36-0x36 in 0x8 byte increments		
Physical Address	0x0000 0091-0x0000 0091	**Instance**	PM_RECEIVER
Description	Voltage regulator: VPLL2 basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		VSEL			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode 1: Regulator output is high-impedance. Protected with the KEY_TST.	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3:0	VSEL	Select LDO output voltage. 0000 0.70	RW	0x2 (1)

(1) This reset value is for boot mode SC021. For the reset values of the other boot modes, see Table 6-1, *Summary of the Power Provider*, in Chapter 6.1, *Power Provider*, in the device data manual.

Bits	Field Name	Description	Type	Reset
		0001 1.00		
		0010 1.20		
		0011 1.30		
		0100 1.50 typical		
		0101 1.80		
		0110 1.85 typical		
		0111 2.50 typical		
		1000 2.60 typical		
		1001 2.80 typical		
		1010 2.85 typical		
		1011 3.00 typical		
		1100 3.15 typical		
		1101 3.15 typical		
		1110 3.15 typical		
		1111 3.15 typical		

Table 5-233. Register Call Summary for Register VPLL2_DEDICATED

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-234. VSIM_DEV_GRP

Address Offset	0x37-0x37 in 0x4 byte increments		
Physical Address	0x0000 0092-0x0000 0092	**Instance**	PM_RECEIVER
Description	Voltage regulator: VSIM device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x0
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-235. Register Call Summary for Register VSIM_DEV_GRP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-236. VSIM_TYPE

Address Offset	0x38-0x38 in 0x4 byte increments		
Physical Address	0x0000 0093-0x0000 0093	**Instance**	PM_RECEIVER
Description	VSIM resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-237. Register Call Summary for Register VSIM_TYPE

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-238. VSIM_REMAP

Address Offset	0x39-0x39 in 0x4 byte increments		
Physical Address	0x0000 0094-0x0000 0094	**Instance**	PM_RECEIVER
Description	When the VSIM device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x0

Table 5-239. Register Call Summary for Register VSIM_REMAP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-240. VSIM_DEDICATED

Address Offset	0x3A-0x3A in 0x4 byte increments		
Physical Address	0x0000 0095-0x0000 0095	**Instance**	PM_RECEIVER
Description	Voltage regulator: VSIM basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved	VSEL		

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode	RW	0
		1: Regulator output is high-impedance. Protected with the KEY_TST.		
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3	Reserved		R	0
2:0	VSEL	Select LDO output voltage.	RW	0x3 (1)
		000 1.0 typical		
		001 1.2 typical		
		010 1.3 typical		
		011 1.8		
		100 2.8		
		101 3.0		
		110 3.0		
		111 3.0		

(1) This reset value is for boot mode SC021. For the reset values of the other boot modes, see Table 6-1, *Summary of the Power Provider*, in Chapter 6.1, *Power Provider*, in the device data manual.

Table 5-241. Register Call Summary for Register VSIM_DEDICATED

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-242. VDAC_DEV_GRP

Address Offset	0x3B-0x3B in 0x4 byte increments		
Physical Address	0x0000 0096-0x0000 0096	**Instance**	PM_RECEIVER
Description	Voltage regulator: VDAC device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group	RW	0x0
		000: Belongs to no device group		
		001: Belongs to P1 device group		
		010: Belongs to P2 device group		
		011: Belongs to P1 and P2 device groups		
		100: Belongs to P3 device group		

Bits	Field Name	Description	Type	Reset
		101: Belongs to P1 and P3 device groups		
		110: Belongs to P2 and P3 device groups		
		111: Belongs to all device groups		
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value.	RW	0
		0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.		
3:0	STATE	Current state of the resource	R	0x0

Table 5-243. Register Call Summary for Register VDAC_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-244. VDAC_TYPE

Address Offset	0x3C-0x3C in 0x4 byte increments		
Physical Address	0x0000 0097-0x0000 0097	**Instance**	PM_RECEIVER
Description	VDAC resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-245. Register Call Summary for Register VDAC_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-246. VDAC_REMAP

Address Offset	0x3D-0x3D in 0x4 byte increments		
Physical Address	0x0000 0098-0x0000 0098	**Instance**	PM_RECEIVER
Description	When the VDAC device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-247. Register Call Summary for Register VDAC_REMAP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-248. VDAC_DEDICATED

Address Offset	0x3E-0x3E in 0x4 byte increments		
Physical Address	0x0000 0099-0x0000 0099	**Instance**	PM_RECEIVER
Description	Voltage regulator: VDAC basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved		VSEL	

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode 1: Regulator output is high-impedance. Protected with the KEY_TST.	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3:2	Reserved		R	0x0
1: 0	VSEL	Select LDO output voltage. 00 1.2 01 1.3 10 1.8 11 1.8	RW	0x2 (1)

(1) This reset value is for boot mode SC021. For the reset values of the other boot modes, see Table 6-1, *Summary of the Power Provider*, in Chapter 6.1, *Power Provider*, in the device data manual.

Table 5-249. Register Call Summary for Register VDAC_DEDICATED

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-250. VINTANA1_DEV_GRP

Address Offset	0x3F-0x3F in 0xC byte increments		
Physical Address	0x0000 009A-0x0000 009A	**Instance**	PM_RECEIVER
Description	Voltage regulator: VINTANA1 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-251. Register Call Summary for Register VINTANA1_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-252. VINTANA1_TYPE

Address Offset	0x40-0x40 in 0xC byte increments		
Physical Address	0x0000 009B-0x0000 009B	**Instance**	PM_RECEIVER
Description	VINTANA1 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x1

Table 5-253. Register Call Summary for Register VINTANA1_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4]

Table 5-254. VINTANA1_REMAP

Address Offset	0x41-0x41 in 0xC byte increments		
Physical Address	0x0000 009C-0x0000 009C	**Instance**	PM_RECEIVER
Description	When the VINTANA1 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-255. Register Call Summary for Register VINTANA1_REMAP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-256. VINTANA1_DEDICATED

Address Offset	0x42-0x42 in 0xC byte increments		
Physical Address	0x0000 009D-0x0000 009D	**Instance**	PM_RECEIVER
Description	Voltage regulator: VINTANA1 basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode 1: Regulator output is high-impedance. Protected with the KEY_TST.	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3:0	Reserved		R	0x0

Table 5-257. Register Call Summary for Register VINTANA1_DEDICATED

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-258. VINTANA2_DEV_GRP

Address Offset	0x43-0x43 in 0xC byte increments		
Physical Address	0x0000 009E-0x0000 009E	**Instance**	PM_RECEIVER
Description	Voltage regulator: VINTANA2 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-259. Register Call Summary for Register VINTANA2_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-260. VINTANA2_TYPE

Address Offset	0x44-0x44 in 0xC byte increments		
Physical Address	0x0000 009F-0x0000 009F	**Instance**	PM_RECEIVER
Description	VINTANA2 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-261. Register Call Summary for Register VINTANA2_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-262. VINTANA2_REMAP

Address Offset	0x45-0x45 in 0xC byte increments		
Physical Address	0x0000 00A0-0x0000 00A0	**Instance**	PM_RECEIVER
Description	When the VINTANA2 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-263. Register Call Summary for Register VINTANA2_REMAP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-264. VINTANA2_DEDICATED

Address Offset	0x46-0x46 in 0xC byte increments		
Physical Address	0x0000 00A1-0x0000 00A1	**Instance**	PM_RECEIVER
Description	Voltage regulator: VINTANA2 basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved			VSEL

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode 1: Regulator output is high-impedance. Protected with the KEY_TST.	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3:1	Reserved		R	0x0
0	VSEL	Select LDO output voltage. 0 2.50 1 2.75	RW	1[(1)]

(1) This reset value is for boot mode SC021. For the reset values of the other boot modes, see Table 6-1, *Summary of the Power Provider*, in Chapter 6.1, *Power Provider*, in the device data manual.

Table 5-265. Register Call Summary for Register VINTANA2_DEDICATED

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-266. VINTDIG_DEV_GRP

Address Offset	0x47-0x47 in 0xC byte increments		
Physical Address	0x0000 00A2-0x0000 00A2	**Instance**	PM_RECEIVER
Description	Voltage regulator: VINTDIG device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-267. Register Call Summary for Register VINTDIG_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-268. VINTDIG_TYPE

Address Offset	0x48-0x48 in 0xC byte increments		
Physical Address	0x0000 00A3-0x0000 00A3	**Instance**	PM_RECEIVER
Description	VINTDIG resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x1

Table 5-269. Register Call Summary for Register VINTDIG_TYPE

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-270. VINTDIG_REMAP

Address Offset	0x49-0x49 in 0xC byte increments		
Physical Address	0x0000 00A4-0x0000 00A4	**Instance**	PM_RECEIVER
Description	When the VINTDIG device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-271. Register Call Summary for Register VINTDIG_REMAP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-272. VINTDIG_DEDICATED

Address Offset	0x4A-0x4A in 0xC byte increments		
Physical Address	0x0000 00A5-0x0000 00A5	**Instance**	PM_RECEIVER
Description	Voltage regulator: VINTDIG basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		VSEL			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	TRIEN	0: Off mode 1: Regulator output is high-impedance. Protected with the KEY_TST.	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST.	RW	0x0
3:0	VSEL	Select LDO output voltage. 0000 0.70 Not allowed 0001 1.00 typical 0010 1.20 typical 0011 1.30 typical	RW	0x4 (1)

(1) This reset value is for boot mode SC021. For the reset values of the other boot modes, see Table 6-1, *Summary of the Power Provider*, in Chapter 6.1, *Power Provider*, in the device data manual.

Bits	Field Name	Description	Type	Reset
		0100 1.50		
		0101 1.80 typical		
		0110 1.85 typical		
		0111 2.50 typical		
		1000 2.60 typical		
		1001 2.80 typical		
		1010 2.85 typical		
		1011 3.00 typical		
		1100 3.15 typical		
		1101 3.15 typical		
		1110 3.15 typical		
		1111 3.15 typical		

Table 5-273. Register Call Summary for Register VINTDIG_DEDICATED

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-274. VIO_DEV_GRP

Address Offset	0x4B-0x4B in 0x26 byte increments		
Physical Address	0x0000 00A6-0x0000 00A6	**Instance**	PM_RECEIVER
Description	VIO device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group	RW	0x7
		000: Belongs to no device group		
		001: Belongs to P1 device group		
		010: Belongs to P2 device group		
		011: Belongs to P1 and P2 device groups		
		100: Belongs to P3 device group		
		101: Belongs to P1 and P3 device groups		
		110: Belongs to P2 and P3 device groups		
		111: Belongs to all device groups		
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value.	RW	0
		0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.		
3:0	STATE	Current state of the resource	R	0x0

Table 5-275. Register Call Summary for Register VIO_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-276. VIO_TYPE

Address Offset	0x4C-0x4C in 0x26 byte increments		
Physical Address	0x0000 00A7-0x0000 00A7	**Instance**	PM_RECEIVER
Description	Resource type set (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x3

Table 5-277. Register Call Summary for Register VIO_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-278. VIO_REMAP

Address Offset	0x4D-0x4D in 0x26 byte increments		
Physical Address	0x0000 00A8-0x0000 00A8	**Instance**	PM_RECEIVER
Description	When the VIO device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-279. Register Call Summary for Register VIO_REMAP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-280. VIO_CFG

Address Offset	0x4E-0x4E in 0x26 byte increments		
Physical Address	0x0000 00A9-0x0000 00A9	**Instance**	PM_RECEIVER
Description	VIO configuration register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						EN_NDRV_LOWV	BUCK_HIZ_LOWV

Bits	Field Name	Description	Type	Reset
7:2	Reserved		R	0x00
1	EN_NDRV_LOWV	Forces PWM operation by requiring synchronous NMOS on every cycle	RW	0
0	BUCK_HIZ_LOWV	Hi-Z disable mode enable. VDIG level.	RW	0

Table 5-281. Register Call Summary for Register VIO_CFG

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-282. VIO_MISC_CFG

Address Offset	0x4F-0x4F in 0x26 byte increments		
Physical Address	0x0000 00AA-0x0000 00AA	**Instance**	PM_RECEIVER
Description	VIO configuration register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			BUCK_AMUX		DRIVE_SEL		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	BUCK_AMUX		RW	0x0
2:0	DRIVE_SEL	Drive strength adjustment - test function	RW	0x0

Table 5-283. Register Call Summary for Register VIO_MISC_CFG

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-284. VIO_TEST1

Address Offset	0x50-0x50 in 0x26 byte increments		
Physical Address	0x0000 00AB-0x0000 00AB	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
TEST_ENB_ CLMP700_LOWV	TEST_EN_2X_ START_LOWV	TEST_ENB_ ANTIGLITCH_ LOWV	TEST_ENB_ ERRAMP_LOWV	TEST_ENB_ ILIMIT_LOWV	TEST_EN_ MEAS_NRDS_ LOWV	TEST_EN_ MEAS_PRES_ LOWV	TEST_ENB_SFTST RT_LOWV

Bits	Field Name	Description	Type	Reset
7	TEST_ENB_ CLMP700_LOWV		RW	0
6	TEST_EN_2X_ START_LOWV		RW	0
5	TEST_ENB_ ANTIGLITCH_ LOWV		RW	0
4	TEST_ENB_ ERRAMP_LOWV		RW	0
3	TEST_ENB_ ILIMIT_LOWV		RW	0
2	TEST_EN_ MEAS_NRDS_ LOWV		RW	0
1	TEST_EN_ MEAS_PRES_ LOWV		RW	0
0	TEST_ENB_SFTST RT_LOWV		RW	0

Table 5-285. Register Call Summary for Register VIO_TEST1

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-286. VIO_TEST2

Address Offset	0x51-0x51 in 0x26 byte increments		
Physical Address	0x0000 00AC-0x0000 00AC	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TEST_DC/DC				TEST_ENB_SYNC_COMP_LOWV	TEST_ENB_SYNC_LOWV	TEST_EN_SLEWCTRL_LOWV

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:3	TEST_DC/DC		RW	0x0
2	TEST_ENB_SYNC_COMP_LOWV		RW	0
1	TEST_ENB_SYNC_LOWV		RW	0
0	TEST_EN_SLEWCTRL_LOWV		RW	0

Table 5-287. Register Call Summary for Register VIO_TEST2

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-288. VIO_OSC

Address Offset	0x52-0x52 in 0x26 byte increments		
Physical Address	0x0000 00AD-0x0000 00AD	**Instance**	PM_RECEIVER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			OVLAP_SEL			SH_RAMP_ SWITCH	

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0
4:2	OVLAP_SEL	BUCK overlap time adjustment - test function	RW	0x0
1: 0	SH_RAMP_ SWITCH		RW	0x0

Table 5-289. Register Call Summary for Register VIO_OSC

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-290. VIO_RESERVED

Address Offset	0x53-0x53 in 0x26 byte increments		
Physical Address	0x0000 00AE-0x0000 00AE	**Instance**	PM_RECEIVER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-291. Register Call Summary for Register VIO_RESERVED

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-292. VIO_VSEL

Address Offset	0x54-0x54 in 0x26 byte increments		
Physical Address	0x0000 00AF-0x0000 00AF	**Instance**	PM_RECEIVER
Description	Controls the output voltage (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							VSEL

Bits	Field Name	Description	Type	Reset
7:1	Reserved		R	0x00
0	VSEL	0 = 1p8V 1 = 1p85V	RW	0[(1)]

(1) This reset value is the same for all boot modes.

Table 5-293. Register Call Summary for Register VIO_VSEL

Reset and Power-Management Programming Model
- Sequencing: [0]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-294. VDD1_DEV_GRP

Address Offset	0x55-0x55 in 0x26 byte increments		
Physical Address	0x0000 00B0-0x0000 00B0	**Instance**	PM_RECEIVER
Description	VDD1 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x1
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-295. Register Call Summary for Register VDD1_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-296. VDD1_TYPE

Address Offset	0x56-0x56 in 0x26 byte increments		
Physical Address	0x0000 00B1-0x0000 00B1	**Instance**	PM_RECEIVER
Description	Resource type set (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x4

Table 5-297. Register Call Summary for Register VDD1_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-298. VDD1_REMAP

Address Offset	0x57-0x57 in 0x26 byte increments		
Physical Address	0x0000 00B2-0x0000 00B2	**Instance**	PM_RECEIVER
Description	When the VDD1 device is in sleep or off mode, it allows setting the resource to active or off/sleep (VRRTC domain) by the nSLEEP1 pin. Not effective if VDD1 is put in sleep mode using SmartReflex I^2C bus (the VDD1_SR_CONTROL register). OFF_STATE and SLEEP_STATE details are given in Table 5-5, or the following values can be used: OFF = 0x0, SLEEP = 0x8, ACTIVE = 0xE.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-299. Register Call Summary for Register VDD1_REMAP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-300. VDD1_CFG

Address Offset	0x58-0x58 in 0x26 byte increments		
Physical Address	0x0000 00B3-0x0000 00B3	**Instance**	PM_RECEIVER
Description	VDD1 configuration register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						EN_NDRV_LOWV	BUCK_HIZ_LOWV

Bits	Field Name	Description	Type	Reset
7:2	Reserved		R	0x00
1	EN_NDRV_LOWV	Forces PWM operation by requiring synchronous NMOS on every cycle	RW	0
0	BUCK_HIZ_LOWV	Hi-Z disable mode enable. VDIG level.	RW	0

Table 5-301. Register Call Summary for Register VDD1_CFG

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-302. VDD1_MISC_CFG

Address Offset	0x59-0x59 in 0x26 byte increments		
Physical Address	0x0000 00B4-0x0000 00B4	**Instance**	PM_RECEIVER
Description	VDD1 configuration register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			BUCK_AMUX		DRIVE_SEL		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x00
4:3	BUCK_AMUX		RW	0x00
2:0	DRIVE_SEL	Drive strength adjustment - test function	RW	0x00

Table 5-303. Register Call Summary for Register VDD1_MISC_CFG

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-304. VDD1_TEST1

Address Offset	0x5A-0x5A in 0x26 byte increments		
Physical Address	0x0000 00B5-0x0000 00B5	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
TEST_ENB_ CLMP700_LOWV	TEST_EN_2X_ START_LOWV	TEST_ENB_ ANTIGLITCH_ LOWV	TEST_ENB_ ERRAMP_LOWV	TEST_ENB_ ILIMIT_LOWV	TEST_EN_ MEAS_NRDS_ LOWV	TEST_EN_ MEAS_PRES_ LOWV	TEST_ENB_ SFTSTRT_LOWV

Bits	Field Name	Description	Type	Reset
7	TEST_ENB_ CLMP700_LOWV		RW	0
6	TEST_EN_2X_ START_LOWV		RW	0
5	TEST_ENB_ ANTIGLITCH_ LOWV		RW	0
4	TEST_ENB_ ERRAMP_LOWV		RW	0
3	TEST_ENB_ ILIMIT_LOWV		RW	0
2	TEST_EN_ MEAS_NRDS_ LOWV		RW	0
1	TEST_EN_ MEAS_PRES_ LOWV		RW	0

Bits	Field Name	Description	Type	Reset
0	TEST_ENB_ SFTSTRT_LOWV		RW	0

Table 5-305. Register Call Summary for Register VDD1_TEST1

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-306. VDD1_TEST2

Address Offset	0x5B-0x5B in 0x26 byte increments		
Physical Address	0x0000 00B6-0x0000 00B6	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TEST_DC/DC				TEST_ENB_SYNC_ COMP_LOWV	TEST_ENB_SYNC_ LOWV	TEST_EN_ SLEWCTRL_LOWV

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:3	TEST_DC/DC		RW	0x0
2	TEST_ENB_SYNC_ COMP_LOWV		RW	0
1	TEST_ENB_SYNC_ LOWV		RW	0
0	TEST_EN_ SLEWCTRL_LOWV		RW	0

Table 5-307. Register Call Summary for Register VDD1_TEST2

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-308. VDD1_OSC

Address Offset	0x5C-0x5C in 0x26 byte increments		
Physical Address	0x0000 00B7-0x0000 00B7	**Instance**	PM_RECEIVER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			OVLAP_SEL			SH_RAMP_ SWITCH	

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
4:2	OVLAP_SEL	BUCK overlap time adjustment - test function	RW	0x0
1: 0	SH_RAMP_ SWITCH		RW	0x0

Table 5-309. Register Call Summary for Register VDD1_OSC

Reset and Power-Management Registers • PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-310. VDD1_RESERVED

Address Offset	0x5D-0x5D in 0x26 byte increments		
Physical Address	0x0000 00B8-0x0000 00B8	**Instance**	PM_RECEIVER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-311. Register Call Summary for Register VDD1_RESERVED

Reset and Power-Management Registers • PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-312. VDD1_VSEL

Address Offset	0x5E-0x5E in 0x26 byte increments		
Physical Address	0x0000 00B9-0x0000 00B9	**Instance**	PM_RECEIVER
Description	Controls the output voltage (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	VSEL						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	VSEL	WRITE: Controsl output voltage when VMODE_EN = 0 and SmartReflex not enabled READ: If READ_REG = 0: Controls output voltage If READ_REG = 1: Value of the register	RW	0x38

Table 5-313. Register Call Summary for Register VDD1_VSEL

Reset and Power Management Functional Description • Voltage Scaling Using VMODE1/2 in C027 Mode: [0]
Reset and Power-Management Registers • PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-314. VDD1_VMODE_CFG

Address Offset	0x5F-0x5F in 0x26 byte increments		
Physical Address	0x0000 00BA-0x0000 00BA	**Instance**	PM_RECEIVER
Description	vmode configuration register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		STS_BUSY	STS_ROOF	STS_FLOOR	DCDC_SLP	READ_REG	ENABLE_VMODE

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5	STS_BUSY	0: DC/DC is not computing a VMODE transition. 1: DC/DC is computing a VMODE transition.	R	0
4	STS_ROOF	0: DC/DC did not reach VROOF voltage output. 1: DC/DC reached VROOF voltage output.	R	0
3	STS_FLOOR	0: DC/DC did not reach VFLOOR voltage output. 1: DC/DC reached VFLOOR voltage output.	R	0
2	DCDC_SLP	0: Output voltage in sleep mode is the same as in active mode. 1: Output voltage in sleep mode is VFLOOR. **Note:** Do not set this bit to 1 when the ENABLE_VMODE bit is set to 1.	RW	0
1	READ_REG	Enable VSEL register value read. This bit is reset to 0 when DC/DC is swoff or when a warm reset occurs.	RW	0
0	ENABLE_VMODE	0: DC/DC voltage controlled by software (through DC/DC_VSEL) 1: DC/DC voltage controlled by VMODE pin **Note:** Do not set this bit to 1 when the DCDC_SLP bit is set to 1.	RW	0

Table 5-315. Register Call Summary for Register VDD1_VMODE_CFG

Reset and Power-Management Integration
- Resets: [0] [1] [2]

Reset and Power-Management Programming Model
- Sequencing: [3]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [4] [5] [6] [7] [8] [9]

Table 5-316. VDD1_VFLOOR

Address Offset	0x60-0x60 in 0x26 byte increments		
Physical Address	0x0000 00BB-0x0000 00BB	**Instance**	PM_RECEIVER
Description	Sets the voltage floor of DC/DC regulator (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	VFLOOR						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	VFLOOR		RW	0x00

Table 5-317. Register Call Summary for Register VDD1_VFLOOR

Reset and Power-Management Programming Model
- Sequencing: [0]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-318. VDD1_VROOF

Address Offset	0x61-0x61 in 0x26 byte increments		
Physical Address	0x0000 00BC-0x0000 00BC	**Instance**	PM_RECEIVER
Description	Sets the voltage roof of DC/DC regulator (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	VROOF						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	VROOF	Sets the voltage roof of DC/DC regulator when controlled by VMODE (VMODE_EN = 1)	RW	0x00

Table 5-319. Register Call Summary for Register VDD1_VROOF

Reset and Power-Management Programming Model
- Sequencing: [0]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-320. VDD1_STEP

Address Offset	0x62-0x62 in 0x26 byte increments		
Physical Address	0x0000 00BD-0x0000 00BD	**Instance**	PM_RECEIVER
Description	Set the step between 2 voltage changes for VDD1 resource (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			STEP_REG				

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:0	STEP_REG	Step between voltage changes STEP = STEP_REG * 10 µs That is from 10 µs to 310 µs When STEP_REG = 0, the DVS is in JUMP mode.	RW	0x00

Table 5-321. Register Call Summary for Register VDD1_STEP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-322. VDD2_DEV_GRP

Address Offset	0x63-0x63 in 0x26 byte increments		
Physical Address	0x0000 00BE-0x0000 00BE	**Instance**	PM_RECEIVER
Description	VDD2 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x2
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-323. Register Call Summary for Register VDD2_DEV_GRP

Reset and Power-Management Programming Model • Sequencing: [0]
Reset and Power-Management Registers • PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-324. VDD2_TYPE

Address Offset	0x64-0x64 in 0x26 byte increments		
Physical Address	0x0000 00BF-0x0000 00BF	**Instance**	PM_RECEIVER
Description	Resource type set (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x5

Table 5-325. Register Call Summary for Register VDD2_TYPE

Reset and Power-Management Registers • PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-326. VDD2_REMAP

Address Offset	0x65-0x65 in 0x26 byte increments		
Physical Address	0x0000 00C0-0x0000 00C0	**Instance**	PM_RECEIVER
Description	When the VDD2 device is in sleep or off mode, it allows setting the resource to active or off/sleep (VRRTC domain) by the nSLEEP2 pin. Not effective if VDD2 is put in sleep mode using SmartReflex I^2C bus (the VDD2_SR_CONTROL register). OFF_STATE and SLEEP_STATE details are given in Table 5-5, or the following values can be used: OFF = 0x0, SLEEP = 0x8, ACTIVE = 0xE.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-327. Register Call Summary for Register VDD2_REMAP

Reset and Power-Management Registers • PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-328. VDD2_CFG

Address Offset	0x66-0x66 in 0x26 byte increments		
Physical Address	0x0000 00C1-0x0000 00C1	**Instance**	PM_RECEIVER
Description	VDD2 configuration register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						EN_NDRV_LOWV	BUCK_HIZ_LOWV

Bits	Field Name	Description	Type	Reset
7:2	Reserved		R	0x00
1	EN_NDRV_LOWV	Forces PWM operation by requiring synchronous NMOS on every cycle	RW	0
0	BUCK_HIZ_LOWV	Hi-Z disable mode enable. VDIG level.	RW	0

Table 5-329. Register Call Summary for Register VDD2_CFG

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-330. VDD2_MISC_CFG

Address Offset	0x67-0x67 in 0x26 byte increments		
Physical Address	0x0000 00C2-0x0000 00C2	**Instance**	PM_RECEIVER
Description	VDD2 configuration register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			BUCK_AMUX		DRIVE_SEL		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	BUCK_AMUX		RW	0x0
2:0	DRIVE_SEL	Drive strength adjustment - test function	RW	0x0

Table 5-331. Register Call Summary for Register VDD2_MISC_CFG

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-332. VDD2_TEST1

Address Offset	0x68-0x68 in 0x26 byte increments		
Physical Address	0x0000 00C3-0x0000 00C3	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
TEST_ENB_CLMP700_LOWV	TEST_EN_2X_START_LOWV	TEST_ENB_ ANTIGLITCH_LOWV	TEST_ENB_ ERRAMP_LOWV	TEST_ENB_ILIMIT_LOWV	TEST_EN_MEAS_NRDS_LOWV	TEST_EN_MEAS_PRES_LOWV	TEST_ENB_SFTSTRT_LOWV

Bits	Field Name	Description	Type	Reset
7	TEST_ENB_CLMP700_LOWV		RW	0
6	TEST_EN_2X_START_LOWV		RW	0
5	TEST_ENB_ ANTIGLITCH_LOWV		RW	0
4	TEST_ENB_ ERRAMP_LOWV		RW	0
3	TEST_ENB_ILIMIT_LOWV		RW	0
2	TEST_EN_MEAS_NRDS_LOWV		RW	0
1	TEST_EN_MEAS_PRES_LOWV		RW	0
0	TEST_ENB_SFTSTRT_LOWV		RW	0

Table 5-333. Register Call Summary for Register VDD2_TEST1

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-334. VDD2_TEST2

Address Offset	0x69-0x69 in 0x26 byte increments		
Physical Address	0x0000 00C4-0x0000 00C4	**Instance**	PM_RECEIVER
Description	Write-protected with the KEY_TST (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	TEST_DC/DC				TEST_ENB_SYNC_ COMP_LOWV	TEST_ENB_SYNC_ LOWV	TEST_EN_ SLEWCTRL_LOWV

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:3	TEST_DC/DC		RW	0x0
2	TEST_ENB_SYNC_ COMP_LOWV		RW	0
1	TEST_ENB_SYNC_ LOWV		RW	0
0	TEST_EN_ SLEWCTRL_LOWV		RW	0

Table 5-335. Register Call Summary for Register VDD2_TEST2

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5] [6]

Table 5-336. VDD2_OSC

Address Offset	0x6A-0x6A in 0x26 byte increments		
Physical Address	0x0000 00C5-0x0000 00C5	**Instance**	PM_RECEIVER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				OVLAP_SEL		SH_RAMP_ SWITCH	

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
4:2	OVLAP_SEL	BUCK overlap time adjustment - test function	RW	0x0
1: 0	SH_RAMP_ SWITCH		RW	0x0

Table 5-337. Register Call Summary for Register VDD2_OSC

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4]

Table 5-338. VDD2_RESERVED

Address Offset	0x6B-0x6B in 0x26 byte increments		
Physical Address	0x0000 00C6-0x0000 00C6	**Instance**	PM_RECEIVER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-339. Register Call Summary for Register VDD2_RESERVED

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-340. VDD2_VSEL

Address Offset	0x6C-0x6C in 0x26 byte increments		
Physical Address	0x0000 00C7-0x0000 00C7	**Instance**	PM_RECEIVER
Description	Controls the output voltage (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	VSEL						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	VSEL	WRITE: Controls output voltage when VMODE_EN = 0 and SmartReflex not enabled READ: if READ_REG = 0: Controls output voltage if READ_REG = 1: Value of the register	RW	0x38

Table 5-341. Register Call Summary for Register VDD2_VSEL

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-342. VDD2_VMODE_CFG

Address Offset	0x6D-0x6D in 0x26 byte increments		
Physical Address	0x0000 00C8-0x0000 00C8	**Instance**	PM_RECEIVER
Description	vmode configuration register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		STS_BUSY	STS_ROOF	STS_FLOOR	DCDC_SLP	READ_REG	ENABLE_VMODE

Bits	Field Name	Description	Type	Reset
7:6	Reserved		R	0x0
5	STS_BUSY	0: DC/DC is not computing a VMODE transition. 1: DC/DC is computing a VMODE transition.	R	0
4	STS_ROOF	0: DC/DC did not reach VROOF voltage output. 1: DC/DC reached VROOF voltage output.	R	0
3	STS_FLOOR	0: DC/DC did not reach VFLOOR voltage output. 1: DC/DC reached VFLOOR voltage output.	R	0
2	DCDC_SLP	0: Output voltage in sleep mode is the same as in active mode. 1: Output voltage in sleep mode is VFLOOR. **Note:** Do not set this bit to 1 when the ENABLE_VMODE bit is set to 1.	RW	0
1	READ_REG	Enable VSEL register value read. This bit is reset to 0 when DC/DC is swoff or when a warm reset occurs.	RW	0
0	ENABLE_VMODE	0: DC/DC voltage controlled by software (through DC/DC_VSEL) 1: DC/DC voltage controlled by VMODE pin **Note:** Do not set this bit to 1 when the DCDC_SLP bit is set to 1.	RW	0

Table 5-343. Register Call Summary for Register VDD2_VMODE_CFG

Reset and Power-Management Integration • Resets: [0] [1] [2]
Reset and Power-Management Programming Model • Sequencing: [3]
Reset and Power-Management Registers • PM_RECEIVER Module Instance: [4] [5] [6] [7] [8] [9]

Table 5-344. VDD2_VFLOOR

Address Offset	0x6E-0x6E in 0x26 byte increments		
Physical Address	0x0000 00C9-0x0000 00C9	**Instance**	PM_RECEIVER
Description	Sets the voltage floor of DC/DC regulator (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	VFLOOR						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	VFLOOR	Sets the voltage floor of DC/DC regulator when controlled by VMODE (VMODE_EN = 1)	RW	0x00

Table 5-345. Register Call Summary for Register VDD2_VFLOOR

Reset and Power-Management Programming Model
- Sequencing: [0]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-346. VDD2_VROOF

Address Offset	0x6F-0x6F in 0x26 byte increments		
Physical Address	0x0000 00CA-0x0000 00CA	**Instance**	PM_RECEIVER
Description	Sets the voltage roof of DC/DC regulator (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved	VROOF						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	VROOF		RW	0x00

Table 5-347. Register Call Summary for Register VDD2_VROOF

Reset and Power-Management Programming Model
- Sequencing: [0]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [1] [2] [3] [4] [5] [6]

Table 5-348. VDD2_STEP

Address Offset	0x70-0x70 in 0x26 byte increments		
Physical Address	0x0000 00CB-0x0000 00CB	**Instance**	PM_RECEIVER
Description	Set the step between voltage changes for VDD1 resource (VRRTC domain).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			STEP_REG				

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:0	STEP_REG	Step between voltage changes STEP = STEP_REG * 10 µs. That is from 10 µs to 310 µs. When STEP_REG = 0, the DVS is in JUMP mode.	RW	0x00

Table 5-349. Register Call Summary for Register VDD2_STEP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-350. VUSB1V5_DEV_GRP

Address Offset	0x71-0x71 in 0xE byte increments		
Physical Address	0x0000 00CC-0x0000 00CC	**Instance**	PM_RECEIVER
Description	Voltage regulator: VUSB1V5 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x0
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-351. Register Call Summary for Register VUSB1V5_DEV_GRP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-352. VUSB1V5_TYPE

Address Offset	0x72-0x72 in 0xE byte increments		
Physical Address	0x0000 00CD-0x0000 00CD	**Instance**	PM_RECEIVER
Description	VUSB1V5 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-353. Register Call Summary for Register VUSB1V5_TYPE

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-354. VUSB1V5_REMAP

Address Offset	0x73-0x73 in 0xE byte increments		
Physical Address	0x0000 00CE-0x0000 00CE	**Instance**	PM_RECEIVER
Description	When the VUSB1V5 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-355. Register Call Summary for Register VUSB1V5_REMAP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-356. VUSB1V8_DEV_GRP

Address Offset	0x74-0x74 in 0xE byte increments		
Physical Address	0x0000 00CF-0x0000 00CF	**Instance**	PM_RECEIVER
Description	Voltage regulator: VUSB1V8 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	000: Belongs to no device group	RW	0x0
		001: Belongs to P1 device group		
		010: Belongs to P2 device group		
		011: Belongs to P1 and P2 device groups		
		100: Belongs to P3 device group		
		101: Belongs to P1 and P3 device groups		
		110: Belongs to P2 and P3 device groups		
		111: Belongs to all device groups		
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value.	RW	0x0
		0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.		
3:0	STATE	Current state of the resource	RW	0x8

Table 5-357. Register Call Summary for Register VUSB1V8_DEV_GRP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-358. VUSB1V8_TYPE

Address Offset	0x75-0x75 in 0xE byte increments		
Physical Address	0x0000 00D0-0x0000 00D0	**Instance**	PM_RECEIVER
Description	VUSB1V8 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-359. Register Call Summary for Register VUSB1V8_TYPE

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-360. VUSB1V8_REMAP

Address Offset	0x76-0x76 in 0xE byte increments		
Physical Address	0x0000 00D1-0x0000 00D1	**Instance**	PM_RECEIVER
Description	When the VUSB1V8 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-361. Register Call Summary for Register VUSB1V8_REMAP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-362. VUSB3V1_DEV_GRP

Address Offset	0x77-0x77 in 0xE byte increments		
Physical Address	0x0000 00D2-0x0000 00D2	**Instance**	PM_RECEIVER
Description	Voltage regulator: VUSB3V1 device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-363. Register Call Summary for Register VUSB3V1_DEV_GRP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-364. VUSB3V1_TYPE

Address Offset	0x78-0x78 in 0xE byte increments		
Physical Address	0x0000 00D3-0x0000 00D3	**Instance**	PM_RECEIVER
Description	VUSB3V1 resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-365. Register Call Summary for Register VUSB3V1_TYPE

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-366. VUSB3V1_REMAP

Address Offset	0x79-0x79 in 0xE byte increments		
Physical Address	0x0000 00D4-0x0000 00D4	**Instance**	PM_RECEIVER
Description	When the VUSB3V1 device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-367. Register Call Summary for Register VUSB3V1_REMAP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-368. VUSBCP_DEV_GRP

Address Offset	0x7A-0x7A in 0xE byte increments		
Physical Address	0x0000 00D5-0x0000 00D5	**Instance**	PM_RECEIVER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-369. Register Call Summary for Register VUSBCP_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-370. VUSBCP_TYPE

Address Offset	0x7B-0x7B in 0xE byte increments		
Physical Address	0x0000 00D6-0x0000 00D6	**Instance**	PM_RECEIVER
Description	VUSBCP resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-371. Register Call Summary for Register VUSBCP_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-372. VUSBCP_REMAP

Address Offset	0x7C-0x7C in 0xE byte increments		
Physical Address	0x0000 00D7-0x0000 00D7	**Instance**	PM_RECEIVER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		R	0x00

Table 5-373. Register Call Summary for Register VUSBCP_REMAP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-374. VUSB_DEDICATED1

Address Offset	0x7D-0x7D in 0xE byte increments		
Physical Address	0x0000 00D8-0x0000 00D8	**Instance**	PM_RECEIVER
Description	Voltage regulator: VUSB basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			WKUPCOMP_EN	SW2VBUS	SW2VBAT	G1	G0

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RW	0x0
4	WKUPCOMP_EN	Enable the VBUS and ID wake-up comparators. For testing only, to evaluate VRRTC current consumption. See USB specification.	RW	1
3	SW2VBUS	VRUSB_3V1 VDD switch to VBUS See USB specification.	RW	0
2	SW2VBAT	VRUSB_3V1 VDD switch to VBAT See USB specification.	RW	1
1	G1	Gain loop trimming (for test mode) See USB specification.	RW	0
0	G0	Gain loop trimming (for test mode) See USB specification.	RW	0

Table 5-375. Register Call Summary for Register VUSB_DEDICATED1

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-376. VUSB_DEDICATED2

Address Offset	0x7E-0x7E in 0xE byte increments		
Physical Address	0x0000 00D9-0x0000 00D9	**Instance**	PM_RECEIVER
Description	Voltage regulator: VUSB basic settings (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				VUSB3V1_SLEEP	Reserved		

Bits	Field Name	Description	Type	Reset
7:4	Reserved		R	0x0
3	VUSB3V1_SLEEP	1: Remap the ACTIVE state to SLEEP state. 0: ACTIVE state remapping disabled	RW	1
2:0	Reserved		R	0x0

Table 5-377. Register Call Summary for Register VUSB_DEDICATED2

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-378. REGEN_DEV_GRP

Address Offset	0x7F-0x7F in 0x15 byte increments		
Physical Address	0x0000 00DA-0x0000 00DA	**Instance**	PM_RECEIVER
Description	Device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-379. Register Call Summary for Register REGEN_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-380. REGEN_TYPE

Address Offset	0x80-0x80 in 0x15 byte increments		
Physical Address	0x0000 00DB-0x0000 00DB	**Instance**	PM_RECEIVER
Description	Resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x2

Table 5-381. Register Call Summary for Register REGEN_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-382. REGEN_REMAP

Address Offset	0x81-0x81 in 0x15 byte increments		
Physical Address	0x0000 00DC-0x0000 00DC	**Instance**	PM_RECEIVER
Description	When the device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-383. Register Call Summary for Register REGEN_REMAP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-384. NRESPWRON_DEV_GRP

Address Offset	0x82-0x82 in 0x15 byte increments		
Physical Address	0x0000 00DD-0x0000 00DD	**Instance**	PM_RECEIVER
Description	NRESPWRON device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-385. Register Call Summary for Register NRESPWRON_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4]

Table 5-386. NRESPWRON_TYPE

Address Offset	0x83-0x83 in 0x15 byte increments		
Physical Address	0x0000 00DE-0x0000 00DE	**Instance**	PM_RECEIVER
Description	NRESPWRON resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-387. Register Call Summary for Register NRESPWRON_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-388. NRESPWRON_REMAP

Address Offset	0x84-0x84 in 0x15 byte increments		
Physical Address	0x0000 00DF-0x0000 00DF	**Instance**	PM_RECEIVER
Description	When the device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-389. Register Call Summary for Register NRESPWRON_REMAP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-390. CLKEN_DEV_GRP

Address Offset	0x85-0x85 in 0x15 byte increments		
Physical Address	0x0000 00E0-0x0000 00E0	**Instance**	PM_RECEIVER
Description	CLKEN device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-391. Register Call Summary for Register CLKEN_DEV_GRP

Resets and Power-Management Environment • CLKEN: [0] [1]
Reset and Power-Management Registers • PM_RECEIVER Module Instance: [2] [3] [4] [5] [6] [7]

Table 5-392. CLKEN_TYPE

Address Offset	0x86-0x86 in 0x15 byte increments		
Physical Address	0x0000 00E1-0x0000 00E1	**Instance**	PM_RECEIVER
Description	CLKEN resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x5

Table 5-393. Register Call Summary for Register CLKEN_TYPE

Reset and Power-Management Registers • PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-394. CLKEN_REMAP

Address Offset	0x87-0x87 in 0x15 byte increments		
Physical Address	0x0000 00E2-0x0000 00E2	**Instance**	PM_RECEIVER
Description	When the device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-395. Register Call Summary for Register CLKEN_REMAP

Reset and Power-Management Registers • PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-396. SYSEN_DEV_GRP

Address Offset	0x88-0x88 in 0x15 byte increments		
Physical Address	0x0000 00E3-0x0000 00E3V	**Instance**	PM_RECEIVER
Description	Device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-397. Register Call Summary for Register SYSEN_DEV_GRP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-398. SYSEN_TYPE

Address Offset	0x89-0x89 in 0x15 byte increments		
Physical Address	0x0000 00E4-0x0000 00E4	**Instance**	PM_RECEIVER
Description	Resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x6

Table 5-399. Register Call Summary for Register SYSEN_TYPE

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-400. SYSEN_REMAP

Address Offset	0x8A-0x8A in 0x15 byte increments		
Physical Address	0x0000 00E5-0x0000 00E5	**Instance**	PM_RECEIVER
Description	When the device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-401. Register Call Summary for Register SYSEN_REMAP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-402. HFCLKOUT_DEV_GRP

Address Offset	0x8B-0x8B in 0x15 byte increments		
Physical Address	0x0000 00E6-0x0000 00E6	**Instance**	PM_RECEIVER
Description	HFCLKOUT device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value.	RW	0

Bits	Field Name	Description	Type	Reset
		0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.		
3:0	STATE	Current state of the resource	R	0x0

Table 5-403. Register Call Summary for Register HFCLKOUT_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-404. HFCLKOUT_TYPE

Address Offset	0x8C-0x8C in 0x15 byte increments		
Physical Address	0x0000 00E7-0x0000 00E7	**Instance**	PM_RECEIVER
Description	HFCLKOUT resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-405. Register Call Summary for Register HFCLKOUT_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-406. HFCLKOUT_REMAP

Address Offset	0x8D-0x8D in 0x15 byte increments		
Physical Address	0x0000 00E8-0x0000 00E8	**Instance**	PM_RECEIVER
Description	When the device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-407. Register Call Summary for Register HFCLKOUT_REMAP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-408. 2KCLKOUT_DEV_GRP

Address Offset	0x8E-0x8E in 0x15 byte increments		
Physical Address	0x0000 00E9-0x0000 00E9	**Instance**	PM_RECEIVER
Description	32KCLKOUT device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-409. Register Call Summary for Register 2KCLKOUT_DEV_GRP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-410. 32KCLKOUT_TYPE

Address Offset	0x8F-0x8F in 0x15 byte increments		
Physical Address	0x0000 00EA-0x0000 00EA	**Instance**	PM_RECEIVER
Description	32KCLKOUT resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-411. Register Call Summary for Register 32KCLKOUT_TYPE

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-412. 32KCLKOUT_REMAP

Address Offset	0x90-0x90 in 0x15 byte increments		
Physical Address	0x0000 00EB-0x0000 00EB	**Instance**	PM_RECEIVER
Description	When the device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-413. Register Call Summary for Register 32KCLKOUT_REMAP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-414. TRITON_RESET_DEV_GRP

Address Offset	0x91-0x91 in 0x15 byte increments		
Physical Address	0x0000 00EC-0x0000 00EC	**Instance**	PM_RECEIVER
Description	Device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value.	RW	0

Bits	Field Name	Description	Type	Reset
		0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.		
3:0	STATE	Current state of the resource	R	0x0

Table 5-415. Register Call Summary for Register TRITON_RESET_DEV_GRP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-416. TRITON_RESET_TYPE

Address Offset	0x92-0x92 in 0x15 byte increments		
Physical Address	0x0000 00ED-0x0000 00ED	**Instance**	PM_RECEIVER
Description	Resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x6

Table 5-417. Register Call Summary for Register TRITON_RESET_TYPE

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-418. TRITON_RESET_REMAP

Address Offset	0x93-0x93 in 0x15 byte increments		
Physical Address	0x0000 00EE-0x0000 00EE	**Instance**	PM_RECEIVER
Description	When the device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x6

Table 5-419. Register Call Summary for Register TRITON_RESET_REMAP

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-420. MAINREF_DEV_GRP

Address Offset	0x94-0x94 in 0x3 byte increments		
Physical Address	0x0000 00EF-0x0000 00EF	**Instance**	PM_RECEIVER
Description	Voltage regulator: Main reference device group register (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	R	0x0

Table 5-421. Register Call Summary for Register MAINREF_DEV_GRP

Reset and Power-Management Registers

- PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-422. MAINREF_TYPE

Address Offset	0x95-0x95 in 0x3 byte increments		
Physical Address	0x0000 00F0-0x0000 00F0	**Instance**	PM_RECEIVER
Description	Main reference resource type setting (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		R	0x0
4:3	RES_TYPE2	Resource type 2 (used primarily for warm reset)	RW	0x0
2:0	RES_TYPE	Resource type	RW	0x0

Table 5-423. Register Call Summary for Register MAINREF_TYPE

Reset and Power-Management Registers • PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

Table 5-424. MAINREF_REMAP

Address Offset	0x96-0x96 in 0x3 byte increments		
Physical Address	0x0000 00F1-0x0000 00F1	**Instance**	PM_RECEIVER
Description	When the main reference device is in sleep or off mode, allows setting the resource to active or off/sleep (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in off mode, the OFF_STATE allows setting the resource to sleep or active mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in sleep mode, the SLEEP_STATE allows setting the resource to off or active mode.	RW	0x8

Table 5-425. Register Call Summary for Register MAINREF_REMAP

Reset and Power-Management Registers • PM_RECEIVER Module Instance: [0] [1] [2] [3] [4] [5]

5.6.4 SMARTREFLEX_REG

Table 5-426. Instance Summary

Module Name	Base Address	Size
SMARTREFLEX_REG	0x0000 0000	2 bytes

This section provides information about the SMARTREFLEX_REG module instance in this product. Each register in the module Instance is described separately below.

Vbat Domain

Table 5-427. SMARTREFLEX_REG Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
VDD1_SR_CONTROL	RW	8	0x0000 0000
VDD2_SR_CONTROL	RW	8	0x0000 0001

Table 5-428. VDD1_SR_CONTROL

Address Offset	0x00		
Physical Address	0x0000 0000	**Instance**	SMARTREFLEX_REG
Description	Vbat domain		
	If the user writes X1111111 in this register, only the MODE bit is updated (the VSEL field is not updated).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
MODE	VSEL						

Bits	Field Name	Description	Type	Reset
7	MODE	0: VDD1 is in active mode.	RW	0
		1: VDD1 is in sleep mode.		
6:0	VSEL	DC/DC voltage: VSEL*12.5 mV + 0.6 V	RW	0x30

Table 5-429. Register Call Summary for Register VDD1_SR_CONTROL

Reset and Power Management Functional Description
- Management Using I2C SmartReflex Control in C021 Mode: [0] [1]

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [2]
- SMARTREFLEX_REG: [3]

Table 5-430. VDD2_SR_CONTROL

Address Offset	0x01		
Physical Address	0x0000 0001	**Instance**	PM_RECEIVER
Description	Vbat domain		
	If the user writes X1111111 in this register, only the MODE bit is updated (the VSEL bit field is not updated).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
MODE	VSEL						

Bits	Field Name	Description	Type	Reset
7	MODE	0: VDD2 is in active mode (and associated resources VPLL and VIO are in active mode).	RW	0
		1: VDD2 is in sleep mode (VPLL is in sleep mode and VIO is in sleep mode if no other processor needs it).		
6:0	VSEL	DC/DC voltage: VSEL*12.5 mV + 0.6 V	RW	0x30

Table 5-431. Register Call Summary for Register VDD2_SR_CONTROL

Reset and Power-Management Registers
- PM_RECEIVER Module Instance: [0]
- SMARTREFLEX_REG: [1]

Power Resources

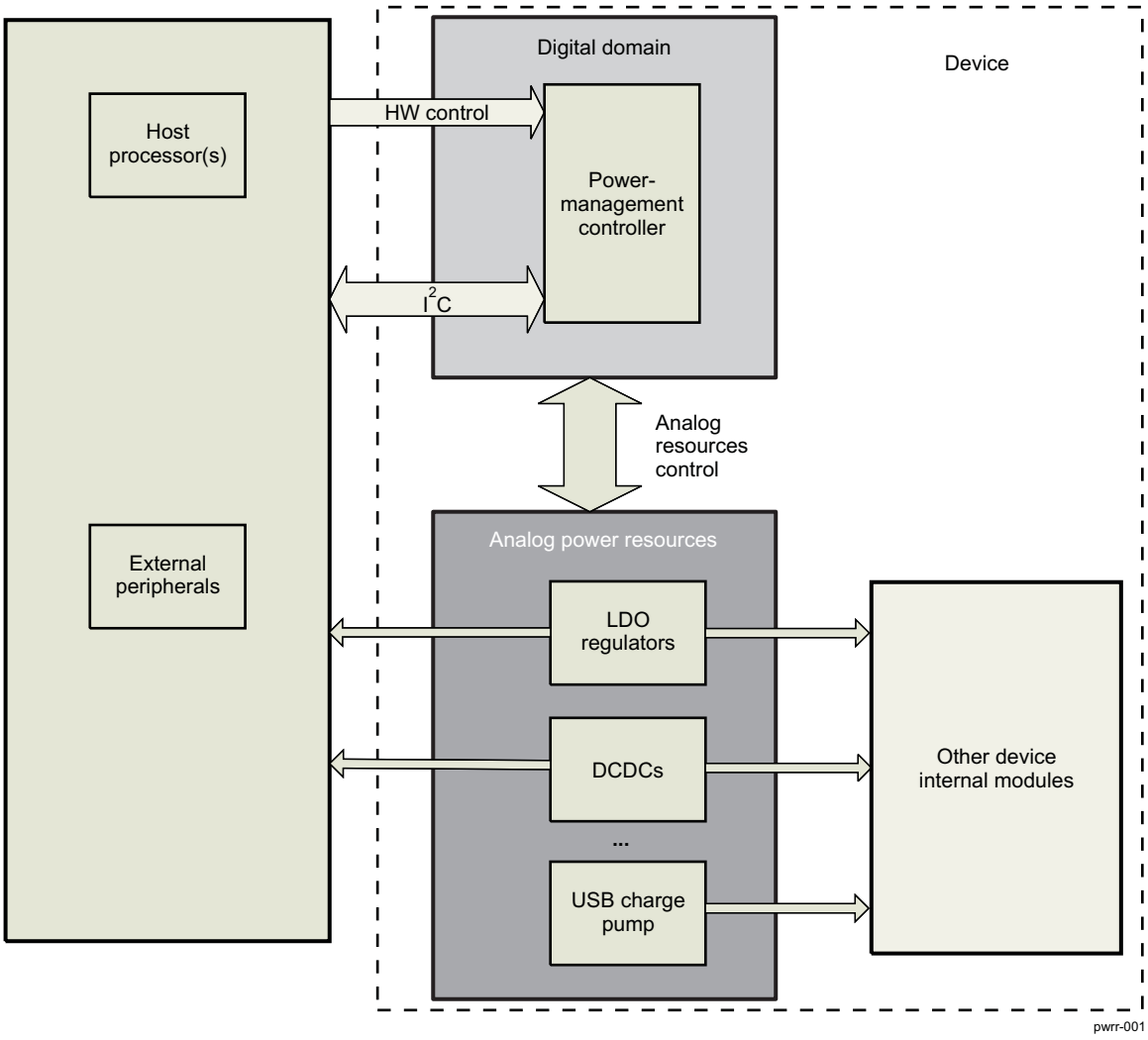
This chapter describes the power resources of the device integrated power-management/audio coder/decoder (codec) device.

Topic **Page**

6.1 Power Resources Overview

This chapter describes the power resources the device provides to external host processors and external peripherals, and to modules in the device. This chapter also provides the programming model and describes the registers that control the power resources. Figure 6-1 is a top-level block diagram of the device power resources.

Figure 6-1. Device Power Resource Overview



The device provides the following power resource features:

- VDD1 and VDD2 switch mode power supply (SMPS) stepdown converters with configurable output voltages. These converters provide a core supply to the host processors.
- VIO SMPS with fixed output voltage for input/output (I/O) ports, external memories on the system, and device internal modules
- Active, sleep, and off modes for SMPS regulators
- Several low dropout (LDO) regulators that provide power to internal analog and digital circuits, digital baseband counterparts, and external components
- LDO regulators (except for some internal digital and analog LDO regulators) with programmable output and configurable modes of operation among off, sleep, and active modes
- Universal serial bus (USB) charge pump to power the USB VBUS

6.2 Power Resource Environment

This section describes the device power resources and how they interface with external components.

Figure 6-2 shows the device power resources and the external pinout.

Figure 6-2. Device Power Resource Environment

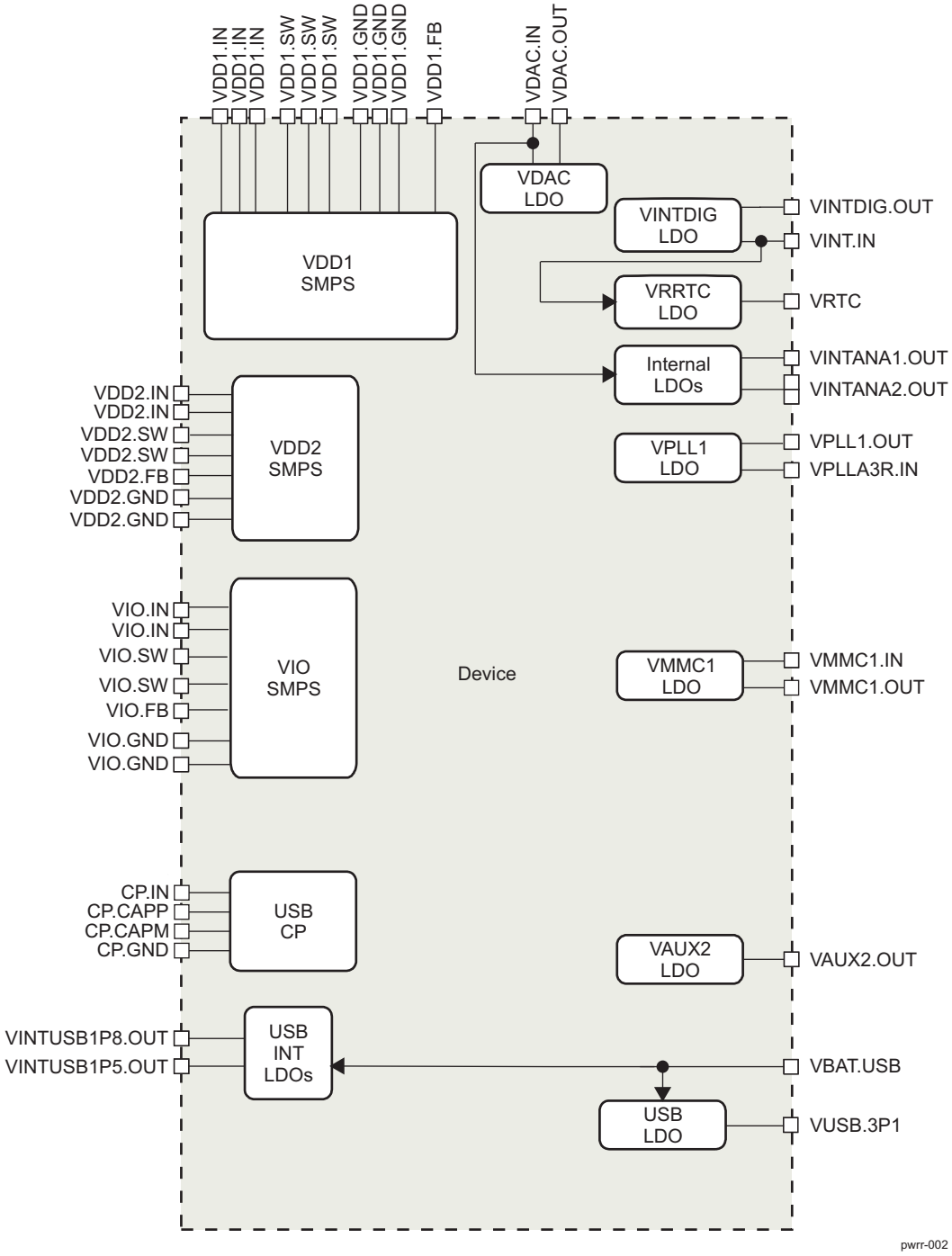


Table 6-1 lists the pins shown in Figure 6-2.

Table 6-1. Device Power Resource Pins

Power Resource	Pin Name	I/O	PAD [1]	Number of Pins Assigned	Description/Comment
VDD1	VDD1.IN	I	Y	3	Input voltage dedicated to VDD1
	VDD1.SW	O	Y	3	VDD1 switch
	VDD1.GND	I	Y	3	VDD1 ground
	VDD1.FB	O	Y	1	VDD1 output
VDD2	VDD2.IN	I	Y	2	Input voltage dedicated to VDD2
	VDD2.SW	O	Y	2	VDD2 switch
	VDD2.GND	I	Y	2	VDD2 ground
	VDD2.FB	O	Y	1	VDD2 output
VIO	VIO.IN	I	Y	2	Input voltage dedicated to VIO
	VIO.SW	O	Y	2	VIO switch
	VIO.GND	I	Y	2	VIO ground
	VIO.FB	O	Y	1	VIO output
LDO VDAC	VDAC.IN	I	Y	1	LDO power input
	VDAC.OUT	O	Y	1	LDO output
LDO VPLL1	VPLLA3R.IN	I	Y	1	LDO power input
	VPLL1.OUT	O	Y	1	LDO output
LDO VMMC1	VMMC1.IN	I	Y	1	Dedicated LDO power input
	VMMC1.OUT	O	Y	1	LDO output
LDO VSIM	VAUX12S.IN	I	Y	1	LDO power input
LDO VAUX2	VAUX2.OUT	O	Y	1	LDO power input: VAUX12S.IN
LDO VINTDIG	VINT.IN	I	Y	1	LDO power input
	VINTDIG.OUT	O	Y	1	LDO output
LDO VINTANA1	VINTANA1.OUT	O	Y	1	LDO power input: VDAC.IN
LDO VINTANA2	VINTANA2.OUT	O	Y	1	LDO power input: VDAC.IN
Power control	VRTC.OUT	O	Y	1	VRTC output common to VRRTC and VBRTC regulators (VRRTC LDO power input: VINT.IN)
	VBATS	I	Y	1	Sense pin on the main battery

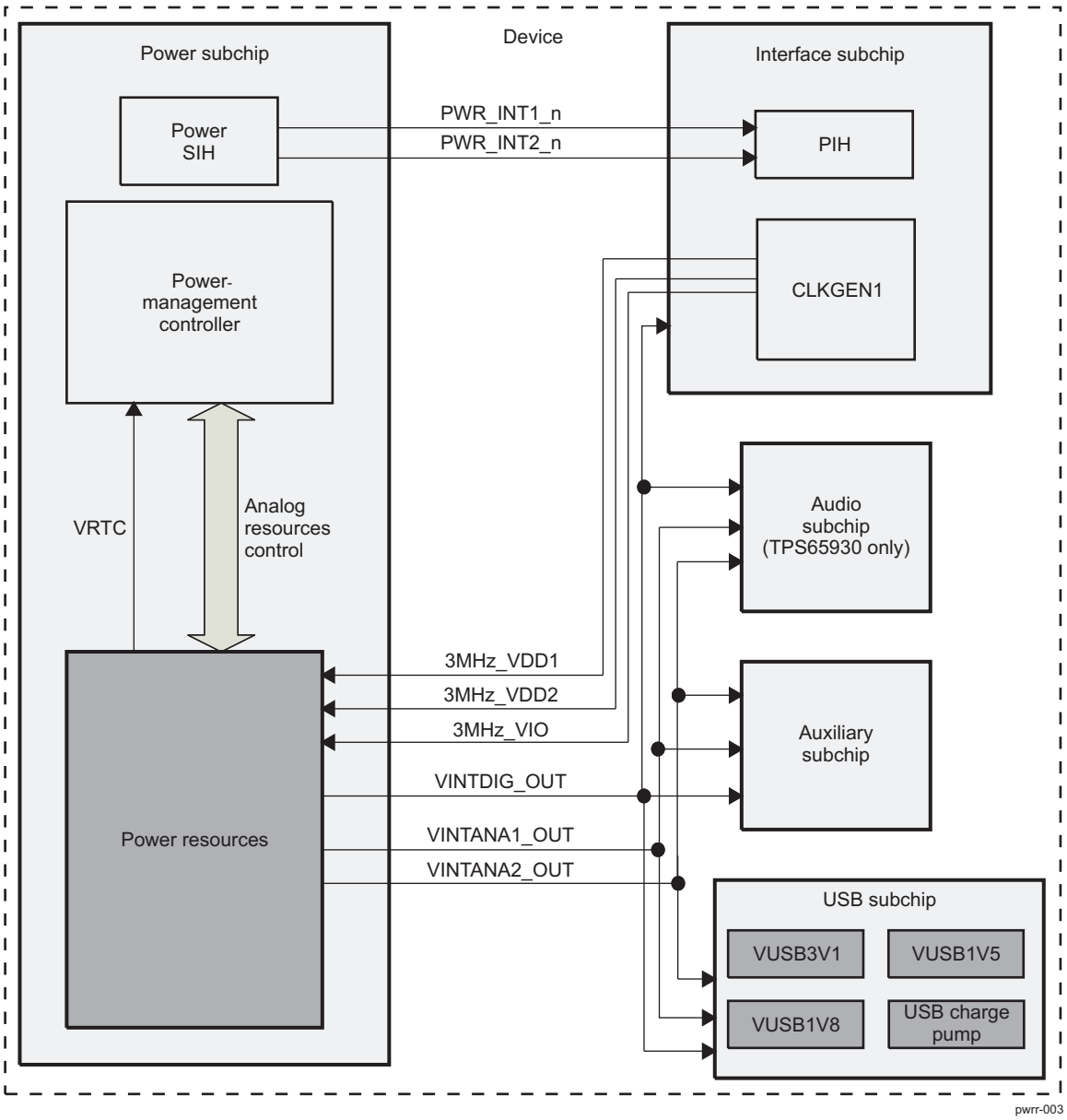
[1] PAD: Y: The module I/O is connected to an I/O pad.

6.3 Power Resource Integration

This section describes the power resources and how they interact with modules in the device. The power supplies are powered by the battery supply VBAT, unless otherwise stated.

Figure 6-3 shows the interaction of the device power resources.

Figure 6-3. Device Power Resource Integration



The CLKGEN1 module of the interface subchip generates three 3-MHz clocks for the ramp generator modules of the VDD1, VDD2, and VIO power supplies.

When the SC_DETECT interrupt is enabled and a short circuit occurs in some of the power providers, the secondary interrupt handler (SIH) of the power subchip generates two interrupts to the primary interrupt handler (PIH) of the interface subchip. The PIH can then generate an interrupt to the host processor. For more information about short-circuit detection and the resulting interrupt generation, see Section 6.4.4, *Short-Circuit Protection*.

The power state controller uses the VRTC supply generated from the VRRTC LDO or the VBRTC LDO.

The digital sections of the subchips use the output of the VINTDIG LDO. The analog modules of the audio, USB, and auxiliary subchips use the VINTANA1 and VINTANA2 analog supplies.

6.4 Functional Description

The power resources provided by the device include the SMPS, LDOs, and a USB charge pump (see Figure 6-4). These regulators supply power to the external processor cores and external components, and to modules in the device.

Figure 6-4. Power Resource Functional Description

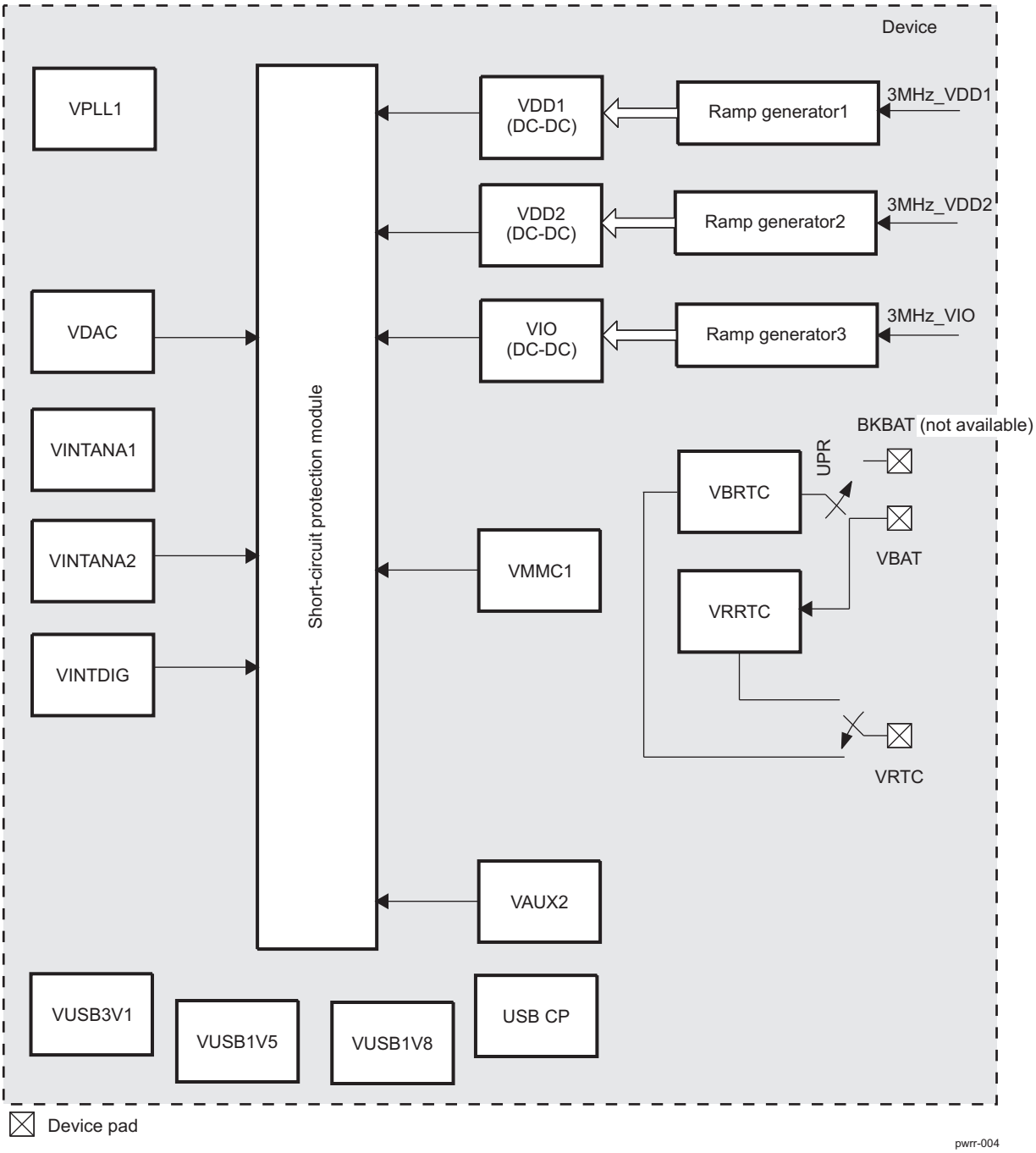


Table 6-2 summarizes the power resources.

Table 6-2. Device Power Resource Summary

Resource	Type	Voltage Range	Maximum Current (mA)	Sleep Current (mA)	Accuracy (%)
VDD1	SMPS	0.6 V to 0.8 V	1200	0	–6/+6
		0.8 V to 1.45 V			–4/+4
VDD2	SMPS	0.6 V to 0.8 V	600	10	–6/+6
		0.8 V to 1.45 V			–4/+4
		1.5 V			–4/+4
VIO	SMPS	1.8 V, 1.85 V	600	10	−4/+4
USB CP	CP	5 V	100	N/A	−12/+5
VUSB3V1[1]	LDO	3.10 V	15	N/A	−3/+3
VUSB1V5[1]	LDO	1.5 V	30	N/A	N/A
VUSB1V8[1]	LDO	1.8 V	30	N/A	N/A
VDAC	LDO	1.2 V, 1.3 V, 1.8 V	65	/5	−3/+3
VPLL1	LDO	1.0 V, 1.2 V, 1.3 V, 1.8 V	40	5	−3/+3
VMMC1	LDO	1.85 V, 2.85 V, 3.0 V, 3.15 V	220	5	−3/+3
VAUX2	LDO	1.3 V, 1.5 V, 1.7 V, 1.8 V, 1.9 V, 2.0 V, 2.1 V, 2.2 V, 2.3 V, 2.4 V, 2.5 V or 2.8 V	100	5	−3/+3
VINTDIG[2]	LDO	1.5 V	100	5	N/A
VRRTC[2] VBRTC[2]	LDO	1.5 V			N/A
VINTANA1[2]	LDO	1.5 V	30	5	N/A
VINTANA2[2]	LDO	2.5 V, 2.75 V	250	5	N/A

(1) Device internal use only
(2) Device internal use only

Each power resource can be owned by one or more resource groups, depending on the value programmed in the <resource name>_DEV_GRP DEV_GRP bit field. Each resource can be classified as a different type by programming the RES_TYPE and RES_TYPE2 bit fields of the <resource name>_TYPE register.

For more information about programming the power registers, see Chapter 5, *Resets and Power Management*.

6.4.1 Switch Mode Power Supplies

The device has three SMPSs: VDD1, VDD2, and VIO.

VDD1 and VDD2 power processor cores, and VIO powers external I/Os and memories. Depending on system requirements and also to optimize mean consumption, three operating modes are allowed for each DC/DC supply:

- Off: Output voltage is not maintained, and DC/DC power consumption is null. This mode is also called power-down mode.
- Active: The DC/DC can deliver its nominal output voltage with a full-load current capability. The clock for the 3-MHz oscillator is the local oscillator or an external high-frequency clock.
- Sleep: The nominal output voltage is maintained with low power consumption, but also with a low load-current capability. The clock for the 3-MHz oscillator is the local oscillator.

The SMPS operates with three modulation schemes:

- Light pulse frequency modulation (PFM)
- Fast PFM
- Continuous pulse-width modulation (PWM)

The light PFM scheme is a high-efficiency power-saving mode when the SMPS is in sleep mode. The SMPS moves between the light PFM and fast PFM schemes when the regulator enters and exits sleep mode. When the SMPS is in active mode, it can operate in fast PFM for low load currents and in

continuous PWM for moderate-to-heavy load currents. The SMPS moves automatically between the fast PFM and continuous PWM schemes, depending on the load requirements. This automatic change of modulation schemes is possible because the EN_NDRV_LOWV bit (for example, VIO_CFG[1]) is set to a default value of 0. When the EN_NDRV_LOWV bit is set to 1, the SMPS is forced to operate with the PWM scheme in active mode, regardless of the load current. If this forced PWM is used, software must reset the EN_NDRV_LOWV bit to 0 before going to sleep mode.

Each SMPS has an internal soft-start circuit that limits inrush current during startup. This prevents drops in input voltage.

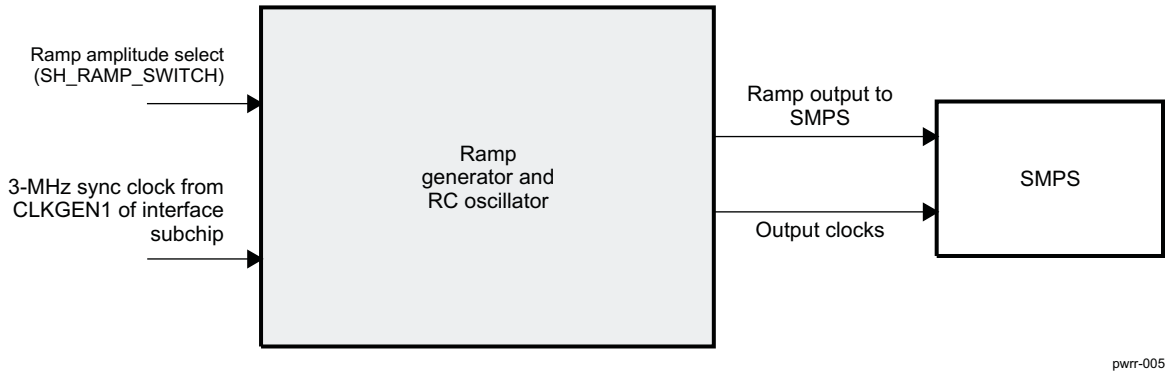
The SMPS SLEEP and OFF states can be modified by writing to the SLEEP_STATE and OFF_STATE bit fields of the <resource name>_REMAP register where <resource name> is VDD1, VDD2, or VIO. The SLEEP_STATE bit field indicates the state to be taken by the resource in case of a system sleep transition. The default value at reset for the SLEEP_STATE bit field lets the resource go to sleep mode. The software, however, can program the SLEEP_STATE bit field to let the resource be in off or active mode when the system requires the resource to be in sleep mode. Similarly, the OFF_STATE bit field indicates the state to be taken by the resource in case of a system off transition. The default value at reset for the OFF_STATE bit field lets the resource go to off mode. The software, however, can program the OFF_STATE bit field to let the resource be in sleep or active mode when the system requires the resource to be in off mode. The current state of the resource can be read from the STATE bit field of the <resource name>_DEV_GRP bit field where <resource name> is VDD1, VDD2, or VIO. For more information about how to program these registers, see Chapter 5, *Resets and Power Management*.

A 3-MHz oscillator circuit is part of the switching regulator system for each SMPS (see Figure 6-5). There are three resistance/capacitive (RC) oscillator circuits, one each for the VDD1, VDD2, and VIO SMPS. The generated ramp is compared to a reference to generate two clock outputs at the same frequency, but with different duty cycles. The ramp frequency can be synchronized with the internal clock or with an external clock source of the same frequency. In internal clock mode, the clock is generated internally, and the frequency is determined by charging the internal capacitor linearly and comparing the ramp voltage against the set reference level. When using external clock synchronization, the ramp comparison comparator is powered down, and the frequency is the same as that of the external clock input.

Each regulator has registers (VDD1_OSC, VDD2_OSC, and VIO_OSC) associated with it to configure the ramp amplitude and ramp frequency. The ramp amplitude can be adjusted by setting the SH_RAMP_SWITCH bit field of the corresponding <SMPS power resource>_OSC register. The SH_RAMP_SWITCH bit field lets ramp voltage be changed between 200 mV, 300 mV, and 400 mV, with the default set to 300 mV.

The ramp generator frequency is synchronized with its own internal RC oscillator. Figure 6-5 is a block diagram of the ramp generator.

Figure 6-5. Ramp Generator Block Diagram



6.4.1.1 VDD1 SMPS Regulator

The VDD1 SMPS is a 1.2 A stepdown power converter with configurable output voltage between 0.6 V and 1.45 V in steps of 12.5 mV. This regulator can power the host processor core. The host processor can request the device to scale the VDD1 output voltage to reduce power consumption. The default output voltage at power-up depends on the boot mode settings.

The output voltage of the VDD1 SMPS regulator can be scaled by software or hardware by setting the VDD1_VMODE_CFG[0] ENABLE_VMODE bit. In each of these modes, the output voltage ramp can be single-step or multiple-step, depending on the value of the VDD1_STEP[4:0] STEP_REG bit field. Apart from these modes, the VDD1 SMPS output voltage can be controlled by the host processor through the SmartReflex™ inter-integrated circuit (I^2C) interface between the host processor and the device. The default voltage scaling method selected at reset is a software-controlled mode.

Regardless of the mode used, VDD1 can be configured to the same output voltage in sleep mode as in active mode by programming the DD1_VMODE_CFG[2] DCDC_SLP bit to 0. When the DCDC_SLP bit is 1, the sleep mode output voltage of VDD1 equals the floor voltage that corresponds to the VDD1_VFLOOR[6:0] VFLOOR bit field.

CAUTION

Do not enable the DCDC_SLP and ENABLE_VMODE bits of the VDDx_VMODE_CFG register at the same time.

6.4.1.1.1 Synchronized Scaling Hardware Strategy (ENABLE_VMODE = 1)

When the VDD1_VMODE_CFG[0] ENABLE_VMODE bit is set to 1, the output voltage of the VDD1 SMPS is controlled by hardware using the VMODE1 signal from the host processor. The host processor must program through the I^2C bus the output voltage associated with the two states of the VMODE1 signal, by programming the VDD1_VROOF[6:0] VROOF and VDD1_VFLOOR[6:0] VFLOOR bit fields. Depending on VMODE1 transitions, the output of VDD1 changes immediately between the voltages that correspond to the VFLOOR and VROOF bit fields.

When the VDD1 output voltage transitions toward the VFLOOR voltage, software can read the VDD1_VMODE_CFG[3] STS_FLOOR bit to check whether the output voltage has reached the VFLOOR level. Similarly, the VDD1_VMODE_CFG[4] STS_ROOF bit shows the status when the output transitions toward the VROOF level. The VDD1_VMODE_CFG[5] STS_BUSY bit indicates whether VDD1 is computing a VMODE transition. Software can also read the instantaneous value of the VDD1 output voltage by reading the VDD1_VSEL[6:0] VSEL bit field after setting the VDD1_VMODE_CFG[1] READ_REG bit to 0.

The two operating modes (single-step and multiple-step) of the SMPS converter can be configured by programming the VDD1_STEP[4:0] STEP_REG bit field.

6.4.1.1.2 Direct Strategy Software Scaling Mode (ENABLE_VMODE = 0)

This mode is entered by writing 0 to the VDD1_VMODE_CFG[0] ENABLE_VMODE bit and disabling the SmartReflex interface. The host processor writes the required output voltage directly to the VDD1_VSEL[6:0] VSEL bit field. The output voltage is given by VSEL*12.5 mV + 600 mV.

When the VDD1_VMODE_CFG[1] READ_REG bit is 1, VSEL shows the voltage level programmed for the VDD1 regulator.

In this mode, the VDD1_VFLOOR[6:0] VDD1_VFLOOR and VDD1_VROOF[6:0] VDD1_VROOF bit fields are not used, and the voltage change is independent of the VMODE1 signal. The SMPS converter can operate in multiple-step and single-step modes, depending on the value of the VDD1_STEP[4:0] STEP_REG bit field.

6.4.1.1.3 Single-Step Voltage-Scaling Mode (STEP_REG = 0)

This mode is entered by setting the STEP_REG field to 0, regardless of the mode of control (ENABLE_VMODE = 0 or 1). In this mode, the SMPS output voltage ramps with the maximum slew rate when a voltage transition is required.

6.4.1.1.4 Multiple-Step Voltage-Scaling Mode (STEP_REG ≠ 0)

This mode is entered when the VDD1_STEP[4:0] STEP_REG bit field has a nonzero value. In this mode, SMPS controls the voltage ramp in 12.5-mV steps by adjusting the time between steps in the voltage. The time between steps equals n clock periods of the 3-MHz RC oscillator circuit where n is the value of the STEP_REG bit field.

6.4.1.1.5 SmartReflex Voltage-Scaling Mode

VDD1 and VDD2 provide SmartReflex-compliant voltage management. The SmartReflex controller in the host processor interfaces with the device counterpart through the use of a dedicated I^2C bus. The host processor computes the required voltage and informs the device using the SmartReflex I^2C interface. For details about the SmartReflex I^2C interface, see Chapter 2, *Control Interface*.

SmartReflex control of the VDD1 and VDD2 regulators can be enabled by setting the DCDC_GLOBAL_CFG[3] SMARTREFLEX_ENABLE bit to 1. To perform VDD1 voltage control through the SmartReflex interface, the device provides the VDD1_SR_CONTROL register. The VDD1_SR_CONTROL MODE bit field can be set to 0 to put VDD1 in an ACTIVE state; setting the field to 1 moves VDD1 to a SLEEP state. VDD1 output voltage can be programmed by setting the VDD1_SR_CONTROL VSEL bit field. VDD1 output voltage is given by VSEL*12.5 mV + 600 mV.

For the details about the VDD2 registers, see Section 6.6, *Register Manual*.

6.4.1.2 VDD2 SMPS Regulator

The VDD2 SMPS is also a stepdown converter with a configurable output voltage of between 0.6 V and 1.45 V. This regulator can power the host processor core. VDD2 differs from VDD1 in its current load capabilities with an output current rating of 600 mA in active mode.

The VDD2 SMPS, like the VDD1 SMPS, provides different voltage regulation schemes. When VDD2 is controlled by the VMODE2 signal or through the SmartReflex interface, the range of output voltage is 0.6 V to 1.45 V. The use of the VMODE2 signal and the VDD2_VMODE_CFG, VDD2_STEP, VDD2_FLOOR, and VDD2_ROOF registers is similar to the use of the corresponding signals and registers for VDD1. VDD2 shares the same SmartReflex I^2C bus to regulate voltage. The VDD2_SR_CONTROL register controls the VDD2 output voltage in SmartReflex mode.

When the VDD2 SMPS is used in software-control mode, the VDD2_DEDICATED[4:0] VSEL bit field can be programmed to provide output voltages of between 0.6 V and 1.45 V. The output voltage for a value of the VSEL field is given by VSEL*12.5 mV + 600 mV. If the VSEL bit field is programmed so that the output voltage computes to more than 1.45 V, the device sets the VDD2 output voltage to 1.5 V.

For details of the VDD2 registers, see Chapter 5, *Resets and Power Management*.

6.4.1.3 VIO SMPS Regulator

The VIO SMPS is a stepdown converter with a choice of two output voltage settings: 1.8 V or 1.85 V. The voltage is set by configuring the VIO_VSEL[0] VSEL bit. When the VSEL bit is set to 0, the output voltage is 1.8 V; when the VSEL bit is set to 1, the output voltage is 1.85 V. When the device resets, the default value of this LDO is 1.80 V; the host processor must write 1 to the VSEL bit to change the output to 1.85 V. The choice of output voltage is based on the platform and transient requirements. This regulator can supply power to the system memories and I/O ports. It is one of the first power supplies to be switched on in the power-up sequence.

VIO does not support the VMODE and SmartReflex voltage control schemes. VIO can be put into sleep or off mode by configuring the SLEEP_STATE and OFF_STATE bit fields of the VIO_REMAP register.

CAUTION

Take care when sequencing the VIO SMPS regulator, because numerous ESD blocks are connected to this supply.

6.4.2 LDO Regulators

Nineteen voltage regulators are integrated in the device to perform linear voltage regulation:

- Device modules receive power from internal LDOs:
  - VUSB3V1
  - VUSB1V5
  - VUSB1V8
  - VINTDIG
  - VINTANA1
  - VINTANA2
  - VRTC
- External peripherals are powered by the remaining LDOs:
  - VDAC
  - VPLL1
  - VMMC1
  - VMIC1
  - VAUX2

Depending on the system requirements and to optimize mean consumption, three operating modes are allowed for each regulator supply:

- Off: The output voltage is not maintained, and the voltage regulator power consumption is null.
- Active: The regulator can deliver its nominal output voltage with full load current capability.
- Sleep: The nominal output voltage is maintained with low power consumption, but also with low`-load current capability. The LDO sleep mode is also referred to as low-power mode.

These states can be modified by writing to the SLEEP_STATE and OFF_STATE bit fields of the <regulator name>_REMAP register where <regulator name> can be any LDO regulator. The SLEEP_STATE bit field indicates the state to be taken by the regulator in case of a system transition from sleep mode to off or active mode. Similarly, the OFF_STATE bit field indicates the state to be taken by the regulator in case of a system transition from OFF state to SLEEP or ACTIVE state. The current state of the resource can be read from the STATE bit field of the <regulator name>_DEV_GRP field, where <regulator name> can be any LDO regulator.

The output voltage of these LDOs can be set by initializing the <regulator name>_DEDICATED VSEL bit field. The default output voltage at power up depends on the boot mode selected.

NOTE: To fulfill the LDO characteristics, a minimum of 250 mV between the LDO input and LDO output voltages is required.

6.4.2.1 VDAC LDO

This programmable LDO is a high-power supply-rejection ratio (PSRR) linear regulator that powers the host processor video digital-to-analog converter (DAC). The VDAC LDO can be configured to provide 1.2 V, 1.3 V, or 1.8 V in on mode, based on the value of the VDAC_DEDICATED[3:0] VSEL bit field. Table 6-3 lists the mapping of the bit field.

Table 6-3. VDAC LDO Output Voltages

VSEL = VDAC_DEDICATED[3:0] (1)	VDAC Output Voltage (V)
xx00	1.2
xx01	1.3
xx10	1.8
xx11	1.8

(1) x − Don't care bit

The default output voltage of the VDAC LDO for Master_C027 boot mode is 1.2 V, which corresponds to a value of 0x0 for the VSEL bit field.

6.4.2.2 VPLL1 LDO

The VPLL1 LDO is a programmable LDO that powers the host processor phase-locked loop (PLL). The VPLL1 LDO can be configured through the I^2C interface to provide output voltage levels of 1.0 V, 1.2 V, 1.3 V, or 1.8 V, based on the value of the VPLL1_DEDICATED[2:0] VSEL bit field. Table 6-4 lists the mapping of the field.

Table 6-4. VPLL1 LDO Output Voltage Scaling

VSEL = VPLL1_DEDICATED[2:0]	VPLL1 Output Voltage (V)
000	1.0
001	1.2
010	1.3
011	1.8

The default output voltage of the VPLL1 LDO for Master_C027 boot mode is 1.3 V, which corresponds to a value of 0x2 for the VSEL bit field.

6.4.2.3 VMMC1 LDO

The VMMC1 LDO is a programmable linear voltage converter that powers a multimedia card (MMC) slot. It includes a discharge resistor and overcurrent protection (short-circuit protection). In addition, it can be turned off when card removal is detected.

GPIO0 can provide an MMC detect function and generate a particular behavior on the device. When card detection is enabled, the device automatically turns off the VMMC1 LDO when a card is removed. Polarity can be chosen, and a debounce period of 0 ms or 30 ms can be selected. For more information about how to use this feature, see Chapter 11, *General-Purpose Inputs/Outputs*.

The VMMC1 LDO can be programmed through the I^2C bus to provide output voltage levels of 1.85 V, 2.85 V, 3.0 V, or 3.15 V in the on mode, based on the value of the VMMC1_DEDICATED[3:0] VSEL bit field. Table 6-5 shows output voltage scaling for the VMMC1 LDO.

Table 6-5. VMMC1 LDO Output Voltage Scaling

VSEL = VMMC1_DEDICATED[3:0]	VMMC1 Output Voltage (V)
xx00	1.85
xx01	2.85
xx10	3.00
xx11	3.15

This LDO can also be used for any supply where the VMMC1 characteristics fulfill the requirements. The default output voltage of VMMC1 for the Master_C027 boot mode is 1.85 V, which corresponds to a value of 0x0 for the VSEL bit field.

6.4.2.4 Audio MIC Bias LDO

The device provides a bias generator to provide an external voltage of 2.2 V. This output can be used to bias an analog microphone (MICBIAS1). The typical output current is 1 mA for the analog microphone bias.

The microphone bias generator can be controlled by programming the MICBIAS_CTL register. For more information about the microphone bias generator and associated programming, see Chapter 13, *Audio*.

6.4.2.5 VAUX2 LDO

VAUX2 is a GP programmable LDO that powers auxiliary devices. The VAUX2_DEDICATED[3:0] VSEL bit field can be programmed through the I^2C interface to provide output voltage of 1.3 V, 1.5 V, 1.7 V, 1.8 V, 1.9 V, 2.0 V, 2.1 V, 2.2 V, 2.3 V, 2.4 V, 2.5 V, or 2.8 V. Table 6-6 shows output voltage scaling for the VAUX2 LDO.

Table 6-6. VAUX2 LDO Output Voltage Scaling

VSEL = VAUX2_DEDICATED[3:0]	VAUX2 Output Voltage (V)
0001	1.70
0010	1.90
0011	1.30
0100	1.50
0101	1.80
0110	2.00
0111	2.50
1000	2.10
1001	2.80
1010	2.20
1011	2.30
1100	2.40

The default output voltage of VAUX2 for the Master_C027S boot mode is 2.8 V, which corresponds to a value of 0x9 for the VSEL bit field.

6.4.2.6 VUSB3V1 LDO

VUSB3V1 is a 3.1-V internal LDO that powers the USB PHY, MCPC, and CEA carkit modules of the USB subchip in the device. By default, the VUSB3V1 LDO is in sleep mode when the device powers up. Before using any of these USB modules, the software must put this LDO in active mode by setting the VUSB_DEDICATED2[3] VUSB3V1_SLEEP bit to 0.

Input to this LDO can be supplied from the VBUS pin or from VBAT, depending on USB use. For the USB PHY to support full-speed USB capability, the minimum output voltage of the VUSBV3P1 LDO must be 3.0 V. This LDO output is possible as long as VBAT is more than 3.1 V. Therefore, the USB subchip can request the monitoring analog-to-digital conversion (MADC) module to perform conversion on VBAT to determine whether it must stay on VBAT supply or switch to VUSB supply in slave mode. It is recommended to use a guard voltage of 150 mV before switching the VUSB3V1 input. Therefore, the software must program the USBREF_ LSB and USBREF_MSB registers of the MADC module to a voltage corresponding to 3.25 V.

For more information about the USBREF_LSB and USBREF_MSB registers, see Chapter 8, *Monitoring ADC*. Switching the LDO input between VBAT and VBUS is performed by programming the correct value in the SW2VBAT and SW2VBUS bits of the VUSB_DEDICATED1 register. Table 6-7 lists the VUSB3V1 LDO input supply used for different combinations of the SW2VBAT and SW2VBUS bits.

Table 6-7. VUSB3V1 LDO Input Switching Register

SW2VBAT = VUSB_DEDICATED1[2]	SW2VBUS = VUSB_DEDICATED1[3]	VUSB3V1 Input Selected
0	0	No input selected
0	1	VBUS
1	0	VBAT
1	1	No input selected

The host processor can configure an interrupt from the MADC.

For more information about the use of this power resource and for device USB use cases, see Chapter 14, *Universal Serial Bus*.

6.4.2.7 VUSB1V5 LDO

VUSB1V5 is a 1.5-V internal LDO that powers the USB subchip in the device.

6.4.2.8 VUSB1V8 LDO

VUSB1V8 is a 1.8-V internal LDO that powers the USB subchip in the device.

6.4.2.9 VINTDIG LDO

VINTDIG is a 1.5-V internal LDO powers the digital sections of the subchips in the device.

6.4.2.10 VRRTC and VBRTC LDOs

The VRTC.OUT output line powers the embedded real-time clock (RTC) (32.768-kHz oscillator) and the power-management digital state-machine in the device. The VRTC.OUT output line is supplied by the VBRTC LDO in low-power consumption modes and by the VRRTC LDO in normal active mode. Therefore, the VRTC.OUT level is present as long as a valid energy source is present (see Figure 6-4).

The VRRTC LDO is powered by VBAT and provides 1.5-V output. By default, the VRRTC LDO is in normal functional mode when the CFG_PWRANA2[6] VRRTC_SLEEP bit is cleared to 0. To reduce power consumption, the VRRTC LDO can be placed in sleep mode by setting the CFG_PWRANA2[6] VRRTC_SLEEP bit to 1.

The VBRTC LDO is supplied from the UPR line. The UPR line is connected to the battery (VBAT) using a clamp circuit.

NOTE: Because the design is based on the TPS65950 device, the UPR line has a switch for connecting it to a backup battery, but the backup battery connection is not available in this device.

6.4.2.11 VINTANA1 LDO

VINTANA1 is a 1.5-V internal LDO that powers the analog sections of the subchips in the device, including the audio, the battery charger interface (BCI), auxiliary, and USB subchips.

6.4.2.12 VINTANA2 LDO

The VINTANA2 LDO can be programmed to provide 2.75 V or 2.5 V to the analog sections of the subchips in the device, including MADC, BCI, and audio.

When the value of the VINTANA2_DEDICATED[3:0] VSEL bit field is 0, the VINTANA2 output voltage is 2.5 V, and when the value of the VSEL bit field is 1, the output voltage is 2.75 V (see Table 6-8). The default output voltage of VINTANA2 is 2.75 V for all boot modes. Table 6-8 shows output voltage scaling for the VINTANA2 LDO.

Table 6-8. VINTANA2 LDO Output Voltage Scaling

VSEL = VINTANA2_DEDICATED[3:0] (1)	VINTANA2 Output Voltage (V)
xxx0	2.50
xxx1	2.75

(1) x − Don't care bit

If the MISC_CFG VINTANA2_SWITCH_MANUAL bit is set to 1, the 2.5-V output setting is automatically selected when the battery voltage falls below 3.0 V. The default value of the VINTANA2_SWITCH_MANUAL bit is 0, which requires the host processor to set the VINTANA2_DEDICATED VSEL bit field to 1 to use the 2.5-V output setting.

6.4.3 USB Charge Pump

When the device acts as an A-device, the USB charge pump provides 4.8 V/100 mA to the VBUS pin. When the device acts as a B-device, the USB charge pump is in high impedance. When VBAT is low, the USB charge pump can feed the VUSB3V1 LDO and let the USB remain functional until VBAT is below 2.7 V.

6.4.4 Short-Circuit Protection

The short-circuit current for the LDOs and DC/DC (SMPS) is twice the maximum load current. When the output of the block is shorted to ground the power, dissipation can exceed the 1.2-W requirement if no action is taken. The short-circuit protection scheme in the device ensures that if the output of an LDO is short-circuited, power dissipation to the ground does not exceed 1.2 W.

All LDOs with at least 100 mA maximum current are included in the short-circuit protection. Based on this assumption, the following regulators require short-circuit protection:

- VDD1
- VDD2
- VIO
- VDAC
- VMMC1
- VAUX2
- VINTANA2
- VUSB1V5
- VUSB1V8
- VUSB3V1

When short-circuit protection is detected on VDD1, VDD2, or VIO, the device is reset to the WaitOn condition. The device can then be switched to ACTIVE state when a starting event is received. When a short circuit is detected on the VDAC, VMMC1, VAUX2, VINTANA2, or VUSB3V1 LDOs, the LDO is put in sleep mode and an interrupt is sent to the host processor. When a short circuit is detected on the VUSB1V5 or VUSB1V8 LDOs, the LDOs are put in off mode and an interrupt is sent to the host processor. Even if the short circuit is detected and removed, the LDO remains in sleep mode. Therefore, the host processor must switch the LDO back to ACTIVE state after short-circuit protection is detected.

The device provides three registers to control and detect short-circuit protection: SC_DETECT1, SC_DETECT2, and SC_CONFIG.

Short-circuit protection is disabled by default at power up. When the SC_CONFIG[7] ENABLE bit is set to 1, short-circuit protection is enabled on 16 LDOs; otherwise, short-circuit protection is disabled.

NOTE: For the VUSB1V5 and VUSB1V8 regulators, because there is no sleep mode, the software must manage the short-circuit event by clearing the interrupt, placing the LDO in question in active mode, and monitoring the status bit.

NOTE: For the VUSB3V1 regulator, if the short circuit is removed, the output voltage rises to the normal value and the software monitoring the immediate status of the LDO detects that the short circuit no longer exists and lets the LDO be programmed to ACTIVE.

NOTE: When the VUSB3V1 regulator is in short circuit, this short circuit is also reported on the VUSB1V5 and VUSB1V8 regulators. When a short circuit is detected on VUSB3V1, the VUSB3V1 regulator is placed in SLEEP and VUSB1V5 and VUSB1V8 are placed in OFF. If the immediate status of the VUSB3V1 regulator, which is monitored by the software, indicates that the short circuit is no longer present, the VUSB1V5 and VUSB1V8 regulators must be reenabled to enable the USB function.

The short-circuit protection scheme should be implemented in manual mode. When the SC_CONFIG[6] MODE bit is set to 0 (automatic mode selected), the device performs automatic short-circuit detection on the power resources that are in ON state. In the automatic short-circuit protection scheme, each of the 16 power providers can be ensured to be checked for short-circuit protection.

For more information about the SC_CONFIG register, see Chapter 5, *Resets and Power Management*.

When short-circuit protection is detected on a power source, the associated bit in the SC_DETECT1 or SC_DETECT2 register is automatically set to 1. For more information about the SC_DETECT1 and SC_DETECT2 registers, see Chapter 5, *Resets and Power Management*.

The device can be programmed to issue an interrupt to the host processor when short-circuit protection is detected on some of the power providers. The SIH of the power subchip can generate an interrupt to the PIH module when short-circuit protection is detected on the following LDOs:

- VINTANA2
- VMMC1
- VMMC2
- VAUX1
- VAUX2
- VAUX3
- VAUX4
- VPLL2
- VDAC
- VUSB1V8
- VUSB1V5
- VUSB3V1

For the SIH to generate this interrupt, the SC_DETECT bit of the PWR_IMR1 or PWR_IMR2 register must be set to 1. The status of this interrupt can be determined by reading the SC_DETECT bit of the PWR_ISR1 or PWR_ISR2 register. For more information about register programming for device interrupts, see Chapter 4, *Interrupts*.

Real-time short-circuit detection can also be performed when the IT_CHECK_CFG[3] SC_STATUS bit is set to 1. In this case, the SC_DETECT1 and SC_DETECT2 registers provide short-circuit detection status in real time. When a short circuit occurs, the following actions must be performed:

1. Clear the IT_CHECK_CFG[3] SC_STATUS bit to 0.
2. Read the SC_DETEC1 and SC_DETECT2 registers to determine which resource generated the short circuit.
3. Set the IT_CHECK_CFG[3] SC_STATUS bit to 1.
4. Remove the cause of the short circuit.
5. Read the SC_DETECT1 and SC_DETECT2 registers to determine whether the short circuit is still present.
6. Clear the IT_CHECK_CFG[3] SC_STATUS bit to 0.
7. Clear the status bits in the SC_DETECT1 and SC_DETECT2 registers by writing 0x00 in these registers to set the resource back to ACTIVE state.

6.5 Programming Model

This section explains how to program various resources.

6.5.1 Voltage Scaling on VDD1

Follow this procedure to enable voltage scaling on VDD1 for power optimization:

1. Initialize the VDD1_VFLOOR[6:0] VFLOOR and VDD1_VROOF[6:0] VROOF bit fields. When the VFLOOR bit field is 0x24, VFLOOR voltage is VFLOOR (in decimals)*12.5 + 600 mV. Therefore, when the VFLOOR bit field is 0x24, the V_{FLOOR} voltage of VDD1 is 1.05 V. Similarly, if the VROOF bit field is set to 0x38, the VROOF voltage of VDD1 is 1.3 V.
2. Enable voltage scaling on VDD1 by setting the VDD1_VMODE_CFG[0] ENABLE_VMODE bit to 1.
   When the VMODE1 signal goes low, VDD1 output voltage decreases toward the VFLOOR voltage. When the VMODE1 signal goes high, VDD1 output voltage increases toward the VROOF voltage.

6.5.2 Setting LDO Output Voltage

To configure the output voltage of the external LDOs, program the <LDO name>_DEDICATED VSEL bit field. To set VAUX2 LDO output voltage to 1.3 V, set the VAUX2_DEDICATED[3:0] VSEL bit field to 0x3.

6.6 Register Manual

For a summary of the device power resource registers and a description of the individual registers see Chapter 5, *Resets and Power Management*.

LED Drivers and PWM Generators

This chapter describes the light-emitting diode (LED) drivers and the two pulse-width modulation (PWM) generators (PWM0 and PWM1) of the device integrated power management/audio coder/decoder (codec) device.

Topic **Page**

7.1 LED Driver and PWM Generators Overview

The device provides light-emitting diode (LED) driver circuitry to power two LED (DC power) circuits that can light a panel or provide user indicators. The two circuits (LEDA and LEDB) are identical except for their current capabilities; LEDA is rated for 160 mA, and LEDB for 60 mA.

The LED driver interfaces are N-channel enhancement mode metal-oxide semiconductor field-effect transistors (MOSFETs) operated in a saturated (nonanalog) regime with LED illumination levels controlled by the pulse-width modulation (PWM) of the MOSFET.

PWM control can be provided two ways:

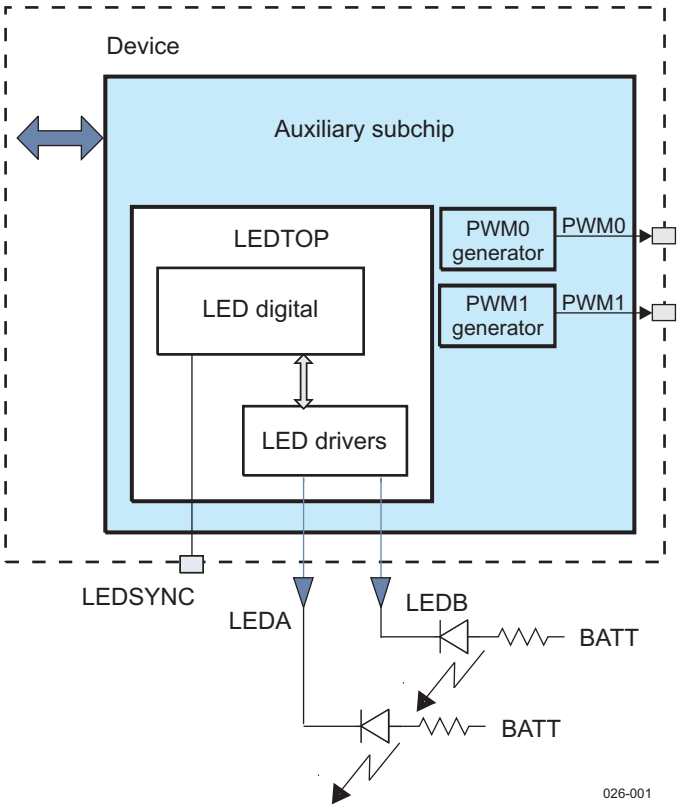
- Mechanisms integral to the LED driver circuitry allow register control of PWM switching times.
- Synchronization of the PWM control can be selected using LEDSYNC.

The device also provides two additional PWM generators (PWM0 and PWM1).

7.2 LED Driver and PWM Generator Environment

The LED driver MOSFETs have a low on resistance and provide no current limiting. As shown in Figure 7-1, resistors must be in-series with the LEDs to limit their current to safe levels.

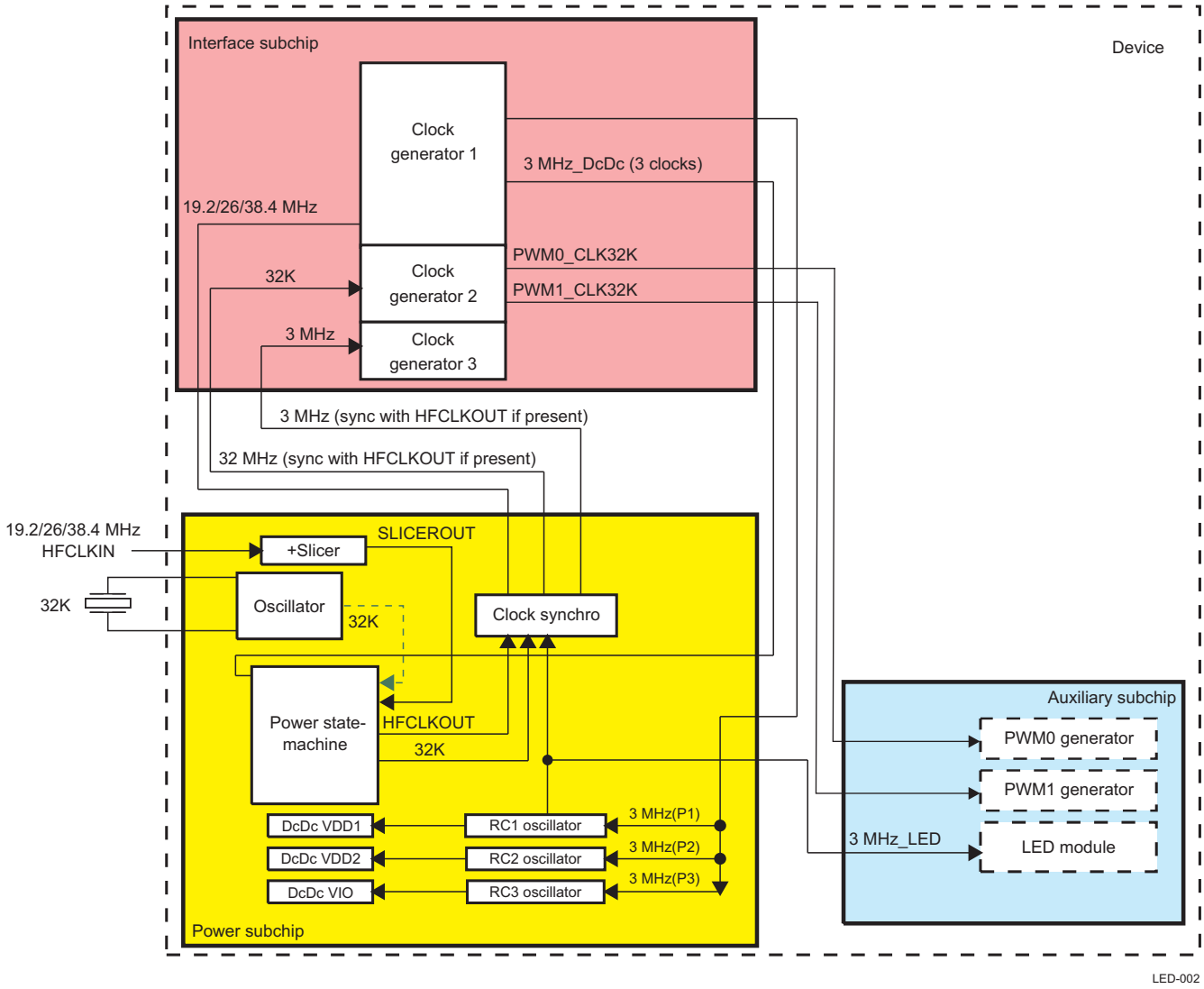
Figure 7-1. Device LED Driver and PWM Generators External Interface



7.3 LED Driver and PWM Generator Integration

The device LED capabilities use the 3-MHz signal provided by the RC1 oscillator. The PWM0 and PWM1 generators use the 32-kHz clock provided by clock generator 2 (see Figure 7-2). For more information, see Chapter 3, *Clocks*.

Figure 7-2. LED Driver and PWM Generator Integration

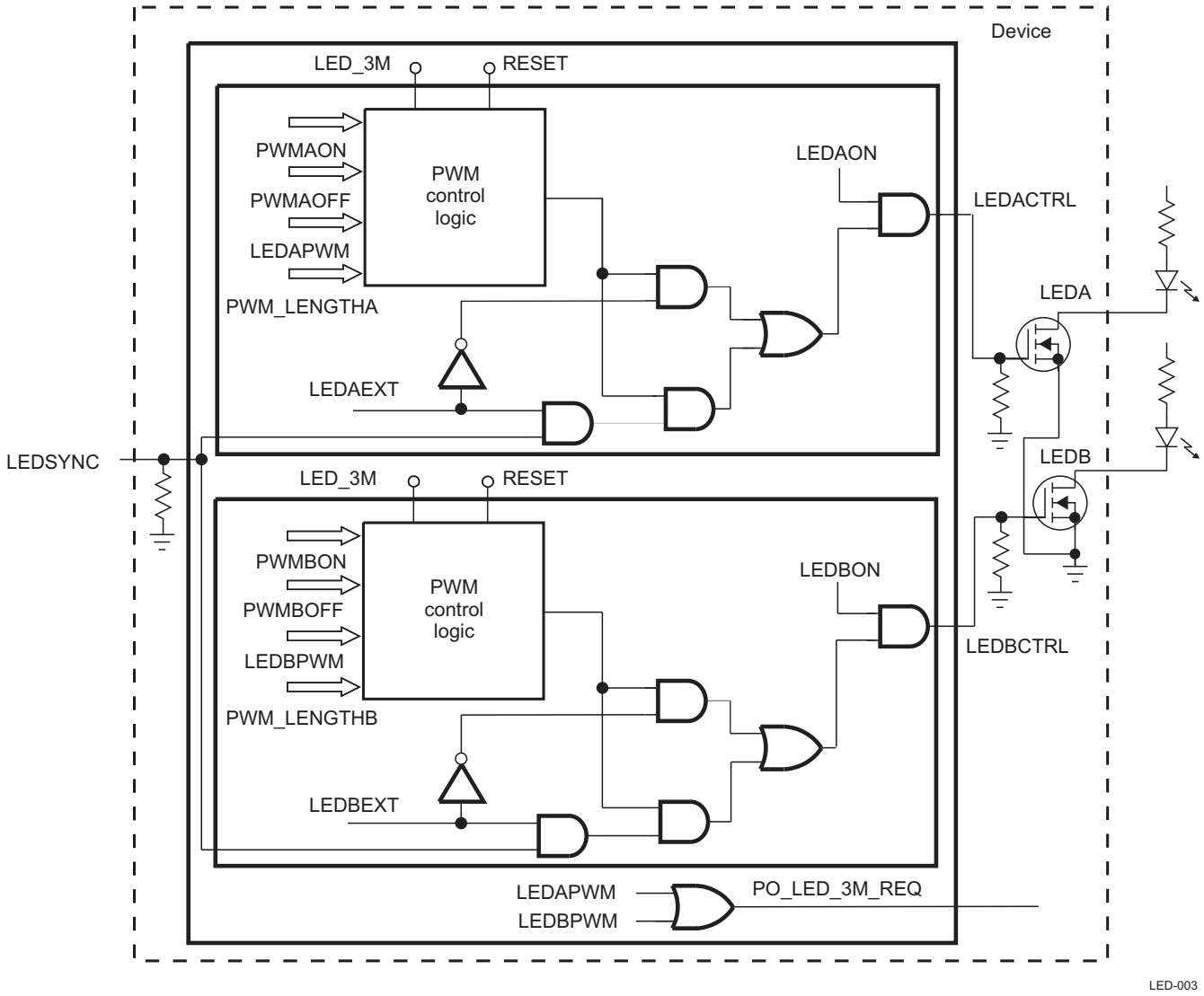


7.4 LED Driver and PWM Generators Functional Description

7.4.1 LED Driver Functional Description

The device LED circuitry consists of two identical PWM generators and the capability of synchronizing the output of the MOSFETs using the LEDSYNC input. Figure 7-3 is an overview of the PWM and the control logic.

Figure 7-3. Device LED PWM and Control Logic



7.4.1.1 Operation

The LED circuits are controlled by registers in the device. These circuits operate identically, except for the current each can supply (160 mA for LEDA; 60 mA for LEDB).

The PWM generators can be turned on or off by using the PWM ON and PWM OFF registers for the A and B LED circuits:

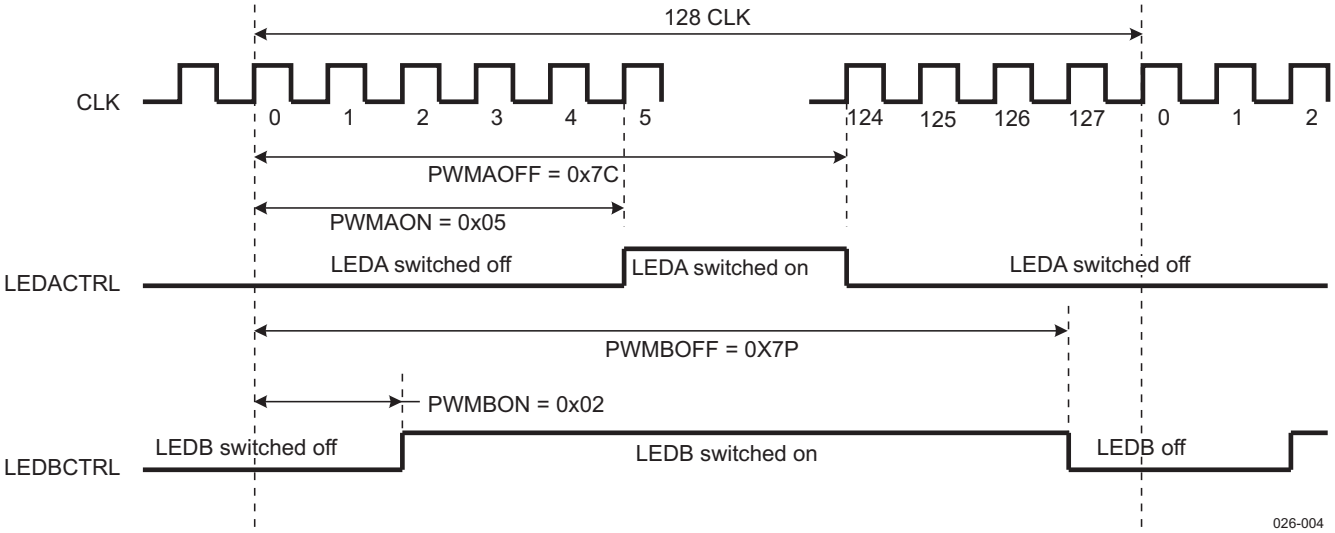
- PWMAON (see Section 7.4.1.2.2, *PWMAON*)
- PWMAOFF (see Section 7.4.1.2.3, *PWMAOFF*)
- PWMBON (see Section 7.4.1.2.4, *PWMBON*)
- PWMBOFF (see Section 7.4.1.2.5, *PWMBOFF*)

The LEDAON and LEDBON bits can also inhibit the PWM output.

When the PWM generators are on, the duty cycle of the LEDs can be changed; this provides variable levels of LED illumination.

The PWM generators operate through the use of registers working with counters driven by a 3-MHz clock; control signals are generated when the counter values match the register values. Figure 7-4 is an overview of the timings with a 128-clock cycle setting.

Figure 7-4. LED Driver PWM Timings With 128-Clock Cycle Setting



NOTE: The following discussion is from the standpoint of a single LED circuit; it is equally true for A and B LED circuits.

The counter starts at 0 and continues to its maximum value. When the counter reaches its maximum value, it resets and starts a new count cycle. The registers associated with the counter are PWM ON, PWM OFF, and PWM LENGTH.

The LED current is turned on when the counter reaches the value set in the PWM ON register.

The LED current is turned off when the counter reaches the value set in the PWM OFF register.

This operation sets one of the constraints: The PWM OFF register value cannot be less than the PWM ON register value (the LED current must be turned on before it can be turned off). The PWM ON and PWM OFF registers can be set to the same value to keep the drive to the LED circuitry continuously on (100 percent).

Another constraint of the design is that the PWM ON register cannot be set to 0.

PWM ON and PWM OFF register values can be changed while the counter is operating. If the counter does not reach a new setting in a register during the count cycle, it executes when it reaches the new value. If a register setting is changed after the counter passes the new value during the count cycle, the effect of the new value is delayed until the next count cycle.

The default counter length is 128 clock cycles, but it can be changed to 64 clock cycles) using the PWM LENGTH register.

It is possible to change the counter length while the counter is running.

If the counter length is changed from 64 to 128, the counter continues until it reaches 128, resets, and then continues to operate with a length of 128 clock cycles.

If the counter length changes from 128 to 64, there are two possible outcomes. If the counter is below 64 when the change occurs, it continues to 64 and resets with succeeding counting periods 64 clock cycles long. If the counter is 64 or higher when the counter length changes, it immediately resets and starts over with a length of 64 clock cycles.

The length of time that the LED current flows during each count cycle is the difference between the PWM ON and PWM OFF register values multiplied by the length of each count (roughly 330 ns per clock cycle of the 3-MHz clock).

The duty cycle of the LEDs is the ratio of the length of time the LED current flows divided by the total time in a complete count cycle (128 or 64 counts at the 3-MHz clock rate; 42.7 μs or 21.2 μs, respectively), multiplied by 100.

Example:

Using the 128-clock cycle default counter length:

Use PWMON register value = 20.

Use PWMOFF register value = 92.

The LED current is turned on 20 clock cycles (3-MHz clock) into the counting period (after 6.67 μs).

The LED current is turned off 92 clock cycles (3-MHz clock) into the counting period (after 30.67 μs).

Therefore, the LED current is on for (30.67 μs − 6.67 μs) = 24 μs

With a counting interval (128 clock cycles) of 42.67 μs

Result is a duty cycle of (24/42.67) x 100 = 56.25%

In addition to direct PWM control of the LED outputs, an external (hardware) control pin (LEDSYNC) can be activated by using two additional control pins, LEDxEXT (where x is A or B for the two LED circuits), which allows synchronizing of the LED circuits with control signals from the host processors.

When LEDxEXT is grounded, LEDSYNC is not active, and the output of the PWM directly controls the LED current. If LEDxEXT is pulled to logical 1, an external signal on LEDSYNC is mixed in an AND gate with the output of the PWM. There is LED current only when the output of the PWM and LEDSYNC are both logical 1. In this situation, PWM output is blocked from controlling the LED current if the signal on LEDSYNC is a logical 0.

7.4.1.2 LED Control Function Registers

7.4.1.2.1 LEDEN

Enable LEDA Output

Bits	Bit Name	Description	Type	Reset
0	LEDAON	LEDA enable. Set to logical 1.	RW	0

Enable LEDB Output

Bits	Bit Name	Description	Type	Reset
1	LEDBON	LEDB enable. Set to logical 1.	RW	0

Enable External Control of LEDA

Bits	Bit Name	Description	Type	Reset
2	LEDAEXT	Control for LEDA. Set to logical 1.	RW	0

Enable External Control of LEDB

Bits	Bit Name	Description	Type	Reset
3	LEDBEXT	Control for LEDB. Set to logical 1.	RW	0

Enable PWM for LEDA

Bits	Bit Name	Description	Type	Reset
4	LEDAPWM	Enables PWM for LEDA. Set to logical 1.	RW	0

Enable PWM for LEDB

Bits	Bit Name	Description	Type	Reset
5	LEDBPWM	Enables PWM for LEDB. Set to logical 1.	RW	0

Select 64 Clock Cycles for PWM A Period

Bits	Bit Name	Description	Type	Reset
6	PWM_LENGTHA	Default is logic 0 (128 bits); set to logical 1 for 64 bits	R	0

Select 64 Clock Cycles for PWM B Period

Bits	Bit Name	Description	Type	Reset
7	PWM_LENGTHB	Default is logic 0 (128 bits); set to logical 1 for 64 bits	R	0

7.4.1.2.2 PWMAON

Select PWMA ON Clock Cycles

Bits	Bit Name	Description	Type	Reset
7	INT_PWM_ LENGTHA	Allows selection of the number of clock cycles used in the PWMA period: 128 (default value: bit set at 0) or 64 (bit set at 1)	RW	0
6	PWMAON6	DATA6 − Set to configure the desired count.	RW	0
5	PWMAON5	DATA5 − Set to configure the desired count.	RW	0
4	PWMAON4	DATA4 − Set to configure the desired count.	RW	0
3	PWMAON3	DATA3 − Set to configure the desired count.	RW	0
2	PWMAON2	DATA2 − Set to configure the desired count.	RW	0
1	PWMAON1	DATA1 − Set to configure the desired count.	RW	0
0	PWMAON0	DATA0 − Set to configure the desired count.	RW	0

7.4.1.2.3 PWMAOFF

Select PWMA OFF Clock Cycles

Bits	Bit Name	Description	Type	Reset
7	Reserved	Not used	R	0
6	PWMAOFF6	DATA6 − Set to configure the desired count.	RW	0
5	PWMAOFF5	DATA5 − Set to configure the desired count.	RW	0
4	PWMAOFF4	DATA4 − Set to configure the desired count.	RW	0
3	PWMAOFF3	DATA3 − Set to configure the desired count.	RW	0
2	PWMAOFF2	DATA2 − Set to configure the desired count.	RW	0
1	PWMAOFF1	DATA1 − Set to configure the desired count.	RW	0
0	PWMAOFF0	DATA0 − Set to configure the desired count.	RW	0

7.4.1.2.4 PWMBON

Select PWMB ON Clock Cycles

Bits	Bit Name	Description	Type	Reset
7	INT_PWM_ LENGTHB	Allows the selection of the number of clock cycles used in the PWMB period: 128 (default value: bit set at 0) or 64 (bit set at 1)	RW	0
6	PWMBON6	DATA6 − Set to configure the desired count.	RW	0
5	PWMBON5	DATA5 − Set to configure the desired count.	RW	0
4	PWMBON4	DATA4 − Set to configure the desired count.	RW	0
3	PWMBON3	DATA3 − Set to configure the desired count.	RW	0
2	PWMBON2	DATA2 − Set to configure the desired count.	RW	0
1	PWMBON1	DATA1 − Set to configure the desired count.	RW	0
0	PWMBON0	DATA0 − Set to configure the desired count.	RW	0

7.4.1.2.5 PWMBOFF

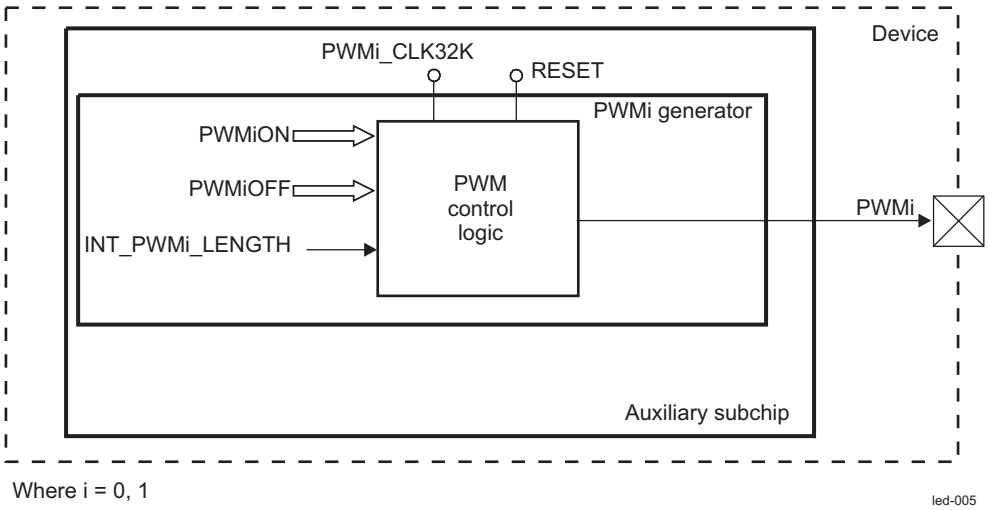
Select PWMB OFF Clock Cycles

Bits	Bit Name	Description	Type	Reset
7	Reserved		RW	0
6	PWMBOFF6	DATA6 − Set to configure the desired count.	RW	0
5	PWMBOFF5	DATA5 − Set to configure the desired count.	RW	0
4	PWMBOFF4	DATA4 − Set to configure the desired count.	RW	0
3	PWMBOFF3	DATA3 − Set to configure the desired count.	RW	0
2	PWMBOFF2	DATA2 − Set to configure the desired count.	RW	0
1	PWMBOFF1	DATA1 − Set to configure the desired count.	RW	0
0	PWMBOFF0	DATA0 − Set to configure the desired count.	RW	0

7.4.2 PWM0 and PWM1 Generators Functional Description

This section describes the function of the digital PWM generators (PWM0 and PWM1). Figure 7-5 is a block diagram of the PWM generators.

Figure 7-5. Device PWM1 and PWM0 Generators Block Diagram



The generators are controlled by registers and operate identically. Each PWM generator is clocked by a 32-kHz clock (PWM0_CLK32K for PWM0, and PWM1_CLK32K for PWM1).

NOTE:

- The PWM0_CLK32K clock is received by the PWM0 generator only when the GPBR1[0] PWM0_CLK_ENABLE bit is set to 1.
- The PWM1_CLK32K clock is received by the PWM1 generator only when the GPBR1[1] PWM1_CLK_ENABLE bit is set to 1.

To save power when the PWMi generator is not used (where i = 0, 1), the clock must be disabled by clearing the corresponding bit in the GPBR1 register.

7.4.2.1 PWM Period Setting

The PWMi period is controlled by the PWMiON[7] INT_PWM_LENGTHi bit (where i = 0, 1):

- Cleared to 0: The PWMi period is 128 cycles of the PWMi_CLK32K clock. The clock-cycles counter counts from 0 to 127. The PWMi frequency is 32.768 kHz/128 = 256 Hz.
- Set to 1: The PWMi period is 64 cycles of the PWMi_CLK32K clock. The clock-cycles counter counts from 0 to 63. The PWMi frequency is 32.768 kHz/64 = 512 Hz.

NOTE:

- If the PWMi period was programmed on 64 clock cycles and is changed to get 128 clock cycles, the clock-cycles counter counts to 127, and then it is cleared to 0. The next PWMi periods will be 128 clock cycles.
- If the PWMi period was programmed on 128 clock cycles and is changed to get 64 clock cycles, and if the clock-cycles counter value is less than 64, the clock-cycles counter counts to 63, and then it is cleared to 0. The next PWMi periods will be 64 clock cycles.
- If the PWMi period was programmed on 128 clock cycles and is changed to get 64 clock cycles, and if the clock-cycles counter value is greater than or equal to 64, the clock-cycles counter is cleared to 0 (PWMi period is aborted). The next PWMi periods will be 64 clock cycles.

7.4.2.2 PWM ON and OFF Positions Setting

The PWMi ON and OFF positions are determined by the PWMiON[6:0] and PWMiOFF[6:0] bit fields, respectively, either in a range of 0 to 127 when the PWMiON[7] INT_PWM_LENGTHi bit is cleared to 0, or in a range of 0 to 63 when the PWMiON[7] INT_PWM_LENGTHi bit is set to 1.

NOTE: The following conditions are prohibited:

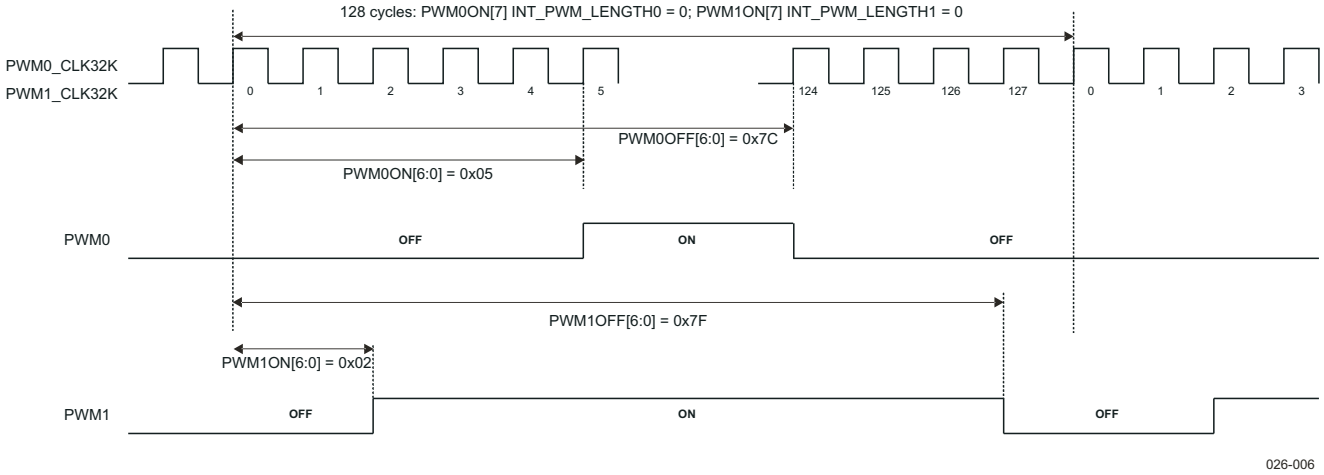
- PWMiON[6:0] bit field greater than the PWMiOFF[6:0] bit field (where i = 0, 1)
- Setting the PWMiON[6:0] bit field to 0x00

NOTE: The PWMi output is constantly on when the value of the PWMiON[6:0] bit field equals the value of the PWMiOFF[6:0] bit field.

Figure 7-6 shows PWM timings for the PWM0 and PWM1 generators with the following settings:

- PWM0 and PWM1 period set to 128 clock cycles: PWM0ON[7] INT_PWM_LENGTH0 and PWM1ON[7] INT_PWM_LENGTH1 bits are cleared to 0.
- PWM0 ON position (PWM0ON[6:0] bit field) is set to 0x05.
- PWM0 OFF position (PWM0OFF[6:0] bit field) is set to 0x7C (124).
- PWM1 ON position (PWM0ON[6:0] bit field) is set to 0x02.
- PWM1 OFF position (PWM0OFF[6:0] bit field) is set to 0x7F (127).

Figure 7-6. PWM Timings



The output of PWM0 is enabled when the GPBR1[2] PWM0_ENABLE bit is set to 1. The output of PWM1 is enabled when the GPBR1[3] PWM1_ENABLE bit is set to 1.

NOTE:

- The output of PWM0 is connected to the external ball GPIO6 only when the PMBR1[3:2] GPIO6_PWM0_MUTE bit field is set to 0x1.
- The output of PWM1 is connected to the external ball GPIO7 only when the PMBR1[5:4] GPIO7_VIBRASYNC_PWM1 bit field is set to 0x3.

7.5 LED Driver Programming Model

Example:

Turn on LEDA, PWM control, no external control, 128 clock cycles (default), and 50 percent duty cycle.

Comments:

The device internal registers are accessed through the device inter-integrated circuit (I²C™) buses. (For more information, see Chapter 2, *Control Interface*. For LED application, use the general-purpose (GP) I²C bus. Do not use the SmartReflex™ I²C bus.)

1. Disable the H-bridge: Set the VIBRA_CTL[0] VIBRA_EN bit to 0.
2. Enable LEDA: Set the LEDEN[0] LEDAON bit to logical 1.
3. Enable PWM for LEDA: Set the LEDEN[4] LEDAPWM bit to logical 1.
4. Do not enable LEDA external control: Leave the LEDEN[2] LEDAEXT bit as logic 0.
5. Do not change the default clock cycles: Leave the LEDEN[6] PWM_LENGTHA bit unchanged.
6. Select the PWMAON clock cycles: Activate PWMAON halfway through the counting interval by setting to 63 (dec).
7. Select the PWMAOFF clock cycles: Delay PWMAOFF until the end of the counting period by setting to 127 (dec).

NOTE: Activating PWMAON halfway through the count and inhibiting PWMAOFF until the end of the count provides the desired 50 percent duty cycle.

NOTE: Do not enable the LEDA/B and the H-vibrator simultaneously.

7.6 LED Driver and PWM Generator Register Manual

This section describes the device registers for the LED operation.

7.6.1 Register Access

The device internal registers are accessed through the device I²C buses. (For more information, see Chapter 2, *Control Interface*. For LED applications, use the GP I²C bus. Do not use the SmartReflex I²C bus.)

7.6.2 LED Register

Table 7-1 summarizes the LED register. Table 7-2 describes the individual register bits.

Table 7-1. LED Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
LEDEN	RW	8	0x0000 00EE

Table 7-2. LEDEN

Address Offset	0x00		
Physical Address	0x0000 00EE	**Instance**	LEDLED
Description	Controls LED operating modes		
Type	RW		

7	6	5	4	3	2	1	0
PWM_LENGTHB	PWM_LENGTHA	LEDBPWM	LEDAPWM	LEDBEXT	LEDAEXT	LEDBON	LEDAON

Bits	Field Name	Description	Type	Reset
7	PWM_LENGTHB	Choose 64- or 128-clock cycles in PWM B period.	RW	0
6	PWM_LENGTHA	Choose 64- or 128-clock cycles in PWM A period.	RW	0
5	LEDBPWM	Enable PWM for LEDB.	RW	0
4	LEDAPWM	Enable PWM for LEDA.	RW	0
3	LEDBEXT	LEDSYNC pin has control if this bit is set to 1.	RW	0
2	LEDAEXT	LEDSYNC pin has control if this bit is set to 1.	RW	0
1	LEDBON	LEDB enable	RW	0
0	LEDAON	LEDA enable	RW	0

7.6.3 PWMA Registers

Table 7-3 lists the PWMA registers. Table 7-4 and Table 7-5 describe the individual registers in the PWMA module instance in the device.

Table 7-3. PWMA Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
PWMAON	RW	8	0x0000 00EF
PWMAOFF	RW	8	0x0000 00F0

Table 7-4. PWMAON

Address Offset	0x00		
Physical Address	0x0000 00EF	**Instance**	LEDPWMA
Description	Determines the number of periods until LEDA is on and allows selection of the number of clock cycles used in the PWMA period: 128 (default value: bit set at 0) or 64 (bit set at 1).		
Type	RW		

7	6	5	4	3	2	1	0
INT_PWM_LENGTHA	PWMAON6	PWMAON5	PWMAON4	PWMAON3	PWMAON2	PWMAON1	PWMAON0

Bits	Field Name	Description	Type	Reset
7	INT_PWM_LENGTHA	Allows selection of the number of clock cycles used in the PWMA period: 128 (default value: bit set at 0) or 64 (bit set at 1)	RW	0
6	PWMAON6	DATA6	RW	0
5	PWMAON5	DATA5	RW	0
4	PWMAON4	DATA4	RW	0
3	PWMAON3	DATA3	RW	0

Bits	Field Name	Description	Type	Reset
2	PWMAON2	DATA2	RW	0
1	PWMAON1	DATA1	RW	0
0	PWMAON0	DATA0	RW	0

Table 7-5. PWMAOFF

Address Offset	0x01		
Physical Address	0x0000 00F0	**Instance**	LEDPWMA
Description	Determines the number of periods until LEDA turns off		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	PWMAOFF6	PWMAOFF5	PWMAOFF4	PWMAOFF3	PWMAOFF2	PWMAOFF1	PWMAOFF0

Bits	Field Name	Description	Type	Reset
7	Reserved	Not used	R	0
6	PWMAOFF6	DATA6	RW	0
5	PWMAOFF5	DATA5	RW	0
4	PWMAOFF4	DATA4	RW	0
3	PWMAOFF3	DATA3	RW	0
2	PWMAOFF2	DATA2	RW	0
1	PWMAOFF1	DATA1	RW	0
0	PWMAOFF0	DATA0	RW	0

7.6.4 PWMB Registers

Table 7-6 lists the PWMA registers. Table 7-7 and Table 7-8 describe the individual registers in the PWMA module instance in the device.

Table 7-6. PWMB Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
PWMBON	RW	8	0x0000 00F1
PWMBOFF	RW	8	0x0000 00F2

Table 7-7. PWMBON

Address Offset	0x00		
Physical Address	0x0000 00F1	**Instance**	LEDPWMB
Description	Determines the number of periods until LEDB is on and allows selection of the number of clock cycles used in the PWMB period: 128 (default value: bit set to 0) or 64 (bit set to 1).		
Type	RW		

7	6	5	4	3	2	1	0
INT_PWM_LENGTHB	PWMBON6	PWMBON5	PWMBON4	PWMBON3	PWMBON2	PWMBON1	PWMBON0

Bits	Field Name	Description	Type	Reset
7	INT_PWM_ LENGTHB	Allows selection of the number of clock cycles used in the PWMB period: 128 (default value: bit set to 0) or 64 (bit to 1)	RW	0
6	PWMBON6	DATA6	RW	0
5	PWMBON5	DATA5	RW	0
4	PWMBON4	DATA4	RW	0
3	PWMBON3	DATA3	RW	0
2	PWMBON2	DATA2	RW	0
1	PWMBON1	DATA1	RW	0
0	PWMBON0	DATA0	RW	0

Table 7-8. PWMBOFF

Address Offset	0x01		
Physical Address	0x0000 00F2	**Instance**	LEDPWMB
Description	Determines the number of periods until LEDB turns off		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	PWMBOFF6	PWMBOFF5	PWMBOFF4	PWMBOFF3	PWMBOFF2	PWMBOFF1	PWMBOFF0

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	PWMBOFF6	DATA6	RW	0
5	PWMBOFF5	DATA5	RW	0
4	PWMBOFF4	DATA4	RW	0
3	PWMBOFF3	DATA3	RW	0
2	PWMBOFF2	DATA2	RW	0
1	PWMBOFF1	DATA1	RW	0
0	PWMBOFF0	DATA0	RW	0

7.6.5 PWM0 Registers

See Section 2.6.1.2.3, *PWM0*.

7.6.6 PWM1 Registers

See Section 2.6.1.2.4, *PWM1*.

Monitoring ADC

This chapter describes the monitoring analog-to-digital converter (MADC) of the device integrated power management/audio coder/decoder (codec) device.

The TPS65930 and TPS65920 devices are variants of the TPS65950. The TPS65950 has functions that are not available in the TPS65930 and TPS65920 because of their reduced package pin count. Internally (in the silicon), the TPS65930 and TPS65920 are almost identical to the TPS65950 and as a result they share the same register structure and mechanisms.

This chapter, on the MADC function, may contain descriptions of features that are not available in the TPS65930 and TPS65920 but the text is included because an understanding of that feature may be needed to understand features that are available in the TPS65930 and TPS65920 devices.

Topic **Page**

8.1 Monitoring ADC Overview

The MADC is a module in the auxiliary subchip of the device that lets the host processors monitor analog signals (such as temperature) using analog-to-digital conversion (ADC) on the input source. After the conversion is complete, the host processor reads the results of the conversion through the inter-integrated circuit (I^2C™) interface. The MADC also performs analog signal conversion for the universal serial bus (USB) subchip. The device MADC has the following features:

- Single 10-bit ADC with successive approximation register (SAR) conversion
- Analog multiplexer with access to 2 inputs (ADCIN0 to ADCIN2)
- MADC resource shared by multiusers, including system host processors and the internal USB subchip of the device
- Four ways of starting ADC on ADC input channels
- Quarter-bit accuracy for modem-initiated real-time (RT) conversion requests
- Management of potential concurrent conversion requests and priority between different resource users
- Interrupt signal to the primary interrupt handler (PIH) at the end-of-sequence of conversions
- Averaging feature to sample the input channel on four consecutive conversion cycles instead of one time, and to provide the average value of four conversions
- Selective enabling or disabling of the averaging feature on individual channels before conversion sequence

Because the MADC is shared by users, there are four ways to start the ACD. Three of these requests can be triggered by external host processors, and two requests are issued by the device internal modules:

- Hardware or RT conversion request: This request is initiated by the external host processor to request RT signal conversion. This conversion request is most useful when tied to a modem processor request for temperature conversions in synchronization with a signal frame boundary. The host processor can use this request to request conversion on the ADC input channels.
- SW1 software conversion request: This request can be initiated by the first external host processor to request non-RT conversions. This request is also called an asynchronous or general-purpose conversion (GPC) request.
- SW2 software conversion request: This request can be initiated by the second external host processor to request non-RT conversions. This request is also called an asynchronous or GPC request.
- USB conversion request: This is a GPC request triggered by the USB subchip through the device internal signals. This conversion request is for the ADCIN12 channel.

Table 8-1 shows the MADC channel assignment.

Table 8-1. MADC Channel Assignment

Monitoring ADC Channel Name	Type of Input	Use
ADCIN0	External	Battery type (BTYPE)
ADCIN2	External	GP analog input

In this chapter, ADCINx refers to the channel name of the MADC,, and adcinx refers to the external pin that feeds this signal.

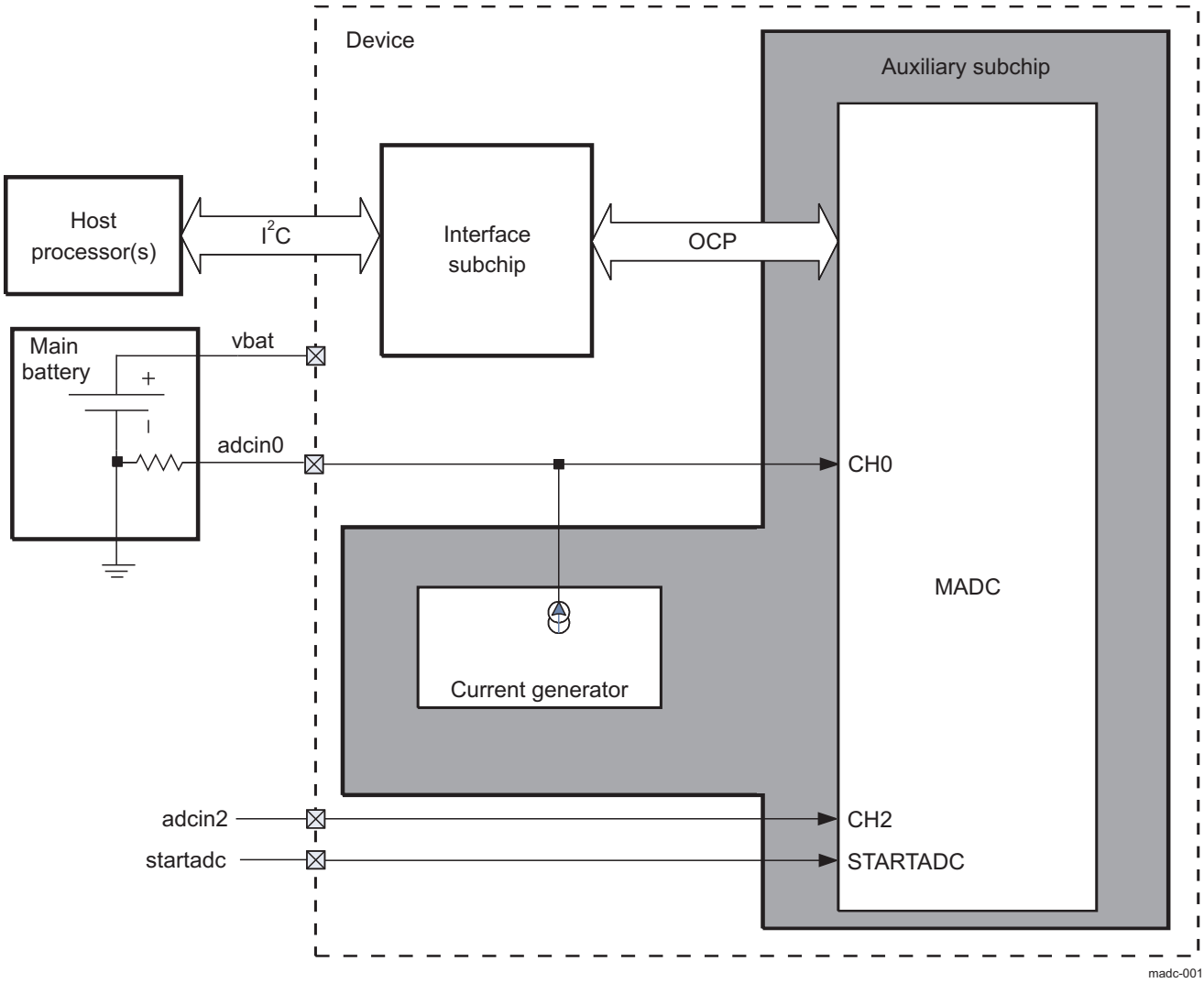
NOTE:

- If VINTANA2 is off, no current above 1 mA through an input channel ADCINx (where x = 0 to 7) should be sourced in Triton2. If current source is higher, VINTANA2 must be put in sleep mode.
- If VINTANA2 and VUSB3V1 are OFF, no current above 1 mA through an input channel ADCINx (where x = 0 to 7) should be sourced in Triton2. If current source is higher, VINTANA2 and VUSB3V1 must be put in sleep mode.

8.2 MADC Environment

This section describes the device MADC and its interaction with components external to the device. Figure 8-1 shows the interaction of the MADC with external devices.

Figure 8-1. MADC Environment



The MADC allows 11 input channels for conversion. Of these, two are external analog input channels (ADCIN0 and ADCIN2). These are external channels because a user can trigger measurements by externally connecting GP signals to the device external pins adcin0 and adcin2.

The input signal on the adcin0 pin is connected by default to the current source in the BCI subchip. This current source can be configured to provide a known bias current to the adcin0 pin. It is possible to use the adcin0 pin as a GP input channel by disabling the BCI current source to this channel. The TYPEN and ITHEN bits of the BCICTL1 register enable or disable the current source for the adcin0 pin. Therefore, by setting the TYPEN bit to 0, it is possible to disable the current source of adcin0 and use this channel as a GP channel.

The ADCIN2 channel is available by default for measuring GP analog signals. The input voltage range on adcin0 is 0.0 V to 1.5 V, and the input range on adcin2 is 0.0 V to 2.5 V. ADCIN2 is first fed through a multiplexer, and then through a common prescaler that scales the range of input signal voltage for these channels from 0.0 to 1.5 V. For more information about interpreting conversion results for MADC input channels, see Section 8.4.7, *Interpretation of MADC Result Registers*.

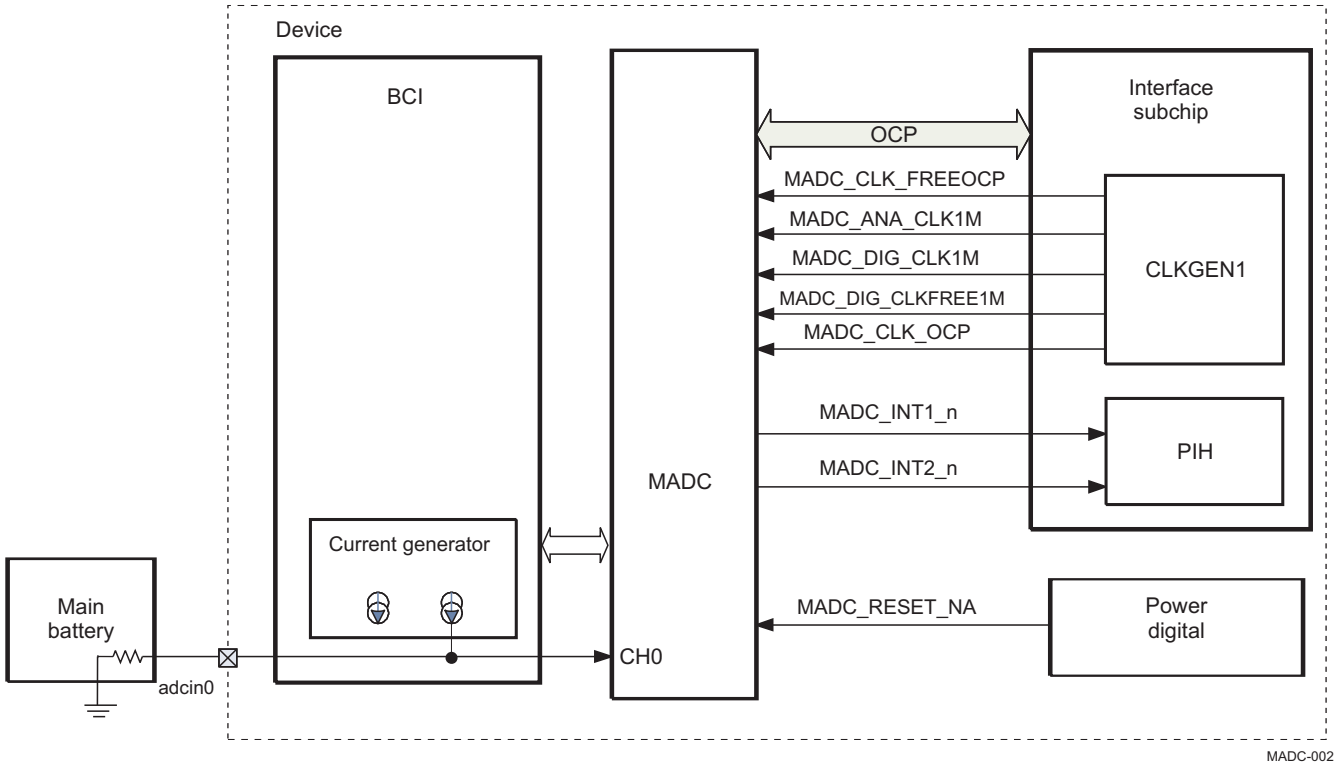
To trigger RT conversion of the input channels, the host processor can toggle the signal on the startadc pin. It is also possible to select the edge of the incoming startadc signal to trigger conversion, as explained in Section 8.4.3.1, *Hardware Conversion Request (startadc)*.

8.3 Monitoring ADC Integration

This section describes MADC integration with other modules in the device.

Figure 8-2 shows the MADC interfaces to the power subchip, PIH, BCI, control interface, and the USB subchips.

Figure 8-2. MADC Integration in the Device



8.3.1 MADC Clocks

The MADC receives five clocks from the CLKGEN1 module of the interface subchip:

- MADC_CLK_FREEOCP: Sampling clock for the startadc signal, MADC power-on requests, and channel conversion requests from the BCI and the USB subchip. This clock is always available afer the system comes up.
- MADC_ANA_CLK1M: Used by the MADC analog section
- MADC_ DIG_CLKFREE1M: Used by the MADC secondary interrupt handler (SIH) block
- MADC_DIG_CLK1M: Used by the rest of the MADC digital logic, including the state-machines in the digital section
- MADC_CLK_OCP: Accesses registers in the MADC

The MADC analog and digital functional clocks are controlled by the CFG_BOOT[1:0] HFCLK_FREQ bit field in the power subchip and the GPBR1 DEFAULT_MADC_CLK_EN bit in the interface subchip. The host processor must program the HFCLK_FREQ bit field based on the frequency of the HFCLK input. When the device powers up, the MADC functional clocks are provided by default for a 26-MHz high-frequency clock (the division factor is 26). If the input high-frequency clock is not 26 MHz, the correct programming steps must be followed when changing the HFCLK_FREQ and DEFAULT_MADC_CLK_EN bits fields.

8.3.2 MADC Resets

The MADC receives the MADC_RESET_NA from the device power subchip. This is the master reset from the device power-management state-machine, which resets the logic and registers in the MADC digital section. It also resets the MADC analog section.

The MADC cannot be reset by software, but it can be put into POWER-OFF state three ways:

- By writing 0 to the CTRL1[0] MADCON bit
- By an internal signal from the BCI
- By the USB subchip

If the MADC is in the process of conversion, it completes all pending conversion sequences before switching to POWER-OFF state

8.3.3 The MADC and the USB Interface

Like the BCI, the USB subchip can use an internal signal to power on the MADC. The USB subchip can then request the MADC to measure VBAT to determine whether to use the VBAT or VRUSB supply in the slave mode. First, the USB subchip sends an internal signal to power on the MADC. This is followed by MACD requests based on a timer in the USB subchip. The USB conversion request can generate interrupts on the PIH at end-of-conversion (EOC) and the results of the conversion are stored in GP registers (GPCH12_MSB and GPCH12_LSB) accessible by a host processor through the I^2C interface. For more information about the USB conversion request, see Section 8.4.3.3, *USB Conversion Request*.

8.3.4 The MADC and the PIH Interface

When the channel conversion sequence completes, the SIH block of the MADC can generate two synchronous interrupts sent to the PIH: MADC_INT1_n and MADC_INT2_n. The PIH can then send these interrupts to host processors. For more information about SIH registers, see Section 8.4.4, *MADC Interrupts*. More information about the SIH and the PIH can be found in Chapter 4, *Interrupts*.

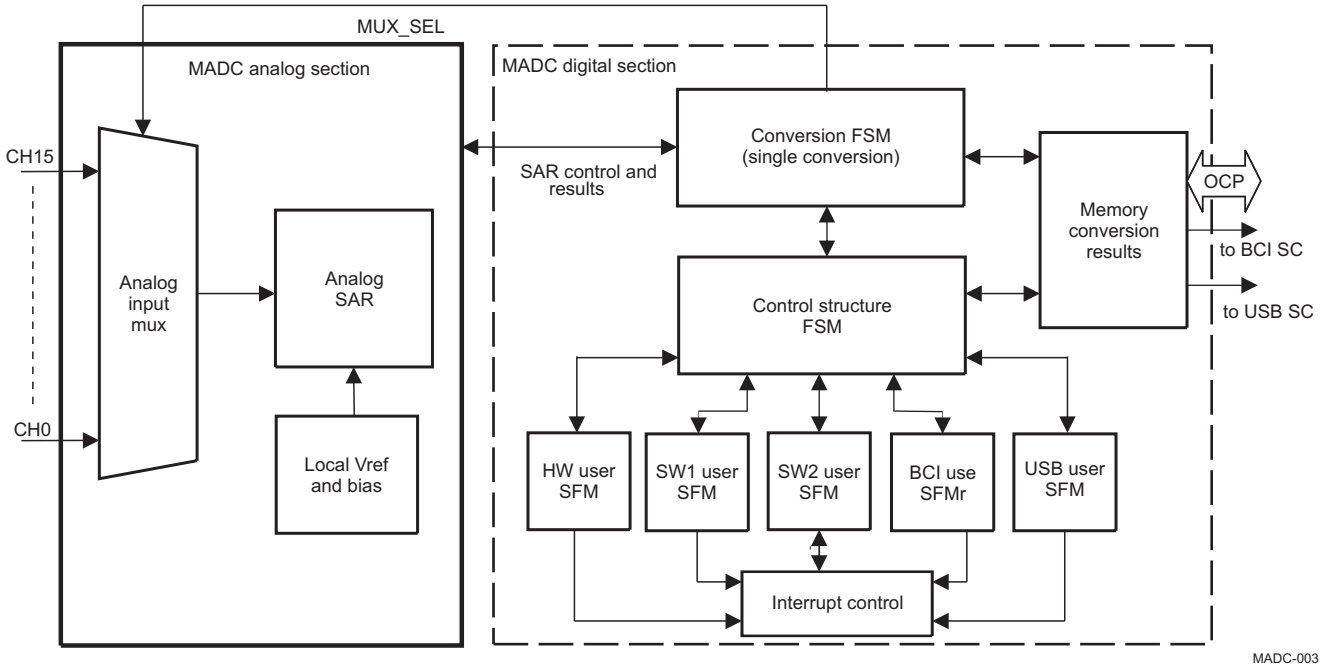
8.4 Monitoring ADC Functional Description

This section describes the MADC and provides process of requesting conversion from different resource users.

8.4.1 MADC Analog and Digital Parts

The MADC consists of analog and digital sections, shown in Figure 8-3.

Figure 8-3. MADC Analog and Digital Sections



The MADC analog section selects input channels based on information from the MADC digital section. The analog SAR block then performs ADC using a successive approximation scheme.

The MADC digital section controls each conversion sequence; manages the result of averaging; and manages the interrupt signals and the priority arbitration among RT, GP, and USB subchip conversion requests. It also contains control registers and conversion result registers that are accessible to the host processor through the I^2C interface.

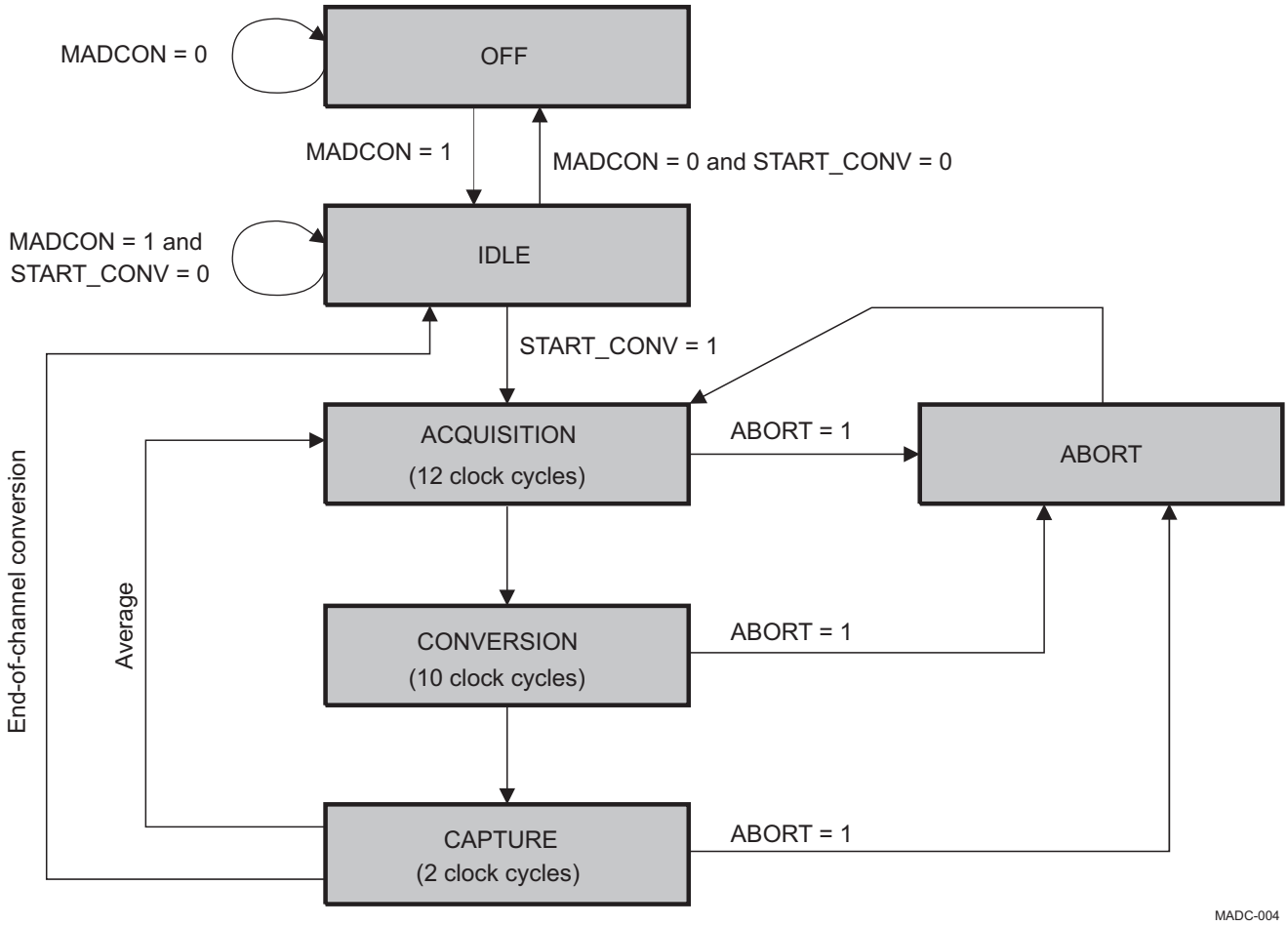
The MADC digital section consists of two types of state-machines and a control structure, as explained in Section 8.4.2, *MADC State-Machines and Control Structure*.

8.4.2 MADC State-Machines and Control Structure

8.4.2.1 MADC Conversion State-Machine

Figure 8-4 shows the MACD state-machine clocked on the MADC_DIG_CLK1M clock from the CLKGEN1 module of the interface subchip.

Figure 8-4. MADC Conversion State-Machine



The conversion state-machine monitors the conversion sequence for a single channel. This state-machine interacts and controls the MADC analog section. The MACD state-machine has various states:

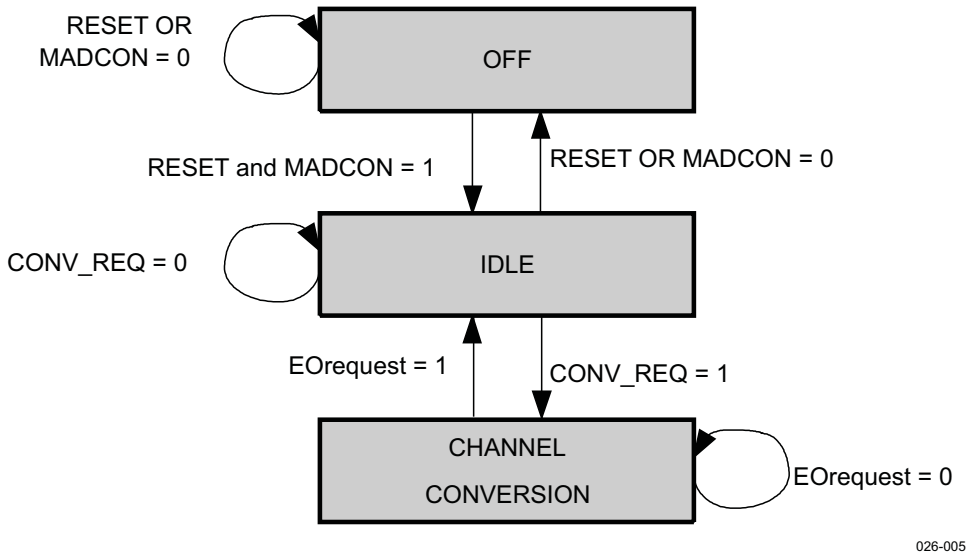
- OFF: MADC is in this state when the device is in RESET state, or when the MADC has not received a power-on request from resource users that request a conversion. The transition from OFF state occurs when the MADC is out of reset and a user sends a request to power on the MADC.
- IDLE: In this state, the MADC control state-machine is waiting for a conversion request. The device is out of reset and at least one user has requested the MADC to power on (the CTRL1[0] MADCON bit is set to 1), an internal MADCON signal is received from the BCI, or the USB subchip is asserted).
- ACQUISITION: The control state-machine launches a START_CONV signal to the MADC analog section after a conversion request of one channel is received. In this state, the MADC analog section multiplexes the analog input and loads the value to convert to the sampling capacitance. A BUSY signal is sent to the control state-machine to indicate that a conversion is running.
- CONVERSION: During this phase, the analog SAR block of the MADC analog section performs the ADC. The ADC result varies.
- CAPTURE: During this state, the MADC digital section stores the analog-to-digital conversion result in the corresponding result register. At the end of the state, the conversion is complete, the following state is IDLE, and the BUSY signal is released.

- ABORT: During an asynchronous conversion sequence (SW1, SW2, BCI, or the USB), if the control state-machine detects an RT conversion request from the startadc pin, the ABORT signal is set to 1, and the conversion state-machine goes to ABORT state. In this state, the digital section resets all the analog sections to begin a new conversion sequence correctly.

8.4.2.2 MADC Resource User State-Machine

The MADC user state-machine is duplicated for the five resource users: HW, SW1, SW2, BCI, and the USB. There are five user state-machines in the digital section of the MADC. A user state-machine memorizes the user's conversion sequence request, monitors the conversion, and indicates when the corresponding request is ended. The EOC request signal is used in the interrupt control block, or in the BCI and the USB interface, to indicate the end of the conversion request. Figure 8-5 shows the MADC resource user state-machine maintained in the MADC digital section.

Figure 8-5. MADC Resource User State-Machine



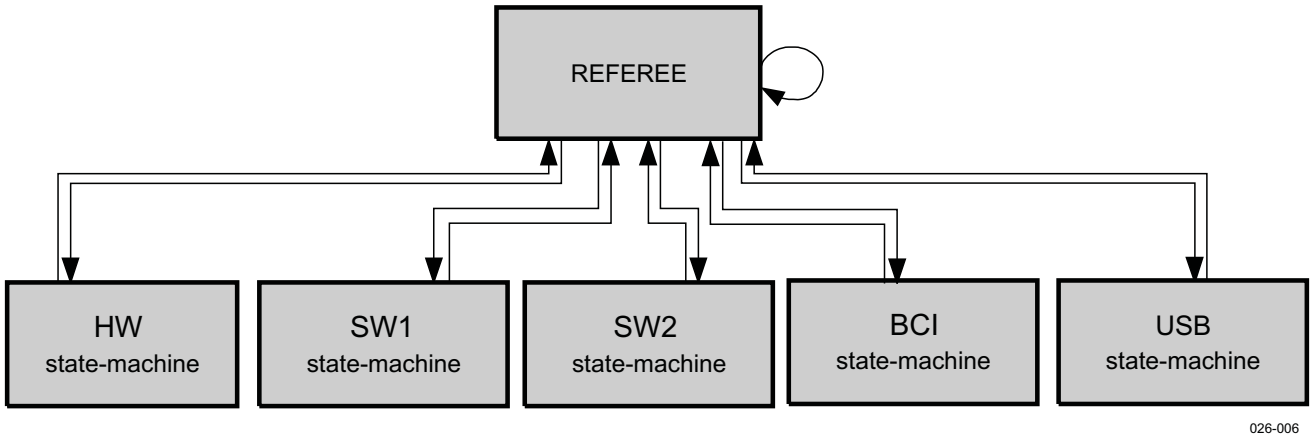
The user state-machine has three states:

- OFF: The device is in reset mode, or the MADC is not powered on.
- IDLE: The MADC moves from OFF state to IDLE state when the MADC receives a power-on signal from the BCI, the USB subchip receives a power-on signal through an internal signal, or a host processor writes 1 to the CTRL1[0] MADCON bit. In this state, the MADC waits for a conversion request from any requester.
- CHANNEL CONVERSION: The user state-machine enters this state when a conversion request is received from the corresponding user. The MADC control state-machine processes the channel conversion request. The user state-machine stays in this state until the MADC control state structure sends the EOC request signal.

8.4.2.3 MADC Control Structure

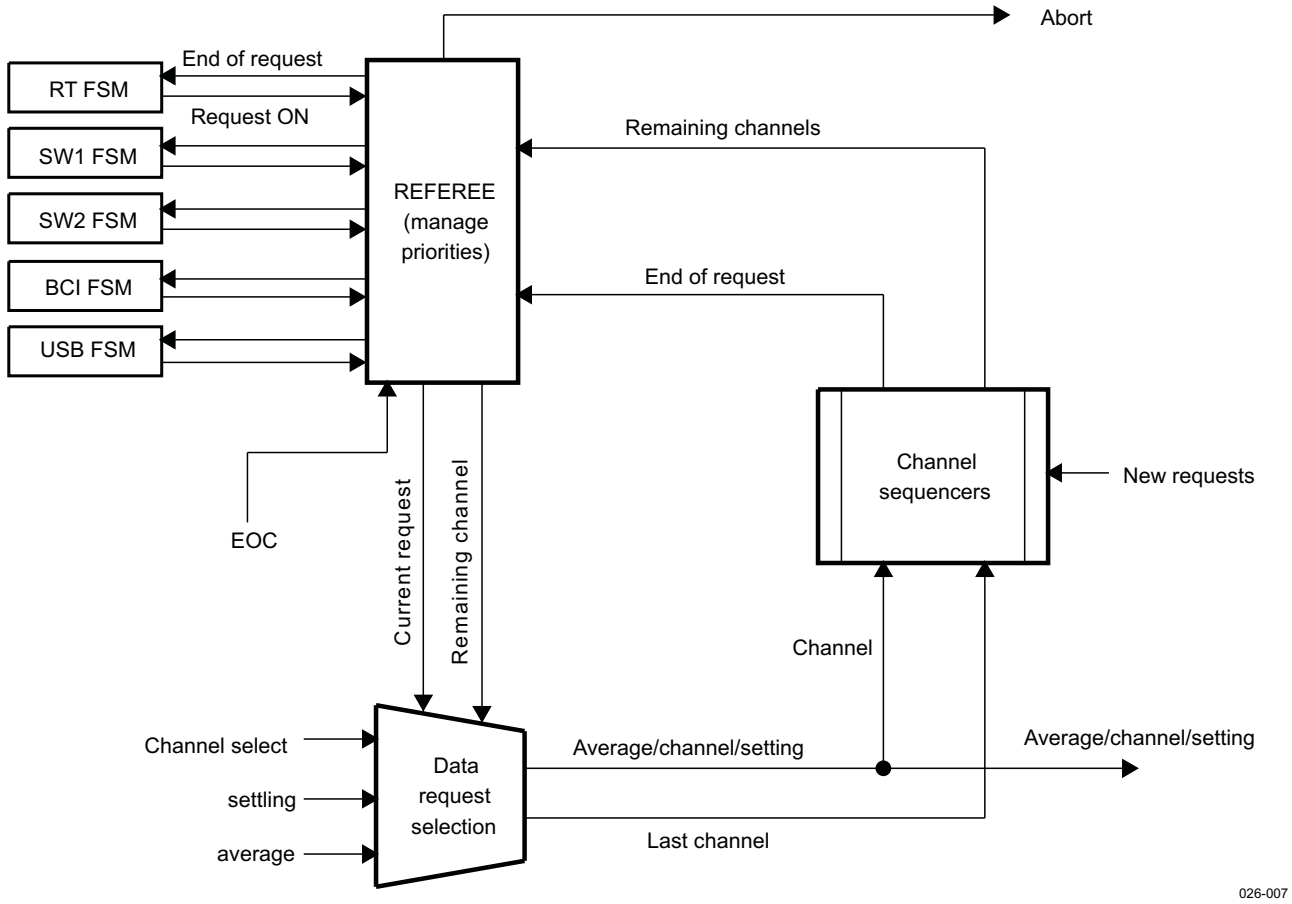
The MADC control structure is dedicated to conversion initiation, averaging, and priority handling among RT conversion (hardware), asynchronous conversions (SW1 and SW2), the BCI, and USB subchip conversion requests. The MADC control structure includes a referee subblock that helps perform these tasks. Figure 8-6 shows the MADC control structure clocked on a 1-MHz clock. Figure 8-7 shows details of the referee subblock.

Figure 8-6. MADC Control Structure State-Machine



The user state-machines shown in Figure 8-6 are the same as those shown in Figure 8-5. Figure 8-7 shows more details of the MADC referee subblock.

Figure 8-7. MADC REFEREE



The referee subblock receives all the requests from the user state-machines and the EOC information from the conversion state-machine. It determines the current request and, depending on the priority, manages the abort signal. It also manages revolving conversion requests when priorities are equal. For information about conversion priority and concurrent request handling, see Section 8.4.5, *Conversion Priority and Concurrent Request Handling*.

There is one channel request signal and one channel sequencer per user state-machine. Each channel sequencer determines the remaining channels to be converted for each requesting user. Each new conversion request forces the corresponding channel sequencer to reset the remaining channel list.

The data request selection unit receives the information about the current request and the remaining channels associated with it, and determines which channel is to be converted next. Then it collects the conversion sequence information relative to the next channel to be converted.

8.4.3 MADC Conversion Process

The MADC allows five methods of requesting signal conversion:

- Hardware-triggered external conversion request through the startadc pin
- Software-triggered external conversion request using SW1
- Software-triggered external conversion request using SW2
- BCI-triggered internal conversion request
- USB-triggered internal conversion request

The conversion requests from the BCI and the USB subchip are through internal signals not available outside the device.

8.4.3.1 Hardware Conversion Request (startadc)

To monitor battery voltage under heavy current sink requires starting the conversion in a well-defined position with respect to the transmitting burst. Because these measurements are time-critical, a hardware (real-time [RT]) conversion request is used, because this method of conversion has the highest priority. RT conversion can be triggered by a host processor through the external dedicated pin, startadc.

The host processor powers on the MADC by setting the CTRL1[0] MADCON bit to 1. The host processor then selects the channels for RT conversion by programming the RTSELECT_LSB and RTSELECT_MSB registers. When a bit in the RTSELECT_LSB or RTSELECT_MSB register is set to 1, the corresponding channel is selected for conversion.

The MADC embeds an averaging feature programmable by software. To enable averaging measurements on a particular channel, the corresponding bit of the RTAVERAGE_LSB or RTAVERAGE_MSB register must be set to 1. During the averaging measurement, the MADC performs measurements on four consecutive conversion cycles, then writes the average of these measurements in the result register. When averaging is not enabled, the sampled signal value is written to the result register after a single conversion cycle.

The MADC RT conversion is activated when the startadc signal is asserted. The polarity of startadc can be programmed with the CTRL2[0] STARTADCRF bit. When the STARTADCRF bit is 1, the rising edge of startadc activates a MACD, and when the STARTADCRF bit is 0, the falling edge activates conversion. The edge-detection mechanism is based on sampling the startadc signal on a free-running clock (MADC_CLK_FREEOCP) provided to the MADC when the CTRL1[0] MADCON bit is set to 1. When a valid startadc signal transition is detected, the digital control module of MADC fetches the RT selection registers RTSELECT_LSB and RTSELECT_MSB to determine which channels are to be sampled and converted. A conversion sequence processes all queued selected channels, starting with ADCIN15 and ending with ADCIN0, depending on the channels selected.

When an RT conversion sequence is running, the CTRL_SW1[2] EOC_RT or CTRL_SW2[2] EOC_RT bit is set to 0. At the end of each individual conversion, the MADC writes the conversion result into the corresponding RTCHx_LSB and RTCHx_MSB results register. At the end of the entire conversion sequence, the EOC_RT bit is set to 1 and a signal is sent to the MADC SIH. Based on the interrupt mask register configuration of SIH, an interrupt can be generated and sent to the PIH. For information about the MADC SIH and PIH interfaces, see Chapter 4, *Interrupts*.

8.4.3.2 Software Conversion Request (SW1/SW2)

SW1 and SW2 are the two ways of starting the GP conversion. These are meant for systems in which two processors, typically an application processor and a modem processor, request MACDs. The procedure follows:

1. Before starting a GP conversion, the host processor powers on the MADC by setting the CTRL1[0] MADCON bit to 1.
2. The host processor selects the channels for conversion by setting the corresponding bits of the SW1SELECT_LSB and SW1SELECT_MSB registers to 1.
3. The host processor also enables averaging on the selected channel by setting the corresponding bits of the SW1AVERAGE_LSB and SW1AVERAGE_MSB registers to 1.
4. The host processor then requests the start of the conversion by setting the CTRL_SW1[5] SW1 bit to 1.
5. Depending on the priority of the pending conversion requests, the MADC starts converting the individual channels from ADCIN15 to ADCIN0, based on the channel selection register. (While conversion is in progress, the CTRL_SW1 EOC_SW1 bit is set to 0.)
6. After the end of each channel conversion, the results are written into the corresponding GPCHx_LSB and GPCHx_MSB registers (where x is the channel number).
7. When the selected channel conversion sequence completes, the CTL_SW1 EOC_SW1 bit is automatically set to 1.
8. If the MADC_IMR1 SW1_IMR1 bit is set to 0, at the end of the conversion sequence, the MADC SIH sends a MADC_INT1_n signal to the PIH. The PIH sends the interrupt (INT1) to the host processor.

The second host processor can follow similar steps using the following registers:

- SW2SELECT_LSB
- SW2SELECT_MSB
- SW2AVERAGE_LSB
- SW2AVERAGE_MSB
- CTRL_SW2
- MADC_IMR2

At the end of the conversion sequence, an interrupt can be generated on the INT2 pin of the device. The results of conversion are available in the GPxCH_LSB and GPxCH_MSB registers.

8.4.3.3 USB Conversion Request

The USB PHY module of the USB subchip depends on the USBV3V1 internal LDO supply. This LDO can take VBAT or VBUS as input (VBAT is the default). For the USB PHY to support full-speed USB capability, the minimum output voltage of the USBV3V1 LDO must be 3.0 V. This LDO output is possible as long as VBAT is more than 3.1 V. Therefore, the USB subchip can request the MADC to perform conversion on VBAT connected to ADCIN12 to determine whether it must stay on VBAT supply, or should switch to VUSB supply in the slave mode.

As shown in Figure 8-2, the VBAT is an input to the MADC through a prescaler in the BCI. Therefore, the host processor must enable this prescaler before the USB subchip starts requesting conversion on this channel. The VBAT prescaler in the BCI can be enabled by setting the BCICTL1[1] MESBAT bit to 1.

Conversion requests are managed in the USB subchip using an internal timer. The conversion request is a GP type. The USB subchip sends an internal MADCON signal, followed by a request for conversion on the VBAT. The EOC_USB bit of the CTRL_SW1 and CTRL_SW2 registers shows the status of this conversion sequence. When the conversion requested by the USB subchip completes, the value of the EOC_USB bit is 1.

At the end of the conversion sequence, the MADC compares the conversion result to a reference value. This 10-bit reference value can be programmed in the USBREF_LSB and USBREF_MSB registers. The recommended reference value programmed in these registers is 3.25 V, which allows 150-mV guard voltage. The default value of the USBREF_MSB[7:0] BIT_9DT2 bit field is 0x8C. The default value of the USBREF_LSB[7:6] BIT_1DT0 bit field is 0x3. The combined 10-bit default value of the USB reference voltage is 563(= 0x233), which corresponds to a voltage level of 3.30 V. By setting USBREF_MSB to 0x8A and USBREF_LSB to 0xC0, the host processor can modify the default values of these registers so that the 10-bit reference values equal 3.25 V. For the steps required to perform MACD on VBAT and inform the host processor when the VBAT level crosses 3.25 V, see Section 8.5.2, *VBAT Monitoring by the USB Subchip*.

One of two interrupt modes is possible:

- When the CTRL2[1] USB_INT_MODE bit is cleared to 0, the comparison result indicates that the conversion result is less than the reference value. An interrupt is sent at each request.
- When the CTRL2[1] USB_INT_MODE bit is set to 1, an interrupt is sent every time the conversion value goes higher or lower than the reference value.

Regardless of the value of the CTRL2[1] USB_INT_MODE bit, the interrupt is sent to the PIH only if the MADC_IMR1[3] USB_IMR1 bit or the MADC_IMR2[3] USB_IMR2 bit is cleared to 0.

The status of this interrupt can be detected by reading the MADC_ISR1[3] USB_ISR1 bit or the MADC_ISR2[3] USB_ISR2 bit.

Because these status bits are shared with the VBAT monitoring feature status bits, the CTRL_SW1[6] USBREF_STS bit indicates whether the interrupt was generated by the USB conversion request (1: Interrupt generated by the USB conversion request; 0: Interrupt not generated by the USB conversion request).

When the host processor detects this interrupt, it switches the input source of the USBV3P1 LDO to the VBUS supply by setting the VUSB_DEDICATED1[2] SW2VBAT bit to 0 and the VUSB_DEDICATED1[3] SW2VBUS bit. For more information about the VUSB_DEDICATED1 register, see Chapter 6, *Power Resources*.

NOTE: When the MADC_IMR1[3] USB_IMR1 or the MADC_IMR2[3] USB_IMR2 bit is set to 0, the host processor continues interrupts, as long as the VBAT level remains less than the reference voltage set in USBREF_MSB and USBREF_LSB, in the case where the CTRL2[1] USB_INT_MODE bit is cleared to 0.

The USB subchip conversion request has the same level of priority as the SW1, SW2, and BCI requests. The conversion result is also stored in the corresponding GP result registers, GPCH12_MSB and GPCH12_LSB.

Averaging is enabled by setting the BCI_ USBAVERAGE[5] AV_USB_CH0 bit to 1. The behavior of averaging is exactly the same as averaging for a hardware conversion request (see Section 8.4.3.1, *Hardware Conversion Request (startadc)*).

8.4.3.4 VBAT Monitoring

Using the description of the USB conversion request in Section 8.4.3.3, a second reference value composed of the CTRL2[7:3] VBATREF_MSB and CTRL1[7:3] VBATREF_LSB bit fields, not dedicated to USB, can be programmed to generate an interrupt when this reference is crossed (exceeds or is less than the reference value) by a USB conversion request measurement. This feature works only when the CTRL2[1] USB_INT_MODE bit is set to 1.

As for the USB conversion request, the interrupt is sent when the MADC_IMR1[3] USB_IMR1 or MADC_IMR2[3] USB_IMR2 bit is set to 0.

The status of this interrupt can be detected by reading the MADC_ISR1[3] USB_ISR1 or MADC_ISR2[3] USB_ISR2 bit.

Because these status bits are shared with the USB conversion request status bits, the CTRL_SW1[7] VBATREF_STS bit indicates whether the interrupt was generated by the VBAT monitoring feature (1: Interrupt generated by the VBAT monitoring feature; 0: Interrupt not generated by the VBAT monitoring feature).

Averaging is enabled by setting the BCI_USBAVERAGE[5] AV_USB_CH0 bit to 1. The behavior of averaging is exactly the same as averaging for a hardware conversion request (see Section 8.4.3.1, *Hardware Conversion Request (startadc)*).

8.4.4 MADC Interrupts

Two identical interrupt generation modules in the MADC SIH process synchronous interrupt requests independently in a biprocessor environment. Each module generates an interrupt, MADC_INT1_n and MADC_INT2_n. Each module controls its own synchronous interrupt request line and has its own interrupt mask register (IMR) and interrupt status register (ISR). For information about the SIH, see Chapter 4, *Interrupts*.

The IMRs, MADC_IMR1 and MADC_IMR2, let each processor enable/disable the expected MADC interrupts, MADC_INT1_n and MADC_INT2_n, respectively, when the MACD sequence completes. When a bit in the MADC_IMRx register is set to 1, the corresponding EOC sequence does not generate a signal MADC_INTx_n to the MADC SIH. For the host processor to generate an interrupt on INTx, the corresponding bit of the MADC_IMRx register must be set to 0.

For each MADC event, in the interrupt edge-detection registers, MADC_EDR1 and MADC_EDR2, the user defines the edge expected to trigger an interrupt request. Detection can be on the rising edge, falling edge, or both edges.

The interrupt status registers, MADC_ISR1 and MADC_ISR2, indicate the current status of the interrupt signals, MADC_INT1_n and MADC_INT2_n, respectively. They are read/write registers. If the corresponding bit of the MADC_IMRx register is set to 0, the register is updated when a conversion sequence completes. Each interrupt is cleared by default (the value of the MADC_SIH_CTRL[2] COR bit is 1) by reading the MADC_ISRx register. When the MADC_SIH_CTRL[2] COR bit is set to 0, the interrupt is cleared by setting the corresponding bit of the MADC_ISRx register to 1. Setting the MADC_ISRx register to 0 has no effect.

The MADC SIH register MADC_SIH_CTRL lets the user enable an incoming pending event during software interrupt latency by setting the MADC_SIH_CTRL[1] PENDDIS bit to 0. Writing 1 in the PENDDIS bit disables the pending feature. Exclusivity can be enabled by setting the MADC_SIH_CTRL[0] EXCLEN bit to 1 and disabled by setting the EXCLEN bit to 0. For more information about interrupt registers and the interface between the MADC SIH and the PIH, see Chapter 4, *Interrupts*.

8.4.5 Conversion Priority and Concurrent Request Handling

MACD requests from users are asynchronous with respect to each other; therefore, the MADC must handle priorities among resource users. The MADC does not handle parallel conversions; it works on a single-conversion sequence. Within a conversion sequence, the channels are converted one after the other from ADCIN15 to ADCIN0, depending on the channels selected.

If a resource user requests conversion on more than one channel, and if during the conversion sequence it is aborted (because of priority, as described later in this section), the conversion of only the current channel is aborted and the MADC remembers this aborted channel. When the MADC is available again, the aborted conversion sequence restarts, starting from the channel that was aborted, and continues with the remaining channels.

An RT conversion initiated by a pulse on startadc has the highest priority. When a startadc pulse occurs, the current running conversion (if there is one) aborts and the RT conversion executes. All channels requested by an RT conversion request are processed one after the other. When the RT conversion sequence completes, the previous conversion (if one was aborted) restarts from the same channel where it was aborted, and then continues with the remaining channels.

The remaining four conversion modes (SW1, SW2, BCI, and USB) have equal priority. If a conversion request from any of these requesters is received, no ongoing conversion request through any of these users is aborted. Because the conversions are handled on a channel-by-channel basis, there is a revolving priority among the four mode. After completing a SW1-requested channel conversion, the MADC checks to ensure that there is no other pending channel conversion request from the remaining requesters. If there is a pending channel conversion request, the next converted channel is SW2, BCI, or the USB channels.

If conversions are averaged, the four conversions needed for the average function are executed consecutively, and the average is stored in the result register. Therefore, the averaging conversion is not affected by the revolving priority. For example, if the MADC is converting a channel with averaging requested by SW1, it completes all four conversions before checking for any pending conversion requests from other users (SW2, USB, or BCI). When an RT conversion request occurs during an averaging conversion, the averaging conversion aborts and the RT conversion starts. When the RT conversion sequence completes, the averaging conversion restarts from the beginning (the four conversions are recomputed). Figure 8-8 shows all these points.

Figure 8-8. MADC Conversion Priority

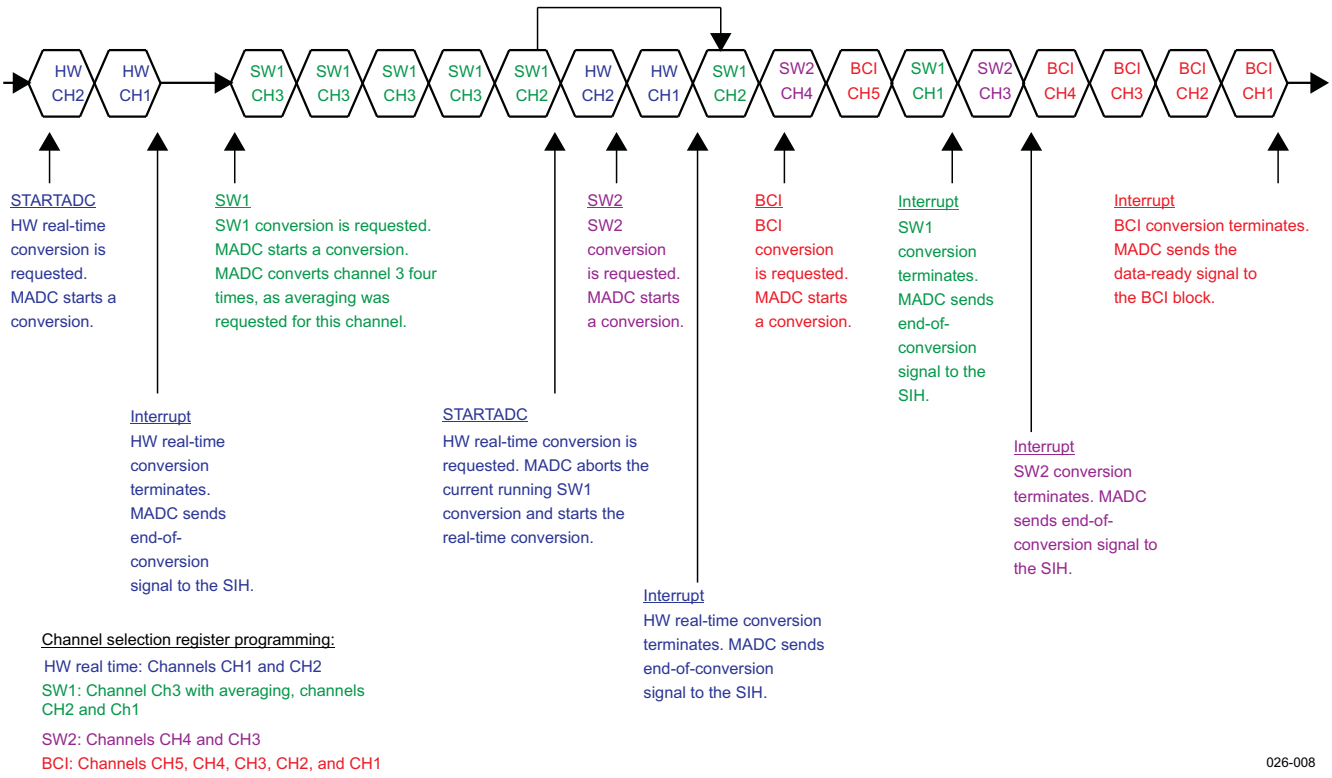


Figure 8-8 shows the following:

- An RT conversion request for two channels, CH1 and CH2, is received when the MADC is available (no current conversion is running).
- A SW1 conversion request is received when the MADC is available. The SW1 channels requested for conversion are CH1, CH2, and CH3 with averaging enabled for CH3. SW1 CH3 conversion starts and repeats for four consecutive conversion cycles to accomplish averaging. The conversion average is stored in the corresponding GPCH3_LSB and GPCH3_MSB registers. After the MADC starts the CH2 conversion, a request for RT conversion is received. Therefore, SW1 CH2 conversion aborts and RT conversion is processed.
- During the RT conversion, a SW2 conversion request is detected for CH3 and CH4 conversion. Because the SW1 CH2 conversion was aborted, it completes first after the RT conversion ends. Based on the revolving priority of SW1−SW2−BCI−USB, after the SW1 CH2 conversion completes, the SW2 CH4 conversion, not the SW1 CH1 conversion, starts.
- During the SW2 CH2 conversion, a BCI conversion request is received for CH1, CH2, CH3, CH4, and CH5. After a SW2 CH2 conversion completes, the BCI CH5 starts.
- After the BCI CH5 conversion completes, SW1 CH1 starts. When the SW1 CH1 conversion completes, the SW1 conversion sequence completes, and an interrupt is sent to the MADC SIH.
- In accordance with the revolving priority, SW2 CH2 is converted followed by BCI CH4, CH3, CH2, and CH1.

8.4.6 Sequence Conversion Time

For a single-channel conversion request, the minimum time for conversion is 22*T, and the maximum time for conversion is 39*T, where T depends on the MADC frequency.

For an N-channel RT conversion sequence or an N-channel nonaborted asynchronous conversion sequence, the minimum total time for conversion is given by the formula (4 + N*18) * T. For this case, the maximum total time for conversion is (6+ N*33) * T.

Based on these conversion times, the minimum duration of a pulse on startadc from the host processor is 2*(1/6)*T and the maximum duration of the startadc pulse is 24*T.

Assuming a MADC functional frequency of 1 MHz, the minimum time for a single-channel RT, or nonaborted SW1 and SW2 conversion is 22 μs and the maximum time for a single channel conversion is 39 μs.

8.4.7 Interpretation of MADC Result Registers

The input range of the MADC is 0.0 to 1.5 V. The actual input on MADC channels can be different. The device implements prescalers for the MADC input channels to ensure that the range of input to the MADC digital-to-analog converter (DAC) is from 0.0 to 1.5 V. The prescaler is usually a voltage divider resistor circuit that performs linear scaling over the input range.

ADCIN0 does not have a prescaler. Its input range is 0.0 to 1.5 V.

Table 8-2 shows the prescaler ratio for various MADC input channels as well as with the prescaler ratio. The prescaler ratio shown in this table is the ratio of the prescaler output voltage to the prescaler input voltage.

Table 8-2. MADC Channel Prescaler Divide Ratio

MADC Channel Number	Analog Input Range (V)		Prescaler Output Range (V)		Prescaler Divider Ratio (R)
	Minimum	Maximum	Minimum	Maximum	
ADCIN0	0.0	1.5	N/A	N/A	1
ADCIN2	0.0	2.5	0.0	1.5	0.6 (= 1.5/2.5)

The result of MACD for a channel is a 10-bit value with a resolution of $(1.5/2^{10} – 1)$ V for each least-significant bit (LSB). If the result is all 0s (0000000000), this corresponds to the lowest input voltage, 0.0 V, while all 1s (1111111111) corresponds to 1.5 V. To get actual input voltage, use the following formula:

Analog Input (V) = conv_result * step_size/R

Where:

conv_result = decimal value of 10-bit conversion result

step_size = $1.5/(2^{10} – 1)$

R = Prescaler ratio for input channel as given in Table 8-2

8.5 Monitoring ADC Programming Model

This section provides examples of how to program the MADC for various types of conversions. Before starting any conversion request, the host processor must ensure that the MADC functional clocks are correctly enabled, as described in Section 8.3.1, *MADC Clocks*.

8.5.1 Asynchronous Conversion by SW1 on ADCIN0

The following sequence of steps is followed by the host processor in requesting SW1 conversion and retrieving results from the MADC through the I^2C interface.

1. Set up the MADC_IMR1 register to receive the interrupt on INT1 by setting the MADC_IMR1[1] SW1_IMR1 bit to 0.
2. Power on the MADC by setting the CTRL1[0] MADCON bit to 1.
3. Select ADCIN0 for conversion: Set the SW1SELECT_LSB register to 0x00.
4. Set up the register for averaging (if needed): Set the SW1AVERAGE_LSB register to 0x01.
5. Start the conversion on the selected channels by setting the CTRL_SW1[5] SW1 bit to 1.
6. When the INT1 interrupt is detected, read the MADC_ISR1 register:
   (a) If the value of the MADC_ISR1[0] SW1_ISR1 bit is 1, read the GP conversion results from the GPCH0_LSB and GPCH0_MSB registers for the ADCIN0 channel.
   (b) Reading MADC_ISR1 in Step 7a clears the interrupt, assuming that the MADC_SIH_CTRL[2] COR bit has the default value of 1.

8.5.2 VBAT Monitoring by the USB Subchip

The following minimum sequence of steps is followed by the host processor when monitoring the VBAT channel by the USB conversion requests. This sequence lets the device interrupt the host processor when the VBAT input crosses (both rising and falling) the 3.25 V level.

1. Program the USB reference level to 3.25 V:
   (a) Set the USBREF_LSB[7:6] BIT_1DT0 bit field to 11.
   (b) Set the USBREF_MSB[7:0] BIT_9DT2 bit field to 0x8A.
2. Enable the VUSB1V5 and VUSB1V8 LDOs: Assign these LDOs to a device group that is in ACTIVE state. For more information, see Chapter 5, *Resets and Power Management*.
3. Enable the VBAT timer in the USB subchip: Set the OTHER_FUNC_CTRL2_SET[0] VBAT_TIMER_EN bit of the USB subchip to 1.
4. Enable the VBAT prescaler in the BCI: Set the BCICTL1[1] MESBAT bit to 1.
5. Let MADC interrupts be generated when the VBAT level falls below and rises above the reference level: Set the CTRL2[1] RSVD0 bit of the MADC to 1.
6. Program the MADC to issue an interrupt on the rising and falling edges:
   (a) Set the MADC_EDR[7] USB_EDRRISING bit to 1.
   (b) Set the MADC_EDR[6] USB_EDRFALLING bit to 1.
7. Set up the MADC_IMR1 register to receive an interrupt on INT1: Set the MADC_IMR1[3] USB_IMR1 bit to 0.
8. When the VBAT level crosses the 3.25 V level, an interrupt is issued to the host processor on INT1. Read the MADC_ISR1 register:
   (a) If the value of the MADC_ISR1[3] USB_ISR1 bit is 1, read the GP conversion result from the GPCH12_LSB and GPCH12_MSB registers to compute the current VBAT level.
   (b) Reading MADC_ISR in Step 8a clears the interrupt, assuming that the MADC_SIH_CTRL[2] COR bit has the default value of 1.

8.6 Monitoring ADC Register Manual

This section summarizes the MADC registers and describes them in detail..

8.6.1 Device Monitoring ADC Register Summary

Table 8-3 lists the general mapping of the MADC registers. The MADC is at base address 0x0000 0000 with respect to the auxiliary subchip of the device. For information about the device addressing registers, see Chapter 2, *Control Interface*.

Table 8-3. Device Monitoring ADC Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
CTRL1	RW	8	0x0000 0000
CTRL2	RW	8	0x0000 0001
RTSELECT_LSB	RW	8	0x0000 0002
RTSELECT_MSB	RW	8	0x0000 0003
RTAVERAGE_LSB	RW	8	0x0000 0004
RTAVERAGE_MSB	RW	8	0x0000 0005
SW1SELECT_LSB	RW	8	0x0000 0006
SW1SELECT_MSB	RW	8	0x0000 0007
SW1AVERAGE_LSB	RW	8	0x0000 0008
SW1AVERAGE_MSB	RW	8	0x0000 0009
SW2SELECT_LSB	RW	8	0x0000 000A
SW2SELECT_MSB	RW	8	0x0000 000B
SW2AVERAGE_LSB	RW	8	0x0000 000C
SW2AVERAGE_MSB	RW	8	0x0000 000D
BCI_USBAVERAGE	RW	8	0x0000 000E
USBREF_LSB	RW	8	0x0000 0010
USBREF_MSB	RW	8	0x0000 0011
CTRL_SW1	RW	8	0x0000 0012
CTRL_SW2	RW	8	0x0000 0013
RTCH0_LSB	RW	8	0x0000 0017
RTCH0_MSB	RW	8	0x0000 0018
RTCH1_LSB	RW	8	0x0000 0019
RTCH1_MSB	RW	8	0x0000 001A
RTCH2_LSB	RW	8	0x0000 001B
RTCH2_MSB	RW	8	0x0000 001C
RTCH3_LSB	RW	8	0x0000 001D
RTCH3_MSB	RW	8	0x0000 001E
RTCH4_LSB	RW	8	0x0000 001F
RTCH4_MSB	RW	8	0x0000 0020
RTCH5_LSB	RW	8	0x0000 0021
RTCH5_MSB	RW	8	0x0000 0022
RTCH6_LSB	RW	8	0x0000 0023
RTCH6_MSB	RW	8	0x0000 0024
RTCH7_LSB	RW	8	0x0000 0025
RTCH7_MSB	RW	8	0x0000 0026
RTCH8_LSB	RW	8	0x0000 0027
RTCH8_MSB	RW	8	0x0000 0028
RTCH9_LSB	RW	8	0x0000 0029
RTCH9_MSB	RW	8	0x0000 002A
RTCH10_LSB	RW	8	0x0000 002B

Table 8-3. Device Monitoring ADC Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address
RTCH10_MSB	RW	8	0x0000 002C
RTCH11_LSB	RW	8	0x0000 002D
RTCH11_MSB	RW	8	0x0000 002E
RTCH12_LSB	RW	8	0x0000 002F
RTCH12_MSB	RW	8	0x0000 0030
RTCH13_LSB	RW	8	0x0000 0031
RTCH13_MSB	RW	8	0x0000 0032
RTCH14_LSB	RW	8	0x0000 0033
RTCH14_MSB	RW	8	0x0000 0034
RTCH15_LSB	RW	8	0x0000 0035
RTCH15_MSB	RW	8	0x0000 0036
GPCH0_LSB	RW	8	0x0000 0037
GPCH0_MSB	RW	8	0x0000 0038
GPCH1_LSB	RW	8	0x0000 0039
GPCH1_MSB	RW	8	0x0000 003A
GPCH2_LSB	RW	8	0x0000 003B
GPCH2_MSB	RW	8	0x0000 003C
GPCH3_LSB	RW	8	0x0000 003D
GPCH3_MSB	RW	8	0x0000 003E
GPCH4_LSB	RW	8	0x0000 003F
GPCH4_MSB	RW	8	0x0000 0040
GPCH5_LSB	RW	8	0x0000 0041
GPCH5_MSB	RW	8	0x0000 0042
GPCH6_LSB	RW	8	0x0000 0043
GPCH6_MSB	RW	8	0x0000 0044
GPCH7_LSB	RW	8	0x0000 0045
GPCH7_MSB	RW	8	0x0000 0046
GPCH8_LSB	RW	8	0x0000 0047
GPCH8_MSB	RW	8	0x0000 0048
GPCH9_LSB	RW	8	0x0000 0049
GPCH9_MSB	RW	8	0x0000 004A
GPCH10_LSB	RW	8	0x0000 004B
GPCH10_MSB	RW	8	0x0000 004C
GPCH11_LSB	RW	8	0x0000 004D
GPCH11_MSB	RW	8	0x0000 004E
GPCH12_LSB	RW	8	0x0000 004F
GPCH12_MSB	RW	8	0x0000 0050
GPCH13_LSB	RW	8	0x0000 0051
GPCH13_MSB	RW	8	0x0000 0052
GPCH14_LSB	RW	8	0x0000 0053
GPCH14_MSB	RW	8	0x0000 0054
GPCH15_LSB	RW	8	0x0000 0055
GPCH15_MSB	RW	8	0x0000 0056
BCICH0_LSB	RW	8	0x0000 0057
BCICH0_MSB	RW	8	0x0000 0058
BCICH1_LSB	RW	8	0x0000 0059
BCICH1_MSB	RW	8	0x0000 005A

Table 8-3. Device Monitoring ADC Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address
BCICH2_LSB	RW	8	0x0000 005B
BCICH2_MSB	RW	8	0x0000 005C
BCICH3_LSB	RW	8	0x0000 005D
BCICH3_MSB	RW	8	0x0000 005E
BCICH4_LSB	RW	8	0x0000 005F
BCICH4_MSB	RW	8	0x0000 0060
MADC_ISR1	RW	8	0x0000 0061
MADC_IMR1	RW	8	0x0000 0062
MADC_ISR2	RW	8	0x0000 0063
MADC_IMR2	RW	8	0x0000 0064
MADC_SIR	RW	8	0x0000 0065
MADC_EDR	RW	8	0x0000 0066
MADC_SIH_CTRL	RW	8	0x0000 0067

8.7 Device Monitoring ADC Registers

This section gives details of each device MADC register.

Table 8-4. CTRL1

Address Offset	0x00		
Physical Address	0x0000 0000	**Instance**	AUX_SCMADC
Description	Control register: The MADCON bit field powers on the MADC, permitting the clock generator to supply 1 MHz clocks.		
Type	RW		

7	6	5	4	3	2	1	0
VBATREF_LSB					RSVD1	RSVD0	MADCON

Bits	Field Name	Description	Type	Reset
7:3	VBATREF_LSB	LSB of the VBAT compared value (5 LSBs)	RW	0x00
2	RSVD1	Reserved for spare	RW	0
1	RSVD0	Reserved for spare	RW	0
0	MADCON	MADC software power on. When set to 1, MADC is powered.	RW	0

Table 8-5. CTRL2

Address Offset	0x01		
Physical Address	0x0000 0001	**Instance**	AUX_SCMADC
Description	Control register: STARTADCRF controls STARTADC detection polarity and is write-protected when MADCON is active. USB_INT_MODE configures the way an interrupt is generated from MADC after a VBATMEAS channel conversion when a USB conversion request occurs. The VBATREF_MSB register is associated with VBAT monitoring (linked with the VBATREF Vbat comparator). VBATREF_LSB bit fields are part of the CTRL1 register.		
Type	RW		

7	6	5	4	3	2	1	0
VBATREF_MSB					RSVD1	USB_INT_MODE	STARTADCRF

Bits	Field Name	Description	Type	Reset
7:3	VBATREF_MSB	LSB of the VBAT compared value (5 MSBs) VBATREF_MSB register is associated with the VBAT monitoring function (linked with the VBATREF Vbat comparator). VBATREF_LSB bit field is part of the CTRL1 register.	RW	0x00
2	RSVD1	Reserved for spare	RW	0
1	USB_INT_MODE	0 (default): The MADC sends an interrupt when the value resulting from the VBATMEAS channel is lower than the USBREF register value. 1: An interrupt is sent when the conversion value goes over or under the USBREF value. This is used only in case of USB conversion request.	RW	0
0	STARTADCRF	STARDADC rising-/falling-edge detection bit field. When set to 1, STARDADC is active high (default value).	RW	1

Table 8-6. RTSELECT_LSB

Address Offset	0x02		
Physical Address	0x0000 0002	**Instance**	AUX_SCMADC
Description	RT conversion channel selection register for channels 0 to 7 These bits become read-only during RT conversion. When the CHi bit is set, MADC channel i is inserted in the conversion sequence started by a RT request through STARTADC.		
Type	RW		

7	6	5	4	3	2	1	0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Bits	Field Name	Description	Type	Reset
7	CH7	RT conversion channel selection register for channel 7	RW	0
6	CH6	RT conversion channel selection register for channel 6	RW	0
5	CH5	RT conversion channel selection register for channel 5	RW	0
4	CH4	RT conversion channel selection register for channel 4	RW	0
3	CH3	RT conversion channel selection register for channel 3	RW	0
2	CH2	RT conversion channel selection register for channel 2	RW	0
1	CH1	RT conversion channel selection register for channel 1	RW	0
0	CH0	RT conversion channel selection register for channel 0	RW	0

Table 8-7. RTSELECT_MSB

Address Offset	0x03		
Physical Address	0x0000 0003	**Instance**	AUX_SCMADC
Description	RT conversion channel selection register for channels 8 to 15 These bits become read-only during RT conversion. When the CHi bit is set, MADC channel i is inserted in the conversion sequence started by a RT request through STARTADC.		
Type	RW		

7	6	5	4	3	2	1	0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8

Bits	Field Name	Description	Type	Reset
7	CH15	RT conversion channel selection register for channel 15	RW	0
6	CH14	RT conversion channel selection register for channel 14	RW	0
5	CH13	RT conversion channel selection register for channel 13	RW	0
4	CH12	RT conversion channel selection register for channel 12	RW	0
3	CH11	RT conversion channel selection register for channel 11	RW	0
2	CH10	RT conversion channel selection register for channel 10	RW	0
1	CH9	RT conversion channel selection register for channel 9	RW	0
0	CH8	RT conversion channel selection register for channel 8	RW	0

Table 8-8. RTAVERAGE_LSB

Address Offset	0x04		
Physical Address	0x0000 0004	**Instance**	AUX_SCMADC
Description	RT conversion averaging function selection register for channels 0 to 7 These bits become read-only during RT conversion. When the AV_CHi bit is set, the MADC takes an average during RT conversion of channel i (it measures the value four times consecutively and stores the average).		
Type	RW		

7	6	5	4	3	2	1	0
AV_CH7	AV_CH6	AV_CH5	AV_CH4	AV_CH3	AV_CH2	AV_CH1	AV_CH0

Bits	Field Name	Description	Type	Reset
7	AV_CH7	RT conversion averaging function selection register for channel 7	RW	0
6	AV_CH6	RT conversion averaging function selection register for channel 6	RW	0
5	AV_CH5	RT conversion averaging function selection register for channel 5	RW	0
4	AV_CH4	RT conversion averaging function selection register for channel 4	RW	0
3	AV_CH3	RT conversion averaging function selection register for channel 3	RW	0
2	AV_CH2	RT conversion averaging function selection register for channel 2	RW	0
1	AV_CH1	RT conversion averaging function selection register for channel 1	RW	0
0	AV_CH0	RT conversion averaging function selection register for channel 0	RW	0

Table 8-9. RTAVERAGE_MSB

Address Offset	0x05		
Physical Address	0x0000 0005	**Instance**	AUX_SCMADC
Description	RT conversion averaging function selection register for channels 8 to 15 These bits become read-only during RT conversion. When the AV_CHi bit is set, the MADC takes an average during RT conversion of channel i (it measures the value four times consecutively and stores the average).		
Type	RW		

7	6	5	4	3	2	1	0
AV_CH15	AV_CH14	AV_CH13	AV_CH12	AV_CH11	AV_CH10	AV_CH9	AV_CH8

Bits	Field Name	Description	Type	Reset
7	AV_CH15	RT conversion averaging function selection register for channel 15	RW	0
6	AV_CH14	RT conversion averaging function selection register for channel 14	RW	0
5	AV_CH13	RT conversion averaging function selection register for channel 13	RW	0
4	AV_CH12	RT conversion averaging function selection register for channel 12	RW	0
3	AV_CH11	RT conversion averaging function selection register for channel 11	RW	0
2	AV_CH10	RT conversion averaging function selection register for channel 10	RW	0
1	AV_CH9	RT conversion averaging function selection register for channel 9	RW	0
0	AV_CH8	RT conversion averaging function selection register for channel 8	RW	0

Table 8-10. SW1SELECT_LSB

Address Offset	0x06		
Physical Address	0x0000 0006	**Instance**	AUX_SCMADC
Description	SW1 conversion channel selection register for channels 0 to 7 These bits become read-only during software conversion initiated by the SW1 bit. When the CHi bit is set, MADC channel i is inserted in the conversion sequence.		
Type	RW		

7	6	5	4	3	2	1	0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Bits	Field Name	Description	Type	Reset
7	CH7	SW1 conversion channel selection register for channel 7	RW	0
6	CH6	SW1 conversion channel selection register for channel 6	RW	0
5	CH5	SW1 conversion channel selection register for channel 5	RW	0
4	CH4	SW1 conversion channel selection register for channel 4	RW	0
3	CH3	SW1 conversion channel selection register for channel 3	RW	0
2	CH2	SW1 conversion channel selection register for channel 2	RW	0
1	CH1	SW1 conversion channel selection register for channel 1	RW	0
0	CH0	SW1 conversion channel selection register for channel 0	RW	0

Table 8-11. SW1SELECT_MSB

Address Offset	0x07		
Physical Address	0x0000 0007	**Instance**	AUX_SCMADC
Description	SW1 conversion channel selection register for channels 8 to 15 These bits become read-only during software conversion initiated by the SW1 bit. When the CHi bit is set, MADC channel i is inserted in the conversion sequence.		
Type	RW		

7	6	5	4	3	2	1	0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8

Bits	Field Name	Description	Type	Reset
7	CH15	SW1 conversion channel selection register for channel 15	RW	0
6	CH14	SW1 conversion channel selection register for channel 14	RW	0
5	CH13	SW1 conversion channel selection register for channel 13	RW	0
4	CH12	SW1 conversion channel selection register for channel 12	RW	0
3	CH11	SW1 conversion channel selection register for channel 11	RW	0
2	CH10	SW1 conversion channel selection register for channel 10	RW	0
1	CH9	SW1 conversion channel selection register for channel 9	RW	0
0	CH8	SW1 conversion channel selection register for channel 8	RW	0

Table 8-12. SW1AVERAGE_LSB

Address Offset	0x08		
Physical Address	0x0000 0008	**Instance**	AUX_SCMADC
Description	SW1 conversion averaging function selection register for channels 0 to 7 These bits become read-only during SW1 conversion. When the AV_CHi bit is set, the MADC takes an average during SW1 conversion of channel i (it measures the value four times consecutively and stores the average).		
Type	RW		

7	6	5	4	3	2	1	0
AV_CH7	AV_CH6	AV_CH5	AV_CH4	AV_CH3	AV_CH2	AV_CH1	AV_CH0

Bits	Field Name	Description	Type	Reset
7	AV_CH7	SW1 conversion averaging function selection register for channel 7	RW	0
6	AV_CH6	SW1 conversion averaging function selection register for channel 6	RW	0
5	AV_CH5	SW1 conversion averaging function selection register for channel 5	RW	0
4	AV_CH4	SW1 conversion averaging function selection register for channel 4	RW	0
3	AV_CH3	SW1 conversion averaging function selection register for channel 3	RW	0
2	AV_CH2	SW1 conversion averaging function selection register for channel 2	RW	0
1	AV_CH1	SW1 conversion averaging function selection register for channel 1	RW	0
0	AV_CH0	SW1 conversion averaging function selection register for channel 0	RW	0

Table 8-13. SW1AVERAGE_MSB

Address Offset	0x09		
Physical Address	0x0000 0009	**Instance**	AUX_SCMADC
Description	SW1 conversion averaging function selection register for channels 8 to 15 These bits become read-only during SW1 conversion. When the AV_CHi bit is set, the MADC takes an average during SW1 conversion of channel i (it measures the value four times consecutively and stores the average).		
Type	RW		

7	6	5	4	3	2	1	0
AV_CH15	AV_CH14	AV_CH13	AV_CH12	AV_CH11	AV_CH10	AV_CH9	AV_CH8

Bits	Field Name	Description	Type	Reset
7	AV_CH15	SW1 conversion averaging function selection register for channel 15	RW	0
6	AV_CH14	SW1 conversion averaging function selection register for channel 14	RW	0
5	AV_CH13	SW1 conversion averaging function selection register for channel 13	RW	0
4	AV_CH12	SW1 conversion averaging function selection register for channel 12	RW	0
3	AV_CH11	SW1 conversion averaging function selection register for channel 11	RW	0
2	AV_CH10	SW1 conversion averaging function selection register for channel 10	RW	0
1	AV_CH9	SW1 conversion averaging function selection register for channel 9	RW	0
0	AV_CH8	SW1 conversion averaging function selection register for channel 8	RW	0

Table 8-14. SW2SELECT_LSB

Address Offset	0x0A		
Physical Address	0x0000 000A	**Instance**	AUX_SCMADC
Description	SW2 conversion channel selection register for channels 0 to 7 These bits become read-only during software conversion initiated by the SW2 bit. When the CHi bit is set, MADC channel i is inserted in the conversion sequence.		
Type	RW		

7	6	5	4	3	2	1	0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Bits	Field Name	Description	Type	Reset
7	CH7	SW2 conversion channel selection register for channel 7	RW	0
6	CH6	SW2 conversion channel selection register for channel 6	RW	0
5	CH5	SW2 conversion channel selection register for channel 5	RW	0
4	CH4	SW2 conversion channel selection register for channel 4	RW	0
3	CH3	SW2 conversion channel selection register for channel 3	RW	0
2	CH2	SW2 conversion channel selection register for channel 2	RW	0
1	CH1	SW2 conversion channel selection register for channel 1	RW	0
0	CH0	SW2 conversion channel selection register for channel 0	RW	0

Table 8-15. SW2SELECT_MSB

Address Offset	0x0B		
Physical Address	0x0000 000B	**Instance**	AUX_SCMADC
Description	SW2 conversion channel selection register for channels 8 to 15 These bits become read-only during software conversion initiated by the SW2 bit. When the CHi bit is set, MADC channel i is inserted in the conversion sequence.		
Type	RW		

7	6	5	4	3	2	1	0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8

Bits	Field Name	Description	Type	Reset
7	CH15	SW2 conversion channel selection register for channel 15	RW	0
6	CH14	SW2 conversion channel selection register for channel 14	RW	0
5	CH13	SW2 conversion channel selection register for channel 13	RW	0
4	CH12	SW2 conversion channel selection register for channel 12	RW	0
3	CH11	SW2 conversion channel selection register for channel 11	RW	0
2	CH10	SW2 conversion channel selection register for channel 10	RW	0
1	CH9	SW2 conversion channel selection register for channel 9	RW	0
0	CH8	SW2 conversion channel selection register for channel 8	RW	0

Table 8-16. SW2AVERAGE_LSB

Address Offset	0x0C		
Physical Address	0x0000 000C	**Instance**	AUX_SCMADC
Description	SW2 conversion averaging function selection register for channels 0 to 7 These bits become read-only during SW2 conversion. When the AV_CHi bit is set, the MADC takes an average during SW2 conversion of channel i (it measures the value four times consecutively and stores the average).		
Type	RW		

7	6	5	4	3	2	1	0
AV_CH7	AV_CH6	AV_CH5	AV_CH4	AV_CH3	AV_CH2	AV_CH1	AV_CH0

Bits	Field Name	Description	Type	Reset
7	AV_CH7	SW2 conversion averaging function selection register for channel 7	RW	0
6	AV_CH6	SW2 conversion averaging function selection register for channel 6	RW	0
5	AV_CH5	SW2 conversion averaging function selection register for channel 5	RW	0
4	AV_CH4	SW2 conversion averaging function selection register for channel 4	RW	0
3	AV_CH3	SW2 conversion averaging function selection register for channel 3	RW	0
2	AV_CH2	SW2 conversion averaging function selection register for channel 2	RW	0
1	AV_CH1	SW2 conversion averaging function selection register for channel 1	RW	0
0	AV_CH0	SW2 conversion averaging function selection register for channel 0	RW	0

Table 8-17. SW2AVERAGE_MSB

Address Offset	0x0D		
Physical Address	0x0000 000D	**Instance**	AUX_SCMADC
Description	SW2 conversion averaging function selection register for channels 8 to 15 These bits become read-only during SW2 conversion. When the AV_CHi bit is set, the MADC takes an average during SW2 conversion of channel i (it measures the value four times consecutively and stores the average).		
Type	RW		

7	6	5	4	3	2	1	0
AV_CH15	AV_CH14	AV_CH13	AV_CH12	AV_CH11	AV_CH10	AV_CH9	AV_CH8

Bits	Field Name	Description	Type	Reset
7	AV_CH15	SW2 conversion averaging function selection register for channel 15	RW	0
6	AV_CH14	SW2 conversion averaging function selection register for channel 14	RW	0
5	AV_CH13	SW2 conversion averaging function selection register for channel 13	RW	0
4	AV_CH12	SW2 conversion averaging function selection register for channel 12	RW	0
3	AV_CH11	SW2 conversion averaging function selection register for channel 11	RW	0
2	AV_CH10	SW2 conversion averaging function selection register for channel 10	RW	0
1	AV_CH9	SW2 conversion averaging function selection register for channel 9	RW	0
0	AV_CH8	SW2 conversion averaging function selection register for channel 8	RW	0

Table 8-18. BCI_USBAVERAGE

Address Offset	0x0E		
Physical Address	0x0000 000E	**Instance**	AUX_SCMADC
Description	BCI and USB conversion averaging function selection register for BCI and USB channels These bits become read-only during BCI and USB conversion. When the AV_CHi bit is set, the MADC takes an average during BCI or USB conversion of channel i (it measures the value four times consecutively and stores the average).		
Type	RW		

7	6	5	4	3	2	1	0
RSVD2	RSVD1	AV_USB_CH0	AV_BCI_CH4	AV_BCI_CH3	AV_BCI_CH2	AV_BCI_CH1	AV_BCI_CH0

Bits	Field Name	Description	Type	Reset
7	RSVD2	Reserved. Read returns 0.	Reserved	0
6	RSVD1	Reserved. Read returns 0.	Reserved	0
5	AV_USB_CH0	USB conversion averaging function selection register for channel 0	RW	0
4	AV_BCI_CH4	BCI conversion averaging function selection register for channel 4	RW	0
3	AV_BCI_CH3	BCI conversion averaging function selection register for channel 3	RW	0
2	AV_BCI_CH2	BCI conversion averaging function selection register for channel 2	RW	0
1	AV_BCI_CH1	BCI conversion averaging function selection register for channel 1	RW	0
0	AV_BCI_CH0	BCI conversion averaging function selection register for channel 0	RW	0

Table 8-19. USBREF_LSB

Address Offset	0x10		
Physical Address	0x0000 0010	**Instance**	AUX_SCMADC
Description	LSB of the reference value to be compared to the conversion result requested by the USB for VBAT conversion		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	LSB of the VBAT compared value (2 LSBs)	RW	0x3
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-20. USBREF_MSB

Address Offset	0x11		
Physical Address	0x0000 0011	**Instance**	AUX_SCMADC
Description	MSB of the reference value to be compared to the conversion result requested by the USB for VBAT conversion		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	MSB of the VBAT compared value (8 MSBs)	RW	0x8C

Table 8-21. CTRL_SW1

Address Offset	0x12		
Physical Address	0x0000 0012	**Instance**	AUX_SCMADC
Description	This register allows the start of an SW1 software conversion and gives the conversion status of all types of conversion requests.		
Type	RW		

7	6	5	4	3	2	1	0
VBATREF_STS	USBREF_STS	SW1	EOC_USB	EOC_BCI	EOC_RT	EOC_SW1	BUSY

Bits	Field Name	Description	Type	Reset
7	VBATREF_STS	VBATREF/VBAT comparator status bit. When set to 1, measured Vbat is greater than the VBATREF value programmed in the VBATREF_LSB and VBATREF_MSB bit fields in the CTRL1/CTRL2 registers; otherwise, the status is 0. It is the same bit as the VBATREF_STS bit in the CTRL_SW2 register.	R	1
6	USBREF_STS	USBREF/VBAT comparator status bit. When set to 1, measured Vbat is greater than the USBREF value programmed in the USBREF_LSB and USBREF_MSB registers; otherwise, the status is 0. It is the same bit as the USBREF_STS bit in the CTRL_SW2 register.	R	1
5	SW1	SW1 Toggle bit used by the host processor to start an all-channel conversion. Writing logical 0 in this bit has no effect.	W	0
4	EOC_USB	End of conversion USB When this bit is set, the MADC indicates that a conversion required by the USB bit is terminated. An interrupt was sent to the interrupt controller at the end of the required conversion sequence. The default state is logic 1, indicating that the conversion is terminated. While the associated conversion sequence is running, this bit is at logical 0. This bit is the same as EOC_USB bit in the CTRL_SW2 register.	R	1
3	EOC_BCI	End of conversion BCI When this bit is set, the MADC indicates that a BCI conversion is terminated. A data-ready signal was sent to the BCI at the end of the required conversion sequence. The default state is logic 1, indicating that the conversion is terminated. While the associated conversion sequence is running, this bit is at logical 0. It is the same bit as the EOC_BCI bit in the CTRL_SW2 register.	R	1
2	EOC_RT	End of conversion RT When this bit is set, the MADC indicates that a conversion with RT constraints is terminated. An interrupt was sent to the interrupt controller at the end of the required conversion sequence. The default state is logic 1, indicating that the conversion is terminated. While the associated conversion sequence is running this bit is at logical 0. It is the same bit as the EOC_RT bit in the CTRL_SW2 register.	R	1

Bits	Field Name	Description	Type	Reset
1	EOC_SW1	End of conversion SW1 When this bit is set, the MADC indicates that a conversion required by the SW1 bit is terminated. An interrupt was sent to the interrupt controller at the end of the required conversion sequence. The default state is logic 1, indicating that the conversion is terminated. While the associated conversion sequence is running, this bit is at logical 0.	R	1
0	BUSY	MADC busy signal When this bit is at 1, the MADC is running its sequence of conversions. It is the same signal as busy signal in CTRL_SW2 register.	R	0

Table 8-22. CTRL_SW2

Address Offset	0x13		
Physical Address	0x0000 0013	**Instance**	AUX_SCMADC
Description	This register allows the start of an SW2 software conversion and gives the conversion status of all types of conversion requests.		
Type	RW		

7	6	5	4	3	2	1	0
VBATREF_STS	USBREF_STS	SW2	EOC_USB	EOC_BCI	EOC_RT	EOC_SW2	BUSY

Bits	Field Name	Description	Type	Reset
7	VBATREF_STS	VBATREF/VBAT comparator status bit. When set to 1, measured Vbat is greater than the VBATREF value programmed in the VBATREF_LSB and VBATREF_MSB bit fields in the CTRL1/CTRL2 registers; otherwise, status is 0. It is the same bit as the VBATREF_STS bit in the CTRL_SW1 register.	R	1
6	USBREF_STS	USBREF/VBAT comparator status bit. When set to 1, measured Vbat is greater than the USBREF value programmed in the USBREF_LSB and USBREF_MSB registers; otherwise, status is 0. It is the same bit as the USBREF_STS bit in the CTRL_SW1 register.	R	1
5	SW2	SW2 Toggle bit used by the host processor to start an all-channel conversion. Writing logical 0 in this bit has no effect.	W	0
4	EOC_USB	End of conversion USB When this bit is set, the MADC indicates that a conversion required by the USB bit is terminated. An interrupt was sent to the interrupt controller at the end of the required conversion sequence. The default state is logic 1, indicating that the conversion is terminated. While the associated conversion sequence is running, this bit is at logical 0. This bit is the same bit as the EOC_USB bit in the CTRL_SW2 register.	R	1
3	EOC_BCI	End of conversion BCI When this bit is set, the MADC indicates that a BCI conversion is terminated. A data-ready signal was sent to the BCI at the end of the required conversion sequence. The default state is logic 1, indicating that the conversion is terminated. While the associated conversion sequence is running, this bit is at logical 0. It is the same bit as the EOC_BCI bit in the CTRL_SW1 register.	R	1
2	EOC_RT	End of conversion RT When this bit is set, the MADC indicates that a conversion with RT constraints is terminated. An interrupt was sent to the interrupt controller at the end of the required conversion sequence. The default state is logic 1, indicating that the conversion is terminated. While the associated conversion sequence is running, this bit is at logical 0. It is the same bit as the EOC_RT bit in the CTRL_SW1 register.	R	1
1	EOC_SW2	End of conversion SW2 When this bit is set, the MADC indicates that a conversion required by the SW2 bit is terminated. An interrupt was sent to the interrupt controller at the end of the required conversion sequence. The default state is logic 1, indicating that the conversion is terminated. While the associated conversion sequence is running, this bit is at logical 0.	R	1

Bits	Field Name	Description	Type	Reset
0	BUSY	MADC busy signal When this bit is at 1, the MADC is running its sequence of conversions. It is the same signal as the busy signal in the CTRL_SW1 register.	R	0

Table 8-23. RTCH0_LSB

Address Offset	0x17		
Physical Address	0x0000 0017	**Instance**	AUX_SCMADC
Description	Channel 0 RT conversion result register (ADIN0 = BTYPE)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 0 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-24. RTCH0_MSB

Address Offset	0x18		
Physical Address	0x0000 0018	**Instance**	AUX_SCMADC
Description	Channel 0 RT conversion result register (ADIN0 = BTYPE)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 0 − result of conversion (8 MSBs)	R	0x00

Table 8-25. RTCH1_LSB

Address Offset	0x19		
Physical Address	0x0000 0019	**Instance**	AUX_SCMADC
Description	Channel 1 RT conversion result register (ADIN1 = BTEMP).		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 1 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0

Bits	Field Name	Description	Type	Reset
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-26. RTCH1_MSB

Address Offset	0x1A		
Physical Address	0x0000 001A	**Instance**	AUX_SCMADC
Description	Channel 1 RT conversion result register (ADIN1 = BTEMP)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 1 − result of conversion (8 MSBs)	R	0x00

Table 8-27. RTCH2_LSB

Address Offset	0x1B		
Physical Address	0x0000 001B	**Instance**	AUX_SCMADC
Description	Channel 2 RT conversion result register (ADIN2)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 2 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-28. RTCH2_MSB

Address Offset	0x1C		
Physical Address	0x0000 001C	**Instance**	AUX_SCMADC
Description	Channel 2 RT conversion result register (ADIN2)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 2 − result of conversion (8 MSBs)	R	0x00

Table 8-29. RTCH3_LSB

Address Offset	0x1D		
Physical Address	0x0000 001D	**Instance**	AUX_SCMADC
Description	Channel 3 RT conversion result register (ADIN3)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 3 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-30. RTCH3_MSB

Address Offset	0x1E		
Physical Address	0x0000 001E	**Instance**	AUX_SCMADC
Description	Channel 3 RT conversion result register (ADIN3)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 3 − result of conversion (8 MSBs)	R	0x00

Table 8-31. RTCH4_LSB

Address Offset	0x1F		
Physical Address	0x0000 001F	**Instance**	AUX_SCMADC
Description	Channel 4 RT conversion result register (ADIN4)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 4 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-32. RTCH4_MSB

Address Offset	0x20		
Physical Address	0x0000 0020	**Instance**	AUX_SCMADC
Description	Channel 4 RT conversion result register (ADIN4)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 4 − result of conversion (8 MSBs)	R	0x00

Table 8-33. RTCH5_LSB

Address Offset	0x21		
Physical Address	0x0000 0021	**Instance**	AUX_SCMADC
Description	Channel 5 RT conversion result register (ADIN5)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 5 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-34. RTCH5_MSB

Address Offset	0x22		
Physical Address	0x0000 0022	**Instance**	AUX_SCMADC
Description	Channel 5 RT conversion result register (ADIN5)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 5 − result of conversion (8 MSBs)	R	0x00

Table 8-35. RTCH6_LSB

Address Offset	0x23		
Physical Address	0x0000 0023	**Instance**	AUX_SCMADC
Description	Channel 6 RT conversion result register (ADIN6)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 6 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-36. RTCH6_MSB

Address Offset	0x24		
Physical Address	0x0000 0024	**Instance**	AUX_SCMADC
Description	Channel 6 RT conversion result register (ADIN6)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 6 − result of conversion (8 MSBs)	R	0x00

Table 8-37. RTCH7_LSB

Address Offset	0x25		
Physical Address	0x0000 0025	**Instance**	AUX_SCMADC
Description	Channel 7 RT conversion result register (ADIN7)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 7 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-38. RTCH7_MSB

Address Offset	0x26		
Physical Address	0x0000 0026	**Instance**	AUX_SCMADC
Description	Channel 7 RT conversion result register (ADIN7)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 7 − result of conversion (8 MSBs)	R	0x00

Table 8-39. RTCH8_LSB

Address Offset	0x27		
Physical Address	0x0000 0027	**Instance**	AUX_SCMADC
Description	Channel 8 RT conversion result register (USBVBUS)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 8 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-40. RTCH8_MSB

Address Offset	0x28		
Physical Address	0x0000 0028	**Instance**	AUX_SCMADC
Description	Channel 8 RT conversion result register (USBVBUS)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 8 − result of conversion (8 MSBs)	R	0x00

Table 8-41. RTCH9_LSB

Address Offset	0x29		
Physical Address	0x0000 0029	**Instance**	AUX_SCMADC
Description	Channel 9 RT conversion result register (VBKP)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 9 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-42. RTCH9_MSB

Address Offset	0x2A		
Physical Address	0x0000 002A	**Instance**	AUX_SCMADC
Description	Channel 9 RT conversion result register (VBKP)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 9 − result of conversion (8 MSBs)	R	0x00

Table 8-43. RTCH10_LSB

Address Offset	0x2B		
Physical Address	0x0000 002B	**Instance**	AUX_SCMADC
Description	Channel 10 RT conversion result register (ICHG)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 10 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-44. RTCH10_MSB

Address Offset	0x2C		
Physical Address	0x0000 002C	**Instance**	AUX_SCMADC
Description	Channel 10 RT conversion result register (ADIN10 = ICHG)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 10 − result of conversion (8 MSBs)	R	0x00

Table 8-45. RTCH11_LSB

Address Offset	0x2D		
Physical Address	0x0000 002D	**Instance**	AUX_SCMADC
Description	Channel 11 RT conversion result register (VCHG)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 11 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-46. RTCH11_MSB

Address Offset	0x2E		
Physical Address	0x0000 002E	**Instance**	AUX_SCMADC
Description	Channel 11 RT conversion result register (VCHG)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 11 − result of conversion (8 MSBs)	R	0x00

Table 8-47. RTCH12_LSB

Address Offset	0x2F		
Physical Address	0x0000 002F	**Instance**	AUX_SCMADC
Description	Channel 12 RT conversion result register (VBAT)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 12 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-48. RTCH12_MSB

Address Offset	0x30		
Physical Address	0x0000 0030	**Instance**	AUX_SCMADC
Description	Channel 12 RT conversion result register (VBAT)		
Type	RW		

7	6	5	4	3	2	1	0

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 12 − result of conversion (8 MSBs)	R	0x00

Table 8-49. RTCH13_LSB

Address Offset	0x31		
Physical Address	0x0000 0031	**Instance**	AUX_SCMADC
Description	Channel 13 RT conversion result register (TESTV1)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 13 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-50. RTCH13_MSB

Address Offset	0x32		
Physical Address	0x0000 0032	**Instance**	AUX_SCMADC
Description	Channel 13 RT conversion result register (TESTV1)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 13 − result of conversion (8 MSBs)	R	0x00

Table 8-51. RTCH14_LSB

Address Offset	0x33		
Physical Address	0x0000 0033	**Instance**	AUX_SCMADC
Description	Channel 14 RT conversion result register (TESTV2)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 14 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-52. RTCH14_MSB

Address Offset	0x34		
Physical Address	0x0000 0034	**Instance**	AUX_SCMADC
Description	Channel 14 RT conversion result register (TESTV2)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 14 − result of conversion (8 MSBs)	R	0x00

Table 8-53. RTCH15_LSB

Address Offset	0x35		
Physical Address	0x0000 0035	**Instance**	AUX_SCMADC
Description	Channel 15 RT conversion result register (USB MEASURE)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 15 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-54. RTCH15_MSB

Address Offset	0x36		
Physical Address	0x0000 0036	**Instance**	AUX_SCMADC
Description	Channel 15 RT conversion result register (USB MEASURE)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 15 − result of conversion (8 MSBs)	R	0x00

Table 8-55. GPCH0_LSB

Address Offset	0x37		
Physical Address	0x0000 0037	**Instance**	AUX_SCMADC
Description	Channel 0 GP conversion result register (ADIN0 = BTYPE)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 0 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-56. GPCH0_MSB

Address Offset	0x38		
Physical Address	0x0000 0038	**Instance**	AUX_SCMADC
Description	Channel 0 GP conversion result register (ADIN0 = BTYPE)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 0 − result of conversion (8 MSBs)	R	0x00

Table 8-57. GPCH1_LSB

Address Offset	0x39		
Physical Address	0x0000 0039	**Instance**	AUX_SCMADC
Description	Channel 1 GP conversion result register (ADIN1 = BTEMP)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 1 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-58. GPCH1_MSB

Address Offset	0x3A		
Physical Address	0x0000 003A	**Instance**	AUX_SCMADC
Description	Channel 1 GP conversion result register (ADIN1 = BTEMP)		
Type	RW		

7	6	5	4	3	2	1	0

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 1 − result of conversion (8 MSBs)	R	0x00

Table 8-59. GPCH2_LSB

Address Offset	0x3B		
Physical Address	0x0000 003B	**Instance**	AUX_SCMADC
Description	Channel 2 GP conversion result register (ADIN2)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 2 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-60. GPCH2_MSB

Address Offset	0x3C		
Physical Address	0x0000 003C	**Instance**	AUX_SCMADC
Description	Channel 2 GP conversion result register (ADIN2)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 2 − result of conversion (8 MSBs)	R	0x00

Table 8-61. GPCH3_LSB

Address Offset	0x3D		
Physical Address	0x0000 003D	**Instance**	AUX_SCMADC
Description	Channel 3 GP conversion result register (ADIN3)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 3 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-62. GPCH3_MSB

Address Offset	0x3E		
Physical Address	0x0000 003E	**Instance**	AUX_SCMADC
Description	Channel 3 GP conversion result register (ADIN3)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 3 − result of conversion (8 MSBs)	R	0x00

Table 8-63. GPCH4_LSB

Address Offset	0x3F		
Physical Address	0x0000 003F	**Instance**	AUX_SCMADC
Description	Channel 4 GP conversion result register (ADIN4)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 4 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-64. GPCH4_MSB

Address Offset	0x40		
Physical Address	0x0000 0040	**Instance**	AUX_SCMADC
Description	Channel 4 GP conversion result register (ADIN4)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 4 − result of conversion (8 MSBs)	R	0x00

Table 8-65. GPCH5_LSB

Address Offset	0x41		
Physical Address	0x0000 0041	**Instance**	AUX_SCMADC
Description	Channel 5 GP conversion result register (ADIN5)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 5 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-66. GPCH5_MSB

Address Offset	0x42		
Physical Address	0x0000 0042	**Instance**	AUX_SCMADC
Description	Channel 5 GP conversion result register (ADIN5)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 5 − result of conversion (8 MSBs)	R	0x00

Table 8-67. GPCH6_LSB

Address Offset	0x43		
Physical Address	0x0000 0043	**Instance**	AUX_SCMADC
Description	Channel 6 GP conversion result register (ADIN6)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 6 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-68. GPCH6_MSB

Address Offset	0x44		
Physical Address	0x0000 0044	**Instance**	AUX_SCMADC
Description	Channel 6 GP conversion result register (ADIN6)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 6 − result of conversion (8 MSBs)	R	0x00

Table 8-69. GPCH7_LSB

Address Offset	0x45		
Physical Address	0x0000 0045	**Instance**	AUX_SCMADC
Description	Channel 7 GP conversion result register (ADIN7)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 7 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-70. GPCH7_MSB

Address Offset	0x46		
Physical Address	0x0000 0046	**Instance**	AUX_SCMADC
Description	Channel 7 GP conversion result register (ADIN7)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 7 − result of conversion (8 MSBs)	R	0x00

Table 8-71. GPCH8_LSB

Address Offset	0x47		
Physical Address	0x0000 0047	**Instance**	AUX_SCMADC
Description	Channel 8 GP conversion result register (USBVBUS)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 8 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-72. GPCH8_MSB

Address Offset	0x48		
Physical Address	0x0000 0048	**Instance**	AUX_SCMADC
Description	Channel 8 GP conversion result register (USBVBUS)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 8. Result of conversion (8 MSBs)	R	0x00

Table 8-73. GPCH9_LSB

Address Offset	0x49		
Physical Address	0x0000 0049	**Instance**	AUX_SCMADC
Description	Channel 9 GP conversion result register (VBKP)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 9. − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-74. GPCH9_MSB

Address Offset	0x4A		
Physical Address	0x0000 004A	**Instance**	AUX_SCMADC
Description	Channel 9 GP conversion result register (VBKP)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 9. Result of conversion (8 MSBs)	R	0x00

Table 8-75. GPCH10_LSB

Address Offset	0x4B		
Physical Address	0x0000 004B	**Instance**	AUX_SCMADC
Description	Channel 10 GP conversion result register (ICHG)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 10. Result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-76. GPCH10_MSB

Address Offset	0x4C		
Physical Address	0x0000 004C	**Instance**	AUX_SCMADC
Description	Channel 10 GP conversion result register (ICHG)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 10. Result of conversion (8 MSBs)	R	0x00

Table 8-77. GPCH11_LSB

Address Offset	0x4D		
Physical Address	0x0000 004D	**Instance**	AUX_SCMADC
Description	Channel 11 GP conversion result register (VCHG)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 11. Result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-78. GPCH11_MSB

Address Offset	0x4E		
Physical Address	0x0000 004E	**Instance**	AUX_SCMADC
Description	Channel 11 GP conversion result register (VCHG)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 11. Result of conversion (8 MSBs)	R	0x00

Table 8-79. GPCH12_LSB

Address Offset	0x4F		
Physical Address	0x0000 004F	**Instance**	AUX_SCMADC
Description	Channel 12 GP conversion result register (VBAT)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 12 − result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-80. GPCH12_MSB

Address Offset	0x50		
Physical Address	0x0000 0050	**Instance**	AUX_SCMADC
Description	Channel 12 GP conversion result register (VBAT)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 12. Result of conversion (8 MSBs)	R	0x00

Table 8-81. GPCH13_LSB

Address Offset	0x51		
Physical Address	0x0000 0051	**Instance**	AUX_SCMADC
Description	Channel 13 GP conversion result register (TESTV1)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 13. Result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-82. GPCH13_MSB

Address Offset	0x52		
Physical Address	0x0000 0052	**Instance**	AUX_SCMADC
Description	Channel 13 GP conversion result register (TESTV1)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 13. Result of conversion (8 MSBs)	R	0x00

Table 8-83. GPCH14_LSB

Address Offset	0x53		
Physical Address	0x0000 0053	**Instance**	AUX_SCMADC
Description	Channel 14 GP conversion result register (TESTV2)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 14. Result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-84. GPCH14_MSB

Address Offset	0x54		
Physical Address	0x0000 0054	**Instance**	AUX_SCMADC
Description	Channel 14 GP conversion result register (TESTV2)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 14. Result of conversion (8 MSBs)	R	0x00

Table 8-85. GPCH15_LSB

Address Offset	0x55		
Physical Address	0x0000 0055	**Instance**	AUX_SCMADC
Description	Channel 15 GP conversion result register (USB MEASURE)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 15. Result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-86. GPCH15_MSB

Address Offset	0x56		
Physical Address	0x0000 0056	**Instance**	AUX_SCMADC
Description	Channel 15 GP conversion result register (USB MEASURE)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 15. Result of conversion (8 MSBs)	R	0x00

Table 8-87. BCICH0_LSB

Address Offset	0x57		
Physical Address	0x0000 0057	**Instance**	AUX_SCMADC
Description	Channel 0 BCI conversion result register (ADCIN1 = BTEMP)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 0. Result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-88. BCICH0_MSB

Address Offset	0x58		
Physical Address	0x0000 0058	**Instance**	AUX_SCMADC
Description	Channel 0 BCI conversion result register (ADCIN1 = BTEMP)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 0. Result of conversion (8 MSBs)	R	0x00

Table 8-89. BCICH1_LSB

Address Offset	0x59		
Physical Address	0x0000 0059	**Instance**	AUX_SCMADC
Description	Channel 1 BCI conversion result register (ADCIN8 = USBVBUS)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 1. Result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-90. BCICH1_MSB

Address Offset	0x5A		
Physical Address	0x0000 005A	**Instance**	AUX_SCMADC
Description	Channel 1 BCI conversion result register (ADCIN8 = USBVBUS)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 1. Result of conversion (8 MSBs)	R	0x00

Table 8-91. BCICH2_LSB

Address Offset	0x5B		
Physical Address	0x0000 005B	**Instance**	AUX_SCMADC
Description	Channel 2 BCI conversion result register (ADCIN10 = ICHG)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 2. Result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-92. BCICH2_MSB

Address Offset	0x5C		
Physical Address	0x0000 005C	**Instance**	AUX_SCMADC
Description	Channel 2 BCI conversion result register (ADCIN10 = ICHG).		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 2. Result of conversion (8 MSBs)	R	0x00

Table 8-93. BCICH3_LSB

Address Offset	0x5D		
Physical Address	0x0000 005D	**Instance**	AUX_SCMADC
Description	Channel 3 BCI conversion result register (ADCIN11 = VCHG).		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 3. Result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-94. BCICH3_MSB

Address Offset	0x5E		
Physical Address	0x0000 005E	**Instance**	AUX_SCMADC
Description	Channel 3 BCI conversion result register (ADCIN11 = VCHG)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 3. Result of conversion (8 MSBs)	R	0x00

Table 8-95. BCICH4_LSB

Address Offset	0x5F		
Physical Address	0x0000 005F	**Instance**	AUX_SCMADC
Description	Channel 4 BCI conversion result register (ADCIN12 = VBAT)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RSVD5	RSVD4	RSVD3	RSVD2	RSVD1	RSVD0

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 4. Result of conversion (2 LSBs)	R	0x0
5	RSVD5	Reserved. Read returns 0.	Reserved	0
4	RSVD4	Reserved. Read returns 0.	Reserved	0
3	RSVD3	Reserved. Read returns 0.	Reserved	0
2	RSVD2	Reserved. Read returns 0.	Reserved	0
1	RSVD1	Reserved. Read returns 0.	Reserved	0
0	RSVD0	Reserved. Read returns 0.	Reserved	0

Table 8-96. BCICH4_MSB

Address Offset	0x60		
Physical Address	0x0000 0060	**Instance**	AUX_SCMADC
Description	Channel 4 BCI conversion result register (ADCIN12 = VBAT)		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 4. Result of conversion (8 MSBs)	R	0x00

Table 8-97. MADC_ISR1

Address Offset	0x61		
Physical Address	0x0000 0061	**Instance**	AUX_SCMADC
Description	Interrupt status ISR1 register Determines which end-of-sequence (RT, SW1, SW2, or USB) triggered the interrupt line po_madc_p1_n request. When a bit in this register is set to 1, the corresponding end of sequence is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the interrupt status ISR1 register. When a bit in this register is set to 1, the corresponding interrupt line is released. If the user writes 0 to a bit in this register, the value does not change. The interrupt status ISR1 register is synchronous with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
RSVD4	RSVD3	RSVD2	RSVD1	USB_ISR1	SW2_ISR1	SW1_ISR1	RT_ISR1

Bits	Field Name	Description	Type	Reset
7	RSVD4	Reserved. Read returns 0.	Reserved	0
6	RSVD3	Reserved. Read returns 0.	Reserved	0
5	RSVD2	Reserved. Read returns 0.	Reserved	0
4	RSVD1	Reserved. Read returns 0.	Reserved	0

Bits	Field Name	Description	Type	Reset
3	USB_ISR1	0: Interrupt not set 1: Interrupt set	RW	0
2	SW2_ISR1	0: Interrupt not set 1: Interrupt set	RW	0
1	SW1_ISR1	0: Interrupt not set 1: Interrupt set	RW	0
0	RT_ISR1	0: Interrupt not set 1: Interrupt set	RW	0

Table 8-98. MADC_IMR1

Address Offset	0x62		
Physical Address	0x0000 0062	**Instance**	AUX_SCMADC
Description	Interrupt mask IMR1 register This register lets the user mask the expected transition on end of sequence from generating an interrupt request on po_madc_p1_n . The interrupt mask registers are programmed synchronously with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
RSVD4	RSVD3	RSVD2	RSVD1	USB_IMR1	SW2_IMR1	SW1_IMR1	RT_IMR1

Bits	Field Name	Description	Type	Reset
7	RSVD4	Reserved. Read returns 0.	R	0
6	RSVD3	Reserved. Read returns 0.	R	0
5	RSVD2	Reserved. Read returns 0.	R	0
4	RSVD1	Reserved. Read returns 0.	R	0
3	USB_IMR1	0: Interrupt not masked 1: Interrupt is masked	RW	1
2	SW2_IMR1	0: Interrupt not masked 1: Interrupt is masked	RW	1
1	SW1_IMR1	0: Interrupt not masked 1: Interrupt is masked	RW	1
0	RT_IMR1	0: Interrupt not masked 1: Interrupt is masked	RW	1

Table 8-99. MADC_ISR2

Address Offset	0x63		
Physical Address	0x0000 0063	**Instance**	AUX_SCMADC
Description	Interrupt status ISR2 register Determines which end-of-sequence (RT, SW1, SW2, or USB) triggered the interrupt line po_madc_p2_n request. When a bit in this register is set to 1, the corresponding end of sequence is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the interrupt status ISR2 register. When a bit in this register is set to 1, the corresponding interrupt line is released. If the user writes 0 to a bit in this register, the value does not change. The interrupt status ISR2 register is synchronous with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
RSVD4	RSVD3	RSVD2	RSVD1	USB_ISR2	SW2_ISR2	SW1_ISR2	RT_ISR2

Bits	Field Name	Description	Type	Reset
7	RSVD4	Reserved. Read returns 0.	Reserved	0
6	RSVD3	Reserved. Read returns 0.	Reserved	0
5	RSVD2	Reserved. Read returns 0.	Reserved	0
4	RSVD1	Reserved. Read returns 0.	Reserved	0

Bits	Field Name	Description	Type	Reset
3	USB_ISR2	0: Interrupt not set 1: Interrupt set	RW	0
2	SW2_ISR2	0: Interrupt not set 1: Interrupt set	RW	0
1	SW1_ISR2	0: Interrupt not set 1: Interrupt set	RW	0
0	RT_ISR2	0: Interrupt not set 1: Interrupt set	RW	0

Table 8-100. MADC_IMR2

Address Offset	0x64		
Physical Address	0x0000 0064	**Instance**	AUX_SCMADC
Description	Interrupt mask IMR2 register This register lets the user mask the expected transition on end of sequence from generating an interrupt request on po_madc_p2_n. The interrupt mask IMR2 register is programmed synchronously with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
RSVD4	RSVD3	RSVD2	RSVD1	USB_IMR2	SW2_IMR2	SW1_IMR2	RT_IMR2

Bits	Field Name	Description	Type	Reset
7	RSVD4	Reserved. Read returns 0.	R	0
6	RSVD3	Reserved. Read returns 0.	R	0
5	RSVD2	Reserved. Read returns 0.	R	0
4	RSVD1	Reserved. Read returns 0.	R	0
3	USB_IMR2	0: Interrupt not masked 1: Interrupt is masked	RW	1
2	SW2_IMR2	0: Interrupt not masked 1: Interrupt is masked	RW	1
1	SW1_IMR2	0: Interrupt not masked 1: Interrupt is masked	RW	1
0	RT_IMR2	0: Interrupt not masked 1: Interrupt is masked	RW	1

Table 8-101. MADC_SIR

Address Offset	0x65		
Physical Address	0x0000 0065	**Instance**	AUX_SCMADC
Description	MADC software interrupt register (for testing) This register provides the generation of an interrupt event on the madc_int1_n or madc_int2_n request line by writing 1 to the targeted SIR bit in a specific test mode. An interrupt is generated if the corresponding MADC_EDR bit is set to edge (falling or rising) sensitive. External interrupt requests and internal software requests are merged before being sent to the PIH.		
Type	RW		

7	6	5	4	3	2	1	0
RSVD4	RSVD3	RSVD2	RSVD1	USB_ISR2	SW2_ISR2	SW1_ISR2	RT_ISR2

Bits	Field Name	Description	Type	Reset
7	RSVD4	Reserved. Read returns 0.	Reserved	0
6	RSVD3	Reserved. Read returns 0.	Reserved	0
5	RSVD2	Reserved. Read returns 0.	Reserved	0
4	RSVD1	Reserved. Read returns 0.	Reserved	0

Bits	Field Name	Description	Type	Reset
3	USB_ISR2	0: Interrupt not set 1: Interrupt set	RW	0
2	SW2_ISR2	0: Software interrupt not set 1: Software interrupt set	RW	0
1	SW1_ISR2	0: Software interrupt not set 1: Software interrupt set	RW	0
0	RT_ISR2	0: Software interrupt not set 1: Software interrupt set	RW	0

Table 8-102. MADC_EDR

Address Offset	0x66		
Physical Address	0x0000 0066	**Instance**	AUX_SCMADC
Description	Interrupt edge detection register MADC_EDR This register lets the user define, for all signals, the end of RT sequence, end of SW1 sequence, end of SW2 sequence, and end of USB sequence, the edge expected to trigger an interrupt request. The interrupt request can be generated from a high- to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions (bits are 11) accruing. To get falling-edge detection capability, the relevant bits corresponding to the MADC must be reset (55).		
Type	RW		

7	6	5	4	3	2	1	0
USB_EDRRISING	USB_EDRFALLING	SW2_EDRRISING	SW2_EDRFALLING	SW1_EDRRISING	SW1_EDRFALLING	RT_EDRRISING	RT_EDRFALLING

Bits	Field Name	Description	Type	Reset
7	USB_EDRRISING	0: Rising detection disabled 1: Rising detection enabled	RW	0
6	USB_ EDRFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	1
5	SW2_EDRRISING	0: Rising detection disabled 1: Rising detection enabled	RW	0
4	SW2_ EDRFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	1
3	SW1_EDRRISING	0: Rising detection disabled 1: Rising detection enabled	RW	0
2	SW1_ EDRFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	1
1	RT_EDRRISING	0: Rising detection disabled 1: Rising detection enabled	RW	0
0	RT_EDRFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	1

Table 8-103. MADC_SIH_CTRL

Address Offset	0x67		
Physical Address	0x0000 0067	**Instance**	AUX_SCMADC
Description	MADC SIH control register This register lets the user disable a pending event incoming during software interrupt latency by programming 1 in the PENDDIS bit. By writing 0 in the EXCLEN bit, the user disables exclusivity between interrupt request lines madc_int1_n and madc_int2_n.The Clear on Read bit enables the Clear on Read feature. This means that any read access to the ISR clears this register and releases the associated interrupt line (default value). If disabled, a read access to a specific address value clears all ISRs in the SIH.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	COR	PENDDIS	EXCLEN

Bits	Field Name	Description	Type	Reset
7	Reserved	Read returns 0.	R	0
6	Reserved	Read returns 0.	R	0
5	Reserved	Read returns 0.	R	0
4	Reserved	Read returns 0.	R	0
3	Reserved	Read returns 0.	R	0
2	COR	0: Clear ISR-specific bit field when write access. 1: Clear ISR on read.	RW	1
1	PENDDIS	0: Pending event enabled 1: Pending event disabled	RW	1
0	EXCLEN	0: Exclusivity disabled 1: Exclusivity enabled	RW	1

Keypad Controller

This chapter describes the keypad controller of the device integrated power management/audio coder/decoder (codec) device.

Topic **Page**

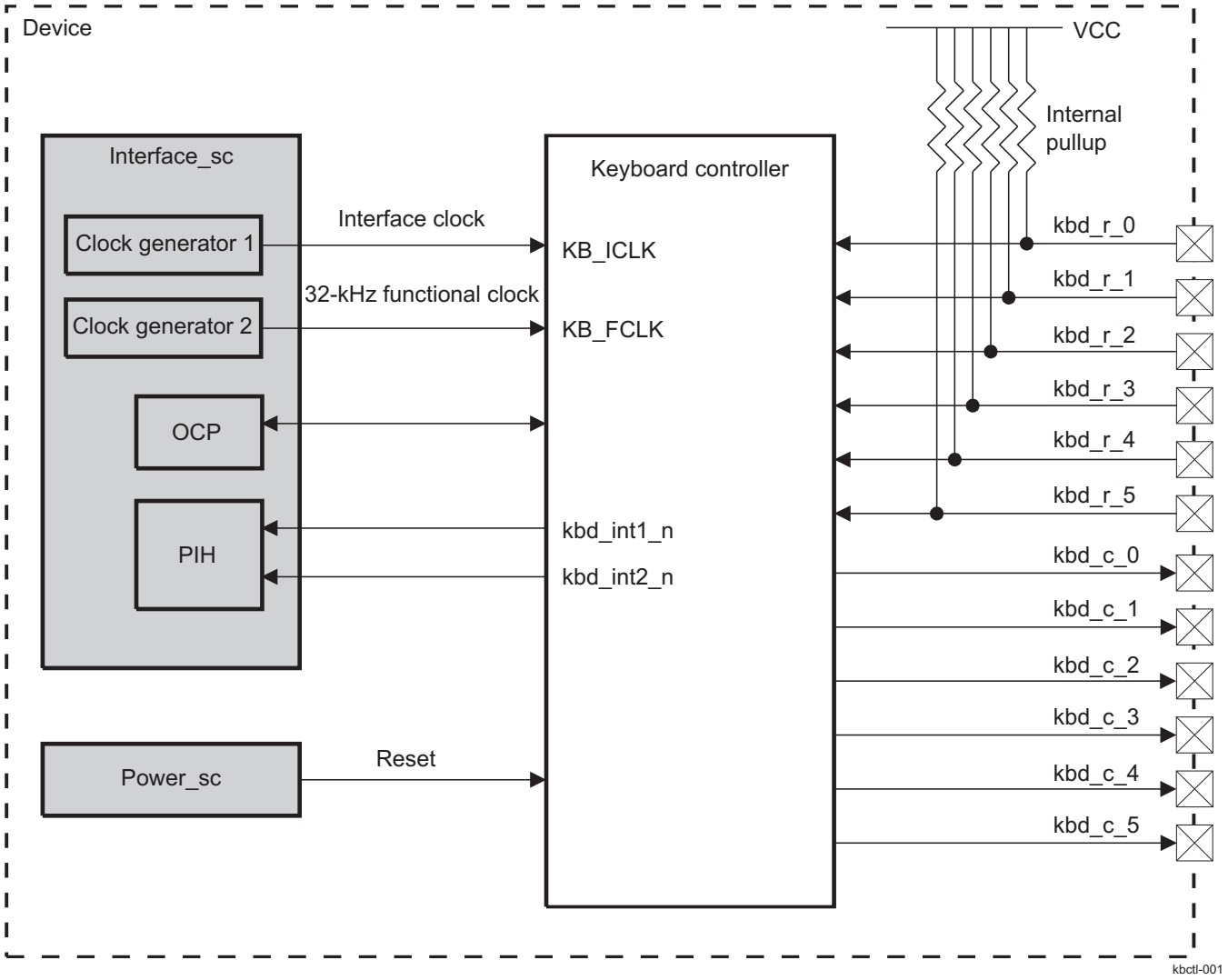
9.1 Keypad Controller Overview

The keypad controller implements a built-in scanning algorithm to decode hardware-based key presses and to reduce software use.

The device keypad controller can handle up to 6 x 6 keypads. It works on a 32-kHz clock in all possible modes of the device. It can generate wake-up events when the device is in sleep mode.

Figure 9-1 is an overview of the device keypad controller.

Figure 9-1. Device Keypad Controller Overview



The keypad controller has the following main features:

- Support of multiconfiguration keypads, up to 6 rows x 6 columns
- Integrated programmable timer
- Programmable interrupt generation on key events
- Event detection on key press and key release
- Multikey press detection and decoding
- Long-key detection on prolonged key press
- Programmable time-out on permanent key press or after keypad release

9.2 Keypad Controller Environment

9.2.1 Keypad Controller Functional Interface

Figure 9-2 shows a typical 8 x 8 keypad connection to the device keypad controller.

The columns keyp_c_0 to keyp_c_5 are open-drain outputs. The rows keyp_r_0 to keyp_r_5 have internal pullup resistors.

Figure 9-2. Device Keypad Controller Environment

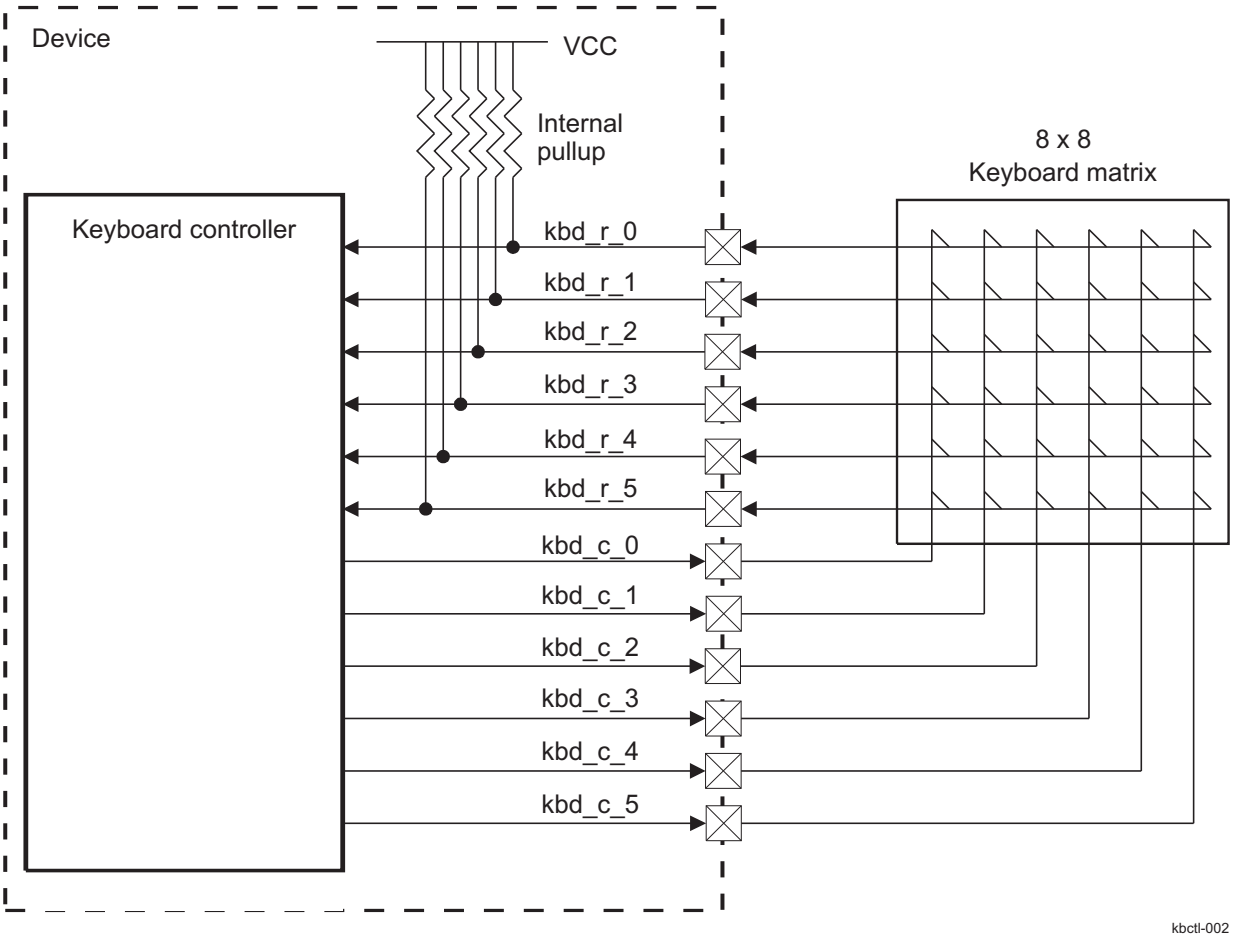


Table 9-1 lists and describes the keypad controller pins.

Table 9-1. Keypad Controller Inputs/Outputs (I/Os)

Signal Name	I/O (1)	Description	Value at Reset
keyp_r_0	I	Keypad matrix row 0 input	N/A
keyp_r_1	I	Keypad matrix row 1 input	N/A
keyp_r_2	I	Keypad matrix row 2 input	N/A
keyp_r_3	I	Keypad matrix row 3 input	N/A
keyp_r_4	I	Keypad matrix row 4 input	N/A
keyp_r_5	I	Keypad matrix row 5 input	N/A
keyp_c_0	O	Keypad matrix column 0 output	1
keyp_c_1	O	Keypad matrix column 1 output	1
keyp_c_2	O	Keypad matrix column 2 output	1
keyp_c_3	O	Keypad matrix column 3 output	1

(1) I = Input; O = Output

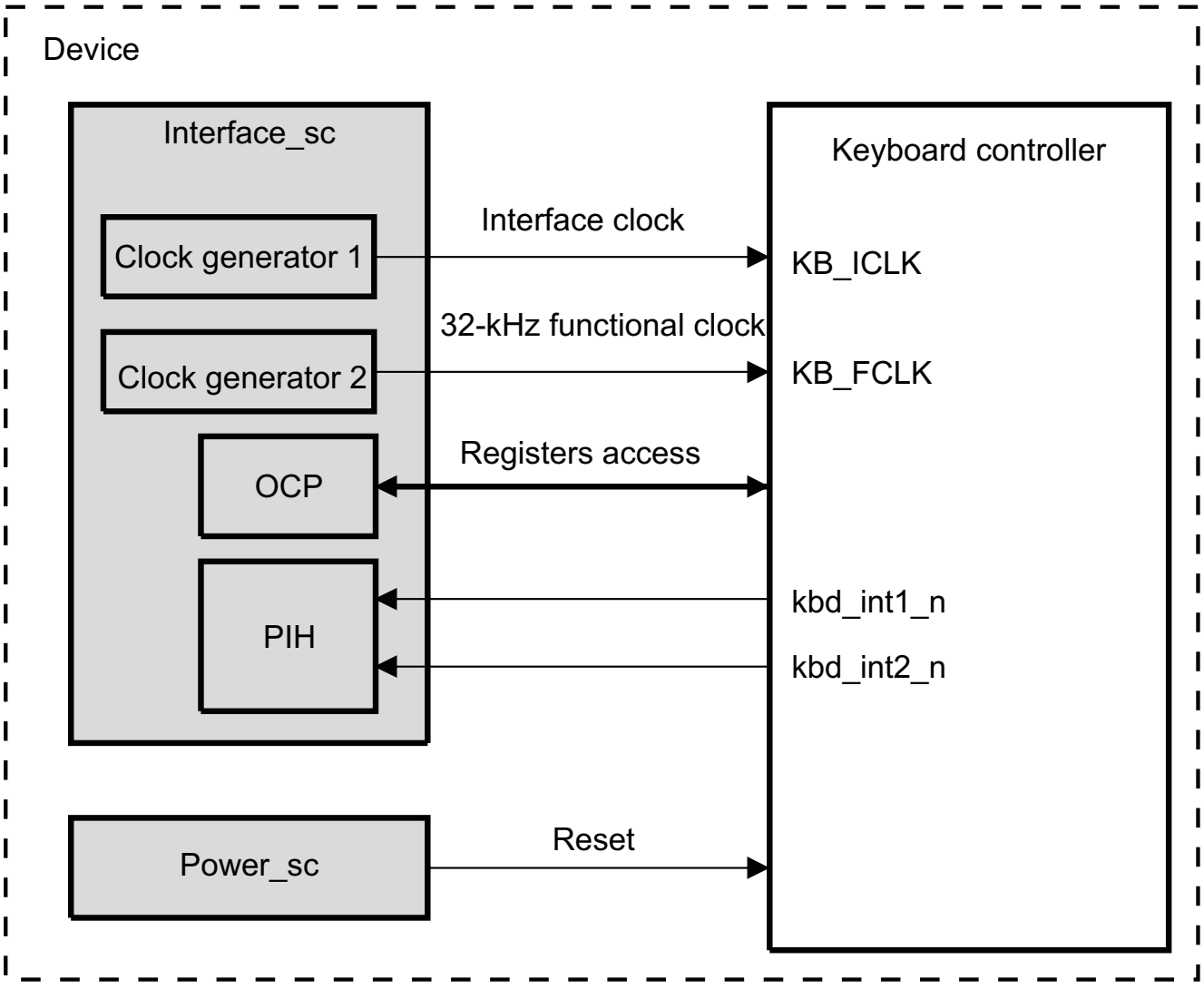
Table 9-1. Keypad Controller Inputs/Outputs (I/Os) (continued)

Signal Name	I/O [1]	Description	Value at Reset
keyp_c_4	O	Keypad matrix column 4 output	1
keyp_c_5	O	Keypad matrix column 5 output	1

9.3 Keypad Controller Integration

Figure 9-3 shows keypad controller integration in the device.

Figure 9-3. Device Keypad Controller Integration



026-003

9.3.1 Clock and Reset Scheme

9.3.1.1 Keypad Controller Clocks

There are two clock domains in the keypad controller: the functional clock domain and the interface clock domain.

- KEYP_FCLK belongs to the functional clock domain. It is a fixed 32-kHz clock provided by the clock generator, CKGEN. It clocks the internal module logic.

NOTE: The clk32k clock remains active when the chip is in sleep mode, thus allowing the keypad controller to generate a wake-up event. An interrupt can be generated to the primary interrupt handler (PIH) only when the KEYP_CTRL_REG[6] KBD_ON bit is set to 1.

- KEYP_ICLK is the interface clock. It triggers access to the keypad controller registers through the open-core protocol (OCP) bus.

  The source of KEYP_ICLK is the system clock.

9.3.1.2 Keypad Controller Reset Scheme

Global reset of the module is performed by setting the KEYP_CTRL_REG[0] SOFT_NRST bit to 0. This bit enables active software reset functionality equal to a hardware reset. The keypad module also has a hardware reset signal from the power subchip, keypad_reset_na.

9.3.2 Hardware Request

The keypad controller can generate two interrupt signals, KEYP_INT1_n and KEYP_INT2_n, and send them to the PI). The PIH sends these interrupts to external devices.

9.4 Keypad Controller Functional Description

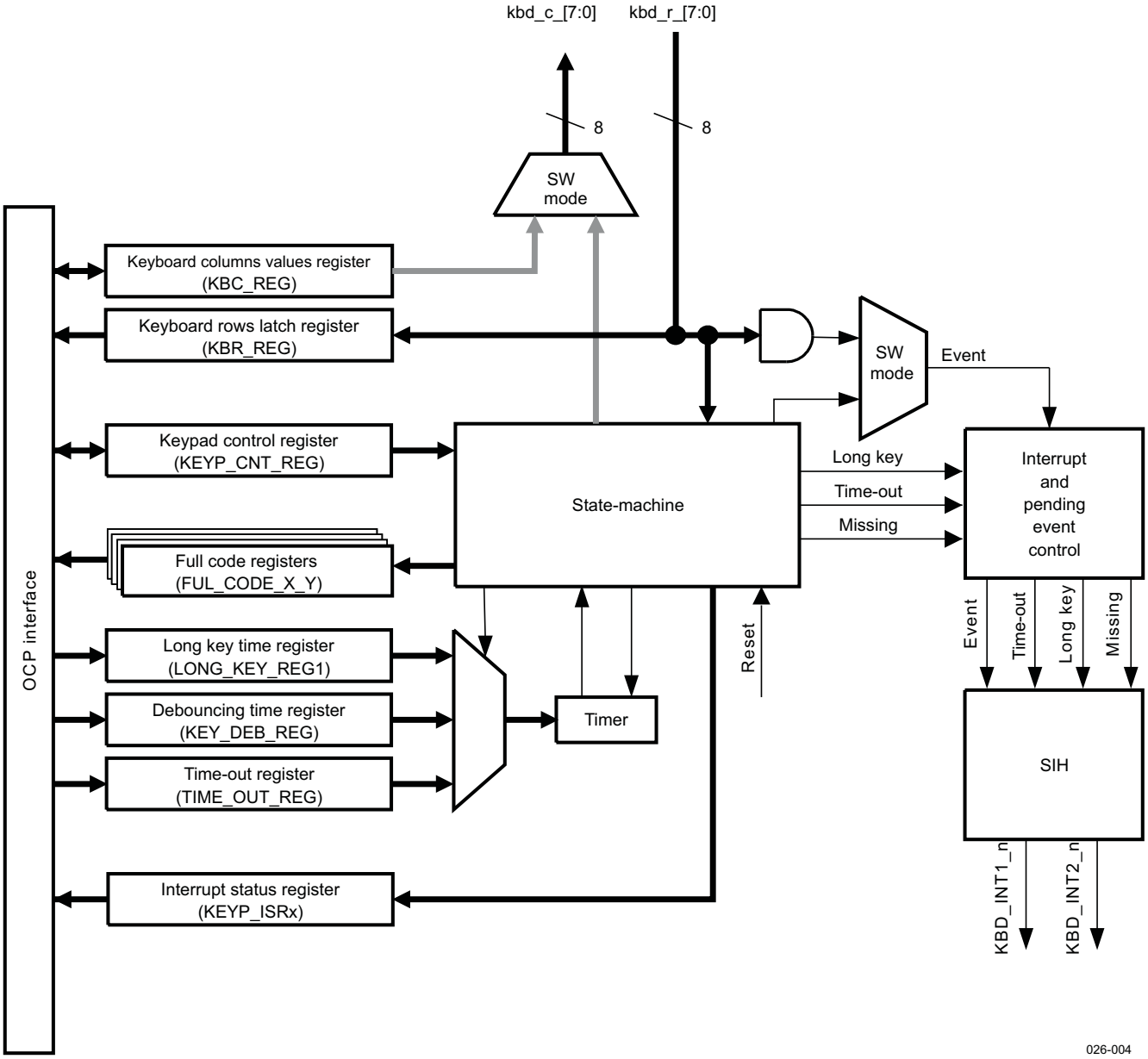
9.4.1 General Description

The keypad controller detects events issued on any key of the connected keypad and generates an interrupt to alert the host processor. In addition, the built-in hardware scan algorithm decodes pressed keys, including multikey combinations.

To reduce software overhead for the application processor, detecting and decoding are hardware-performed within the keypad controller state-machine. It is also possible to deactivate hardware decoding and handle the scanning algorithm with software.

Figure 9-4 is a block diagram of the keypad controller architecture.

Figure 9-4. Keypad Controller Block Diagram



9.4.2 Software Mode

The KEYP_CTRL_REG[1] SOFTMODEN bit allows selection of hardware decoding (activated by default after reset) or software mode.

In software mode, the keypad controller internal sequencer that performs automatic scanning and decoding processes is disabled. Consequently, the software must manually perform the scanning algorithm.

The software scan is performed using the KBC_REG and KBR_REG registers. The KBC_REG register sets the column output values, while the KBR_REG register reflects the row input values. At reset, all KBC_REG bits are 1 (default value). To enable the keypad matrix columns, the respective column register bit must be set to 0. The keypad module must be turned on before this by setting the KEYP_CTRL_REG[6] KBD_ON bit to 1.

Any key press connects a column output (driving a logical 0) to a row input (internally pulled up to a logical 1) and generates an interrupt (KEYP_INTx_n asserted low) to indicate that the software scan can start.

For more information about the software scan, see Section 9.5, *Programming Mode*.

9.4.3 Keypad Controller Hardware Decoding Mode

9.4.3.1 Functional Modes

When operating in the hardware decoding mode (the KEYP_CTRL_REG[1] SOFTMODEN bit is set to 1), the keypad controller offers several functional modes, summarized in Table 9-2.

Table 9-2. Keypad Controller Functional Modes

Functional Mode	Associated Interrupt	Associated Timer Value	Description	Control
Keypad event	Event IT	Debouncing value	Occurs when a key is pressed or released Always enabled	N/A, always active
Long key	Long-key IT	Long-key value	Detects a key that is pressed for a long time Must be associated with the long key time-out function	KEYP_CTRL_REG[2] LK_EN
Repeat key	Long-key IT	Long-key value	Generates an interrupt every long key delay No time-out can be associated.	KEYP_CTRL_REG[5] RP_EN
Empty time-out	Time-out IT	Empty time-out value	Interrupt generated if no key is pressed during an empty time-out period	KEYP_CTRL_REG[3] TOE_EN
Long key time-out	Time-out IT	Long-key time-out value	Associated with the long key function Generated after a long-key interrupt if no event occurs during a long key time-out period	KEYP_CTRL_REG[4] TOLE_EN

9.4.3.2 Keypad Controller Timer

As described in Section 9.4.3.1, *Functional Modes*, each functional mode is associated with a timer value. Depending on the selected mode, the keypad controller timer is loaded with the corresponding value as set in the related registers: KEY_DEB_REG, LONG_KEY_REG1, and TIME_OUT_REG.

Table 9-3 summarizes the keypad controller timer values.

Table 9-3. Keypad Controller Timer Values

Timer Value	Associated Bit Field	Description
Debouncing time	KEY_DEB_REG[5:0] KEYP_DEB	To remove the effects of glitches when an event occurs on the keypad, the controller waits a full debouncing period before taking a snapshot of the keypad matrix current state. The timer is loaded with the debouncing time value after each detected event on the keypad matrix. An event interrupt is generated after this delay.
Long key time	LONG_KEY_REG1[7:0] LSB_LK and LK_PTV_REG[3:0] MSB_LK	This is the delay before generating a long-key interrupt after an event interrupt. If long-key mode is selected, the timer is loaded with the long-key time value after an event interrupt is generated. In repeat mode, the timer is reloaded with the same value after a long-key interrupt and starts to count down again.
Long key time-out	TIME_OUT_REG1[7:0] LSB_TO TIME_OUT_REG2[7:0] MSB_TO	The timer is loaded with the time-out value. A long-key interrupt is generated and starts to count down. When it reaches 0, a time-out interrupt is generated and the keypad controller returns to IDLE state.
Empty key time-out	TIME_OUT_REG1[7:0] LSB_TO TIME_OUT_REG2[7:0] (MSB_TO)	If no key is pressed during this delay, the time-out interrupt occurs. The keypad controller then goes back to IDLE state.

Timer countdown period depends on three factors:

- The loaded value as set in the KEY_DEB_REG, LONG_KEY_REG1, and TIME_OUT_REG registers
- The prescale clock timer value as set in the LK_PTV_REG[7:5] PTV bit field. This programmable clock divider allows reducing the clock frequency used by the timer.
- The keypad controller functional clock frequency (32 kHz)

The period is calculated as follows:

$T_{period} = (T_{value} + 1) * (2^{(PTV + 1)}) * T_{clk}$

Where:

- T_{value} is the value stored in the KEY_DEB_REG, LONG_KEY_REG1, or TIME_OUT_REG register.
- PTV is the value of the LK_PTV_REG[7:5] PTV bit field.
- T_{clk} is the period of the 32-kHz functional clock (31.25 μs).

The timer value registers (KEY_DEB_REG and TIME_OUT_REG) can be updated at any time. When the KEY_DEB_REG or TIME_OUT_REG registers are updated, the new value is considered only at the next timer load. If the timer is already counting down when the registers are updated, the timer keeps counting down from the previous value and is loaded with the new one on the next load.

9.4.3.3 Keypad Controller Interrupt Generation

9.4.3.3.1 Interrupt Generation

There are two identical interrupt-generation modules (INT1 and INT2) in the secondary interrupt handler (SIH), which processes synchronous interrupt requests to be used independently in a biprocessor environment. Each module generates an interrupt, KEYP_INT1_n and KEYP_INT2_n, respectively. Each module controls its own synchronous interrupt request line and its own interrupt mask and interrupt status register.

The interrupt status registers (ISRs), KEYP_ISR1 and KEYP_ISR2, indicate the current status of the interrupt signals KEYP_INT1_n and KEYP_INT2_n, respectively. The registers are updated after a key-press event, a long-key-press event, or a time-out detection. Each interrupt bit can be cleared by a read access or a write access, depending on the value in the KEYP_SIH_CTRL[2] COR bit, which is described in the following paragraphs.

The interrupt mask registers (IMRs), KEYP_IMR1 and KEYP_IMR2, let the user mask the expected keypad transition on a keypad event from generating a keypad interrupt request on KEYP_INT1_n or KEYP_INT2_n, respectively. The IMR can mask a key-pressed event, a long-key-pressed event, and a time-out event to the interrupt line.

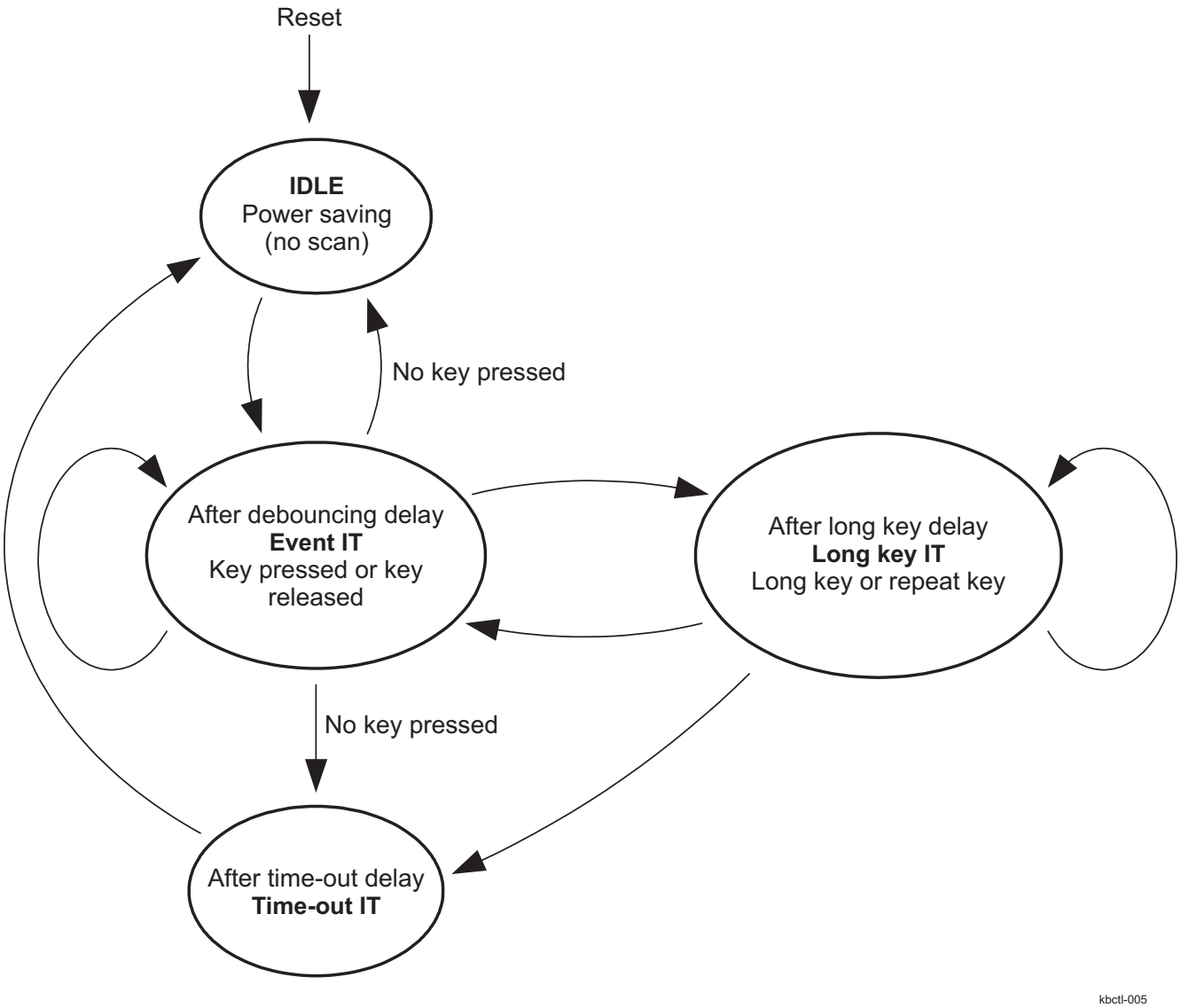
The interrupt edge detection register, KEYP_EDR, lets the user define for each keypad event the edge expected to trigger an interrupt request. Detection can be on the rising edge, the falling edge, or both edges. At reset, falling-edge detection is enabled.

The keypad control register, KEYP_SIH_CTRL, lets the user enable an incoming pending event during software interrupt latency by setting the KEYP_SIH_CTRL[1] PENDDIS bit to 0. Setting the PENDDIS bit to 1 disables the pending feature. The pending event is enabled at reset. Exclusivity can be enabled by setting the KEYP_SIH_CTRL[0] EXCLEN bit to 1, and disabled by setting the EXCLEN bit to 0. This feature is enabled at reset. The ISR can be configured to clear the interrupt on a read access or a write access by setting the KEYP_SIH_CTRL[2] COR bit to 1 or 0, respectively. Clear-on-write is enabled at reset.

NOTE: The software must clear the interrupt to ensure that the correct value corresponding to the last key pressed is available. There is no way to poll the registers to see if the interrupt has cleared.

Figure 9-5 shows the interrupt events generated in each keypad controller functional mode and details the relationships between them. Depending on the selected mode, some interrupt events cannot be generated.

Figure 9-5. Functional Modes and Related IT Events



When running in hardware decoding mode, the keypad controller performs automatic scans when it is not

in IDLE state. When a key press event occurs on the keypad matrix, the keypad controller leaves IDLE state and an interrupt event—ITKPISRx (KEYP_ISRx[0]) bit—is set after the timer counts down the debouncing delay. An interrupt event is generated as many times as a key is pressed or released. An interrupt event, ITKPISRx, is generated regardless of the selected functional mode. If no time-out is set and no more keys are pressed, the keypad controller returns to IDLE state.

If long-key detection mode is set, after the timer counts down the long key delay, an interrupt long key—ITLKISRx (KEYP_ISRx[1]) bit—is generated. This ITLKISRx interrupt is generated once. There is no pending event for the long key. A second ITLKISRx interrupt is sent only if the previous ITLKISRx interrupt was cleared.

A time-out can also be set in event-detection or long-key-detection mode. In this case, a time-out interrupt—ITTOIISRx (KEYP_ISRx[2]) bit—is generated after the time-out delay timer expires. After such an interrupt, the keypad controller always returns to IDLE state.

NOTE: In repeat mode, no time-out can be set. Only a keypad event can stop the periodic interrupt generation.

9.4.3.3.2 Keypad Buffer and Missed Events

A dedicated buffer lets the keypad controller memorize two successive events. If two successive events occur before a read is performed, the second event is stored and a second interrupt is generated when the first one is cleared, allowing two key events to be received in a row.

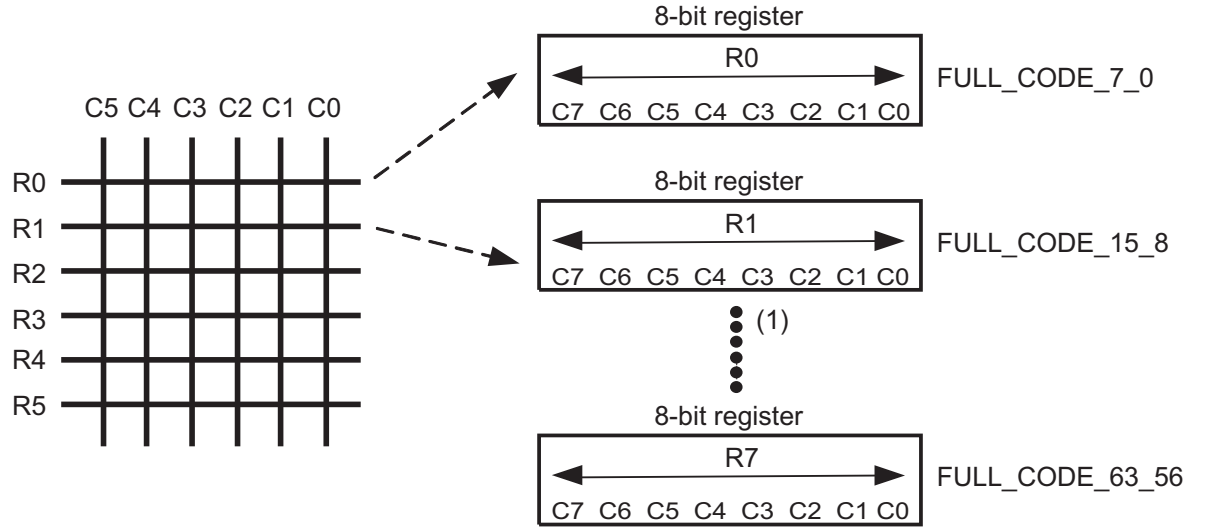
9.4.3.4 Keypad Controller Key Coding Registers

The keypad controller matrix-pressed-keys state (which columns/rows are connected) is reflected in the following registers:

- FULL_CODE_7_0
- FULL_CODE_15_8
- FULL_CODE_23_16
- FULL_CODE_31_24
- FULL_CODE_39_32
- FULL_CODE_47_40
- FULL_CODE_55_48
- FULL_CODE_63_56

Figure 9-6 shows the key coding registers.

Figure 9-6. Key Coding Registers



A The C6 and C7 bit positions and the R6 and R7 registers exist because in the TPS65950 design, the keypad can be up to 8 x 8. In the TPS65930 and TPS65920, pad access limits the keypad function to 6 x 6.

Each register stores the state of a keypad row. For a given row, each bit corresponds to a keypad column. For example, bit 0 corresponds to column 0 and row 0 key, bit 1 corresponds to column 1 and row 0 key. A bit set to 1 means that the corresponding key is pressed.

NOTE: With a small keypad (for example, 7 x 7 or 6 x 6), some bits are not used.

9.5 Programming Model

9.5.1 Using the Keypad Controller in Software Scanning Mode

To deactivate the internal keypad controller sequencer and use the module in software mode, ensure that the following steps are performed:

1. Set the KEYP_CTRL_REG[1] SOFTMODEN bit to 0 (this is not the default mode after reset).
2. Enable the interrupt setting using the interrupt mask register KEYP_IMRx. This allows KEYP_INTx_n interrupt signal assertion on a key press/release event on the keypad matrix.
3. After the KEYP_INTx_n is generated, indicating an event on the keys, the software scan begins:
   (a) Disable all the columns to drive a logical 1 on the keyp_c_[7:0] outputs by setting KBC_REG[7:0] to 0x0.
   (b) Enable the first column to set the corresponding bit to 1 in the KBC_REG register.
   (c) Read the KBR_REG register. A 0 read in the KBR_REG register means that the corresponding row is connected to the column being enabled.
   (d) Repeat Steps b and c for all columns.

NOTE: In software mode, an interrupt is generated when the keypad status goes from no key pressed to one or more keys pressed. No new interrupt is generated if a key is already pressed.

9.5.2 Using the Keypad Controller in Hardware Decoding Mode (Default Setting)

The hardware mode is the default mode after reset (the SOFTMODEN bit set to 1).

1. Select the functional mode.

After reset, all functional modes are disabled, except detect event mode, which is always active. To activate a functional mode, set the corresponding bit to 1 in the KEYP_CTRL_REG register:

- The KEYP_CTRL_REG[2] LK_EN bit activates/deactivates long-key detection mode.
- The KEYP_CTRL_REG[3] TOE_EN bit activates/deactivates empty time-out mode.
- The KEYP_CTRL_REG[4] TOLE_EN bit activates/deactivates long-key time-out mode.
- The KEYP_CTRL_REG[5] RP_EN bit activates/deactivates repeat mode.

NOTE: Because long-key-detection mode and repeat mode share the same interrupt status bit and are mutually exclusive, they cannot be used simultaneously. The software must ensure that only one of these modes is selected at a time.

2. Set the timer periods. For more information about timer programming, see Section 9.5.3, *Using the Timer*.

   The combination of the the LONG_KEY_REG1[7:0] MSB_LK and LK_PTV_REG[3:0] LSB_LK bit fields is used in long-key-detection and repeat modes. In long-key-detection mode, the bit field determines the delay required to consider a key press a long press. In repeat mode, the register field sets the recursive interrupt period.

   The TIME_OUT_REG1[7:0] LSB_TO and TIME_OUT_REG2[7:0] MSB_TO bit fields are used for empty time-out and long-key time-out modes. The same value is applied when the two modes are enabled.

   The KEY_DEB_REG[5:0] KEYP_DEB bit field is used with any selected functional mode. The debouncing countdown is launched after any key event (key pressed or released).
3. Configure the keypad controller interrupt line.

   Each functional mode generates a dedicated interrupt bit logged in the ISR KEYP_ISRx register. To activate the interrupt line and trigger KEYP_INTx_n on one or more of these events, the corresponding bit in the IMR must be set to 0.

NOTE: After reset, all interrupt lines are masked.

After configuration, the keypad controller is ready to operate. To decode any event on the keypad:

1. Wait for KEYP_INTx_n to be asserted.
   Regardless of mode, any event on the keypad matrix generates an interrupt, ITKPISRx (the ITKPISRx bit set to 1). The selected mode(s) determines whether the other bits are set.
2. Read the KEYP_ISRx register to determine which event caused the interrupt.
3. To determine which keys were pressed, read the following registers:
   - FULL_CODE_7_0
   - FULL_CODE_15_8
   - FULL_CODE_23_16
   - FULL_CODE_17_24
   - FULL_CODE_31_24
   - FULL_CODE_39_32
   - FULL_CODE_47_55
   - FULL_CODE_63_56
4. Depending on the KEYP_SIH_CTRL[2] COR bit, the interrupt is cleared on a read or write operation.

9.5.3 Using the Timer

As described in Section 9.4.3.2, *Keypad Controller Timer*, the keypad controller timer is loaded with the content of the KEY_DEB_REG, LONG_KEY_REG1, or TIME_OUT_REG register, depending on the selected mode and the state of the internal sequencer.

Countdown time is calculated as follows:

$T_{period} = (T_{value} + 1) * (2^{(PTV + 1)}) * T_{clk}$

The LK_PTV_REG[7:5] PTV bit field lets the timer clock be predivided. Table 9-4 shows the divider rates.

Table 9-4. Timer Prescale Values

CNTL[4:2] PTV Value	Divisor
0	2
1	4
2	8
3	16
4	31
5	64
6	128
7	256

CAUTION

To avoid undefined results, the LK_PTV_REG[7:5] PTV bit field must not be changed when the timer is running.

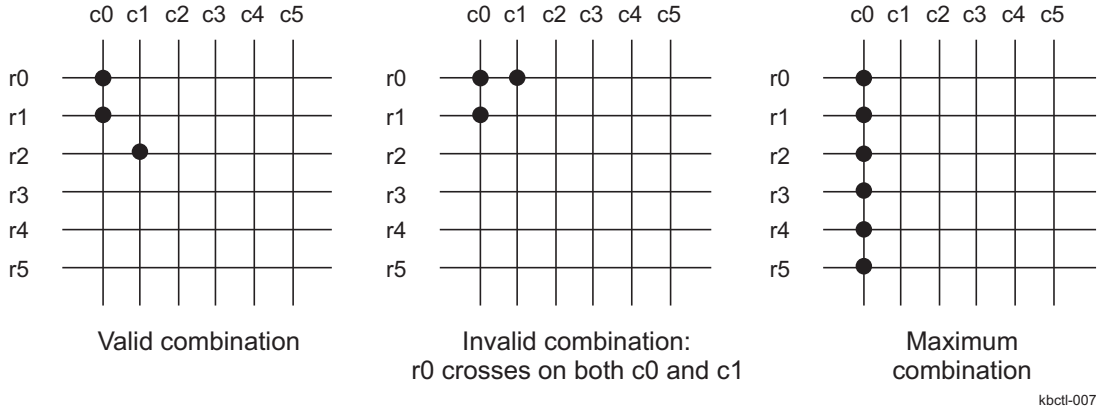
9.5.4 Multikey Limitations

The keypad controller can detect and decode multikey combinations, but the following rules must be followed:

1. Any 2-key combination is valid and can be decoded.
2. Combinations using more than two keys are valid only if the rows and columns used do not cross over on another key to detect. This is the result of equipotent propagation on a row/column.

Figure 9-7 shows examples of a valid 3-key combination, an invalid 3-key combination, and the largest combination allowed for an 8 x 8 keypad.

Figure 9-7. Multikey Limitation Example



9.5.5 Using the Keypad Controller With a Small Keypad

When using the keypad controller with a small keypad (for example, 5 x 5), unused rows must be tied high to prevent disturbing the scanning process.

9.6 Registers

This section summarizes the registers used for the configuration of the keypad controller.

Table 9-5. Instance Summary

Module Name	Base Address	Size
KEYPAD	0x0000 00D2	24 bytes

9.6.1 Keypad Controller Register Mapping Summary

This section provides information about the keypad module instance. The registers in the module instance are described separately in Table 9-7 through Table 9-30.

Table 9-6. Keypad Controller Register Address

Register Name	Type	Register Width (Bits)	Physical Address
KEYP_CTRL_REG	RW	8	0x0000 00D2
KEY_DEB_REG	RW	8	0x0000 00D3
LONG_KEY_REG1	RW	8	0x0000 00D4
LK_PTV_REG	RW	8	0x0000 00D5
TIME_OUT_REG1	RW	8	0x0000 00D6
TIME_OUT_REG2	RW	8	0x0000 00D7
KBC_REG	RW	8	0x0000 00D8
KBR_REG	R	8	0x0000 00D9
KEYP_SMS	R	8	0x0000 00DA
FULL_CODE_7_0	R	8	0x0000 00DB
FULL_CODE_15_8	R	8	0x0000 00DC
FULL_CODE_23_16	R	8	0x0000 00DD
FULL_CODE_31_24	R	8	0x0000 00DE
FULL_CODE_39_32	R	8	0x0000 00DF
FULL_CODE_47_40	R	8	0x0000 00E0
FULL_CODE_55_48	R	8	0x0000 00E1
FULL_CODE_63_56	R	8	0x0000 00E2
KEYP_ISR1	RW	8	0x0000 00E3
KEYP_IMR1	RW	8	0x0000 00E4
KEYP_ISR2	RW	8	0x0000 00E5
KEYP_IMR2	RW	8	0x0000 00E6
KEYP_SIR	RW	8	0x0000 00E7
KEYP_EDR	RW	8	0x0000 00E8
KEYP_SIH_CTRL	RW	8	0x0000 00E9

9.6.2 Register Descriptions

Table 9-7. KEYP_CTRL_REG

Address Offset	0x00		
Physical Address	0x0000 00D2	**Instance**	AUX_SCkeypad
Description	This keypad control register controls keypad mode (software/hardware decoding mode) and event mode detection (long key/time-out/repeat). KBD_ON powers on the keypad by requesting the required functional clock.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	KBD_ON	RP_EN	TOLE_EN	TOE_EN	LK_EN	SOFTMODEN	SOFT_NRST

Bits	Field Name	Description	Type	Reset
7	Reserved	Read returns 0.	R	0
6	KBD_ON	When the KBD_ON bit is set to 1, the keypad requests the 32-kHz functional clock and then starts to run.	RW	0
5	RP_EN	1 enables repeat mode detection.	RW	0
4	TOLE_EN	1 enables long-key time-out detection.	RW	0
3	TOE_EN	1 enables time-out empty detection.	RW	0
2	LK_EN	1 enables long-key process detection.	RW	0
1	SOFTMODEN	0x0: Enable software mode using kbr_latch_reg and kbc_reg. Configure SIH to receive kbr AND. 0x1: Hardware decoding using internal sequencer	RW	1
0	SOFT_NRST	0x0: Reset 0x1: Normal operation	RW	1

Table 9-8. KEY_DEB_REG

Address Offset	0x01		
Physical Address	0x0000 00D3	**Instance**	AUX_SCkeypad
Description	The value written to this register corresponds to the value for debouncing time.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED		KEYP_DEB					

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Read returns 0.	R	0x0
5:0	KEYP_DEB	Debouncing time preset value	RW	0x00

Table 9-9. LONG_KEY_REG1

Address Offset	0x02		
Physical Address	0x0000 00D4	**Instance**	AUX_SCkeypad
Description	The value written to this register corresponds to the LSB value of the long-key interrupt or repeat mode value.		
Type	RW		

7	6	5	4	3	2	1	0
LSB_LK							

Bits	Field Name	Description	Type	Reset
7:0	LSB_LK	Long-key LSB preset value	RW	0x00

Table 9-10. LK_PTV_REG

Address Offset	0x03		
Physical Address	0x0000 00D5	**Instance**	AUX_SCkeypad
Description	The value written to this register bit field 3:0 corresponds to the MSB value of the long-key interrupt or repeat mode value. The value written to bit field 7:5 corresponds to the prescaler timer value.		
Type	RW		

7	6	5	4	3	2	1	0
PTV			RESERVED	MSB_LK			

Bits	Field Name	Description	Type	Reset
7:5	PTV	Prescaler timer value	RW	0x7
4	Reserved	Read returns 0.	R	0
3:0	MSB_LK	Long-key MSB preset value	RW	0x0

Table 9-11. TIME_OUT_REG1

Address Offset	0x04		
Physical Address	0x0000 00D6	**Instance**	AUX_SCkeypad
Description	The value written to this register corresponds to the LSB value of the time-out interrupt.		
Type	RW		

7	6	5	4	3	2	1	0
LSB_TO							

Bits	Field Name	Description	Type	Reset
7:0	LSB_TO	Time-out LSB preset value	RW	0x00

Table 9-12. TIME_OUT_REG2

Address Offset	0x05		
Physical Address	0x0000 00D7	**Instance**	AUX_SCkeypad
Description	The value written to this register corresponds to the MSB value of the time-out interrupt.		
Type	RW		

7	6	5	4	3	2	1	0
MSB_TO							

Bits	Field Name	Description	Type	Reset
7:0	MSB_TO	Time-out MSB preset value	RW	0x00

Table 9-13. KBC_REG

Address Offset	0x06		
Physical Address	0x0000 00D8	**Instance**	AUX_SCkeypad
Description	This register manages the scanning sequence in software sequencing mode. The register values drive the output column pins.		
Type	RW		

7	6	5	4	3	2	1	0
KBC7 − KBC0							

Bits	Field Name	Description	Type	Reset
7	KBC7	Drives the KBC7 output pin	RW	1
6	KBC6	Drives the KBC6 output pin	RW	1
5	KBC5	Drives the KBC5 output pin	RW	1
4	KBC4	Drives the KBC4 output pin	RW	1
3	KBC3	Drives the KBC3 output pin	RW	1
2	KBC2	Drives the KBC2 output pin	RW	1
1	KBC1	Drives the KBC1 output pin	RW	1
0	KBC0	Drives the KBC0 output pin	RW	1

Table 9-14. KBR_REG

Address Offset	0x07		
Physical Address	0x0000 00D9	**Instance**	AUX_SCkeypad
Description	This register manages the decoding sequence in software sequencing mode and samples the row input line in this mode.		
Type	R		

7	6	5	4	3	2	1	0
KBR7 − KBR0							

Bits	Field Name	Description	Type	Reset
7	KBR7	Reflects the KBR7 input pin	R	1
6	KBR6	Reflects the KBR6 input pin	R	1
5	KBR5	Reflects the KBR5 input pin	R	1
4	KBR4	Reflects the KBR4 input pin	R	1
3	KBR3	Reflects the KBR3 input pin	R	1
2	KBR2	Reflects the KBR2 input pin	R	1
1	KBR1	Reflects the KBR1 input pin	R	1
0	KBR0	Reflects the KBR0 input pin	R	1

Table 9-15. KEYP_SMS

Address Offset	0x08		
Physical Address	0x0000 00DA	**Instance**	AUX_SCkeypad
Description	This test register indicates the current status of the sequencer state-machine, and enables SIR test mode of the instantiated SIH.		
Type	R		

7	6	5	4	3	2	1	0
RESERVED		MISS_EN	SIR_EN	STMSTS			

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Read returns 0.	R	0x0
5	MISS_EN	1 enables missed-event detection.	RW	0
4	SIR_EN	1 enables the SIH test mode (SIR).	RW	0
3:0	STMSTS	Read 0x0: Idle Read 0x1: Scanning Read 0x2: Load timer debouncing Read 0x3: Test timer debouncing Read 0x4: Gen IT event Read 0x6: Load timer long key Read 0x7: Test timer long key Read 0x8: Gen IT long key Read 0xA: Test timer time-out Read 0xB: Gen IT time-out Read 0xD: Load timer time-out Read 0xF: Other	R	0x0

Table 9-16. FULL_CODE_7_0

Address Offset	0x09		
Physical Address	0x0000 00DB	**Instance**	AUX_SCkeypad
Description	This register is updated when any key (in the range 0:7) is pressed. A bit at 1 indicates that the corresponding key is pressed.		
Type	R		

7	6	5	4	3	2	1	0
FULL_CODE_K7 − FULL_CODE_K0							

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K7	1 indicates that key 7 is pressed.	R	0
6	FULL_CODE_K6	1 indicates that key 6 is pressed.	R	0
5	FULL_CODE_K5	1 indicates that key 5 is pressed.	R	0
4	FULL_CODE_K4	1 indicates that key 4 is pressed.	R	0
3	FULL_CODE_K3	1 indicates that key 3 is pressed.	R	0
2	FULL_CODE_K2	1 indicates that key 2 is pressed.	R	0
1	FULL_CODE_K1	1 indicates that key 1 is pressed.	R	0
0	FULL_CODE_K0	1 indicates that key 0 is pressed.	R	0

Table 9-17. FULL_CODE_15_8

Address Offset	0x0A		
Physical Address	0x0000 00DC	**Instance**	AUX_SCkeypad
Description	This register is updated when any key (in the range 8:15) is pressed. A bit at 1 indicates that the corresponding key is pressed.		
Type	R		

7	6	5	4	3	2	1	0
FULL_CODE_K15 − FULL_CODE_K8							

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K15	1 indicates that key 15 is pressed.	R	0
6	FULL_CODE_K14	1 indicates that key 14 is pressed.	R	0
5	FULL_CODE_K13	1 indicates that key 13 is pressed.	R	0
4	FULL_CODE_K12	1 indicates that key 12 is pressed.	R	0
3	FULL_CODE_K11	1 indicates that key 11 is pressed.	R	0
2	FULL_CODE_K10	1 indicates that key 10 is pressed.	R	0
1	FULL_CODE_K9	1 indicates that key 9 is pressed.	R	0
0	FULL_CODE_K8	1 indicates that key 8 is pressed.	R	0

Table 9-18. FULL_CODE_23_16

Address Offset	0x0B		
Physical Address	0x0000 00DD	**Instance**	AUX_SCkeypad
Description	This register is updated when any key (in the range 16:23) is pressed. A bit at 1 indicates that the corresponding key is pressed.		
Type	R		

7	6	5	4	3	2	1	0
FULL_CODE_K23 − FULL_CODE_K16							

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K23	1 indicates that key 23 is pressed.	R	0
6	FULL_CODE_K22	1 indicates that key 22 is pressed.	R	0
5	FULL_CODE_K21	1 indicates that key 21 is pressed.	R	0
4	FULL_CODE_K20	1 indicates that key 20 is pressed.	R	0
3	FULL_CODE_K19	1 indicates that key 19 is pressed.	R	0
2	FULL_CODE_K18	1 indicates that key 18 is pressed.	R	0
1	FULL_CODE_K17	1 indicates that key 17 is pressed.	R	0
0	FULL_CODE_K16	1 indicates that key 16 is pressed.	R	0

Table 9-19. FULL_CODE_31_24

Address Offset	0x0C		
Physical Address	0x0000 00DE	**Instance**	AUX_SCkeypad
Description	This register is updated when any key (in the range 24:31) is pressed. A bit at 1 indicates that the corresponding key is pressed.		
Type	R		

7	6	5	4	3	2	1	0
FULL_CODE_K31 − FULL_CODE_K24							

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K31	1 indicates that key 31 is pressed.	R	0
6	FULL_CODE_K30	1 indicates that key 30 is pressed.	R	0
5	FULL_CODE_K29	1 indicates that key 29 is pressed.	R	0
4	FULL_CODE_K28	1 indicates that key 28 is pressed.	R	0
3	FULL_CODE_K27	1 indicates that key 27 is pressed.	R	0
2	FULL_CODE_K26	1 indicates that key 26 is pressed.	R	0
1	FULL_CODE_K25	1 indicates that key 25 is pressed.	R	0
0	FULL_CODE_K24	1 indicates that key 24 is pressed.	R	0

Table 9-20. FULL_CODE_39_32

Address Offset	0x0D		
Physical Address	0x0000 00DF	**Instance**	AUX_SCkeypad
Description	This register is updated when any key (in the range 32:39) is pressed. A bit at 1 indicates that the corresponding key is pressed.		
Type	R		

7	6	5	4	3	2	1	0
FULL_CODE_K39 − FULL_CODE_K32							

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K39	1 indicates that key 39 is pressed.	R	0
6	FULL_CODE_K38	1 indicates that key 38 is pressed.	R	0
5	FULL_CODE_K37	1 indicates that key 37 is pressed.	R	0
4	FULL_CODE_K36	1 indicates that key 36 is pressed.	R	0
3	FULL_CODE_K35	1 indicates that key 35 is pressed.	R	0
2	FULL_CODE_K34	1 indicates that key 34 is pressed.	R	0
1	FULL_CODE_K33	1 indicates that key 33 is pressed.	R	0
0	FULL_CODE_K32	1 indicates that key 32 is pressed.	R	0

Table 9-21. FULL_CODE_47_40

Address Offset	0x0E		
Physical Address	0x0000 00E0	**Instance**	AUX_SCkeypad
Description	This register is updated when any key (in the range 40:47) is pressed. A bit at 1 indicates that the corresponding key is pressed.		
Type	R		

7	6	5	4	3	2	1	0
FULL_CODE_K47 − FULL_CODE_K40							

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K47	1 indicates that key 47 is pressed.	R	0
6	FULL_CODE_K46	1 indicates that key 46 is pressed.	R	0
5	FULL_CODE_K45	1 indicates that key 45 is pressed.	R	0
4	FULL_CODE_K44	1 indicates that key 44 is pressed.	R	0
3	FULL_CODE_K43	1 indicates that key 43 is pressed.	R	0
2	FULL_CODE_K42	1 indicates that key 42 is pressed.	R	0
1	FULL_CODE_K41	1 indicates that key 41 is pressed.	R	0
0	FULL_CODE_K40	1 indicates that key 40 is pressed.	R	0

Table 9-22. FULL_CODE_55_48

Address Offset	0x0F		
Physical Address	0x0000 00E1	**Instance**	AUX_SCkeypad
Description	This register is updated when any key (in the range 48:55) is pressed. A bit at 1 indicates that the corresponding key is pressed.		
Type	R		

7	6	5	4	3	2	1	0
FULL_CODE_K55 − FULL_CODE_K48							

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K55	1 indicates that key 55 is pressed.	R	0
6	FULL_CODE_K54	1 indicates that key 54 is pressed.	R	0
5	FULL_CODE_K53	1 indicates that key 53 is pressed.	R	0
4	FULL_CODE_K52	1 indicates that key 52 is pressed.	R	0
3	FULL_CODE_K51	1 indicates that key 51 is pressed.	R	0
2	FULL_CODE_K50	1 indicates that key 50 is pressed.	R	0
1	FULL_CODE_K49	1 indicates that key 49 is pressed.	R	0
0	FULL_CODE_K48	1 indicates that key 48 is pressed.	R	0

Table 9-23. FULL_CODE_63_56

Address Offset	0x10		
Physical Address	0x0000 00E2	**Instance**	AUX_SCkeypad
Description	This register is updated when any key (in the range 56:63) is pressed. A bit at 1 indicates that the corresponding key is pressed.		
Type	R		

7	6	5	4	3	2	1	0
FULL_CODE_K63 – FULL_CODE_K56							

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K63	1 indicates that key 63 is pressed.	R	0
6	FULL_CODE_K62	1 indicates that key 62 is pressed.	R	0
5	FULL_CODE_K61	1 indicates that key 61 is pressed.	R	0
4	FULL_CODE_K60	1 indicates that key 60 is pressed.	R	0
3	FULL_CODE_K59	1 indicates that key 59 is pressed.	R	0
2	FULL_CODE_K58	1 indicates that key 58 is pressed.	R	0
1	FULL_CODE_K57	1 indicates that key 57 is pressed.	R	0
0	FULL_CODE_K56	1 indicates that key 56 is pressed.	R	0

Table 9-24. KEYP_ISR1

Address Offset	0x11		
Physical Address	0x0000 00E3	**Instance**	AUX_SCkeypad
Description	This interrupt status ISR1 register determines which input keypad event triggered the interrupt line KEYP_INT1_n request. As shown in this table, bit 0 corresponds to a key-pressed event (ITKP), bit 1 to a long-key pressed event (ITLK), and bit 2 to a time-out event (ITTO). When a bit in this register is set to 1, the corresponding event is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the interrupt status ISR2 register. If the user writes 0 to a bit in this register, the value does not change when in COR mode. The interrupt status ISR2 register is synchronous with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED				ITMISR1	ITTOISR1	ITLKISR1	ITKPISR1

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Read returns 0.	RW	0x0
3	ITMISR1	0x0: Missing event hardware interrupt inactive on processor 1 request line 0x1: Missing event hardware interrupt active on processor 1 request line in test mode only	RW	0
2	ITTOISR1	0x0: Time-out hardware interrupt inactive on processor 1 request line 0x1: Time-out hardware interrupt active on processor 1 request line	RW	0
1	ITLKISR1	0x0: Long-key hardware interrupt inactive on processor 1 request line 0x1: Long-key hardware interrupt active on processor 1 request line	RW	0
0	ITKPISR1	0x0: Key-pressed hardware interrupt inactive on processor 1 request line 0x1: Key-pressed hardware interrupt active on processor 1 request line	RW	0

Table 9-25. KEYP_IMR1

Address Offset	0x12		
Physical Address	0x0000 00E4	**Instance**	AUX_SCkeypad
Description	This interrupt mask IMR1 register lets the user mask the expected transition on keypad event from generating an interrupt request on KEYP_INT1_n. The interrupt mask registers are programmed synchronously with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED				ITMISIMR1	ITTOIMR1	ITLKIMR1	ITKPIMR1

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Read returns 0.	RW	0x0
3	ITMISIMR1	0x0: Key-pressed event not masked on processor 1 request line 0x1: Missed event masked on processor 1 request line (active in test mode only)	RW	1
2	ITTOIMR1	0x0: Time-out event not masked on processor 1 request line 0x1: Time-out event masked on processor 1 request line	RW	1
1	ITLKIMR1	0x0: Long-key event not masked on processor 1 request line 0x1: Long-key event masked on processor 1 request line	RW	1
0	ITKPIMR1	0x0: Key-pressed event not masked on processor 1 request line 0x1: Key-pressed event masked on processor 1 request line	RW	1

Table 9-26. KEYP_ISR2

Address Offset	0x13		
Physical Address	0x0000 00E5	**Instance**	AUX_SCkeypad
Description	This interrupt status ISR2 register determines which input keypad event triggered the interrupt line KEYP_INT2_n request. As shown in this table, bit 0 corresponds to a key-pressed event (ITKP), bit 1 to a long-key pressed event (ITLK), and bit 2 to a time-out event (ITTO). When a bit in this register is set to 1, the corresponding event is requesting the interrupt. However, the user cannot generate an interrupt by writing 1 to the interrupt status ISR2 register. If the user writes 0 to a bit in this register, the value does not change when in COR mode. The interrupt status ISR2 register is synchronous with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED				ITMISR2	ITTOISR2	ITLKISR2	ITKPISR2

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Read returns 0.	RW	0x0
3	ITMISR2	0x0: Missing event hardware interrupt inactive on processor 2 request line 0x1: Missing event hardware interrupt active on processor 2 request line in test mode only	RW	0
2	ITTOISR2	0x0: Time-out hardware interrupt inactive on processor 2 request line 0x1: Time-out hardware interrupt active on processor 2 request line	RW	0
1	ITLKISR2	0x0: Long-key hardware interrupt inactive on processor 2 request line 0x1: Long-key hardware interrupt active on processor 2 request line	RW	0
0	ITKPISR2	0x0: Key-pressed hardware interrupt inactive on processor 2 request line 0x1: Key-pressed hardware interrupt active on processor 2 request line	RW	0

Table 9-27. KEYP_IMR2

Address Offset	0x14		
Physical Address	0x0000 00E6	**Instance**	AUX_SCkeypad
Description	This interrupt mask IMR2 register lets the user mask the expected transition on keypad event from generating an interrupt request on KEYP_INT2_n. The interrupt mask registers are programmed synchronously with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED				ITMISIMR2	ITTOIMR2	ITLKIMR2	ITKPIMR2

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Read returns 0.	RW	0x0
3	ITMISIMR2	0x0: Key-pressed event not masked on processor 2 request line 0x1: Missed event masked on processor 2 request line (active in test mode only)	RW	1
2	ITTOIMR2	0x0: Time-out event not masked on processor 2 request line 0x1: Time-out event masked on processor 2 request line	RW	1
1	ITLKIMR2	0x0: Long-key event not masked on processor 2 request line 0x1: Long-key event masked on processor 2 request line	RW	1
0	ITKPIMR2	0x0: Key-pressed event not masked on processor 2 request line 0x1: Key-pressed event masked on processor 2 request line	RW	1

Table 9-28. KEYP_SIR

Address Offset	0x15		
Physical Address	0x0000 00E7	**Instance**	AUX_SCkeypad
Description	For testing, this KEYP software interrupt KEYP_SIR register allows generating an interrupt event on the KEYP_INT1_n or KEYP_INT2_n request line by writing 1 to the targeted SIR bit in a specific test mode. An interrupt is generated if the corresponding KEYP_EDR bit is set to edge- (falling or rising) sensitive. External interrupt requests and internal software requests are merged before being sent to the PIH.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED				ITMISSIR	ITTOSIR	ITLKSIR	ITKPSIR

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Read returns 0.	R	0x0
3	ITMISSIR	0x0: Missed event software interrupt not set 0x1: Missed event software interrupt set (in test mode only)	RW	0
2	ITTOSIR	0x0: Time-out software interrupt not set 0x1: Time-out software interrupt set	RW	0
1	ITLKSIR	0x0: Long-key software interrupt not set 0x1: Long-key software interrupt set	RW	0
0	ITKPSIR	0x0: Key-pressed software interrupt not set 0x1: Key-pressed software interrupt set	RW	0

Table 9-29. KEYP_EDR

Address Offset	0x16		
Physical Address	0x0000 00E8	**Instance**	AUX_SCkeypad
Description	This interrupt edge-detection register KEYP_EDR lets the user define, for each external event (key pressed, long key, time-out event), the edge expected to trigger an interrupt request. The interrupt request can be generated from a high-to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions (bits are 11) accruing. To disable edge detection, the bits corresponding to the keypad event must be reset (00).		
Type	RW		

7	6	5	4	3	2	1	0
ITMISRISING	ITMISFALLING	ITTORISING	ITTOFALLING	ITLKRISING	ITLKFALLING	ITKPRISING	ITKPFALLING

Bits	Field Name	Description	Type	Reset
7	ITMISRISING	0x0: Missed event rising detection disabled 0x1: Missed event rising detection enabled (test mode only)	RW	0
6	ITMISFALLING	0x0: Missed event falling detection disabled 0x1: Missed event falling detection enabled (test mode only)	RW	1
5	ITTORISING	0x0: Time-out event rising detection disabled 0x1: Time-out event rising detection enabled	RW	0
4	ITTOFALLING	0x0: Time-out event falling detection disabled 0x1: Time-out event falling detection enabled	RW	1
3	ITLKRISING	0x0: Long-key event rising detection disabled 0x1: Long-key event rising detection enabled	RW	0
2	ITLKFALLING	0x0: Long-key event falling detection disabled 0x1: Long-key event falling detection enabled	RW	1
1	ITKPRISING	0x0: Key-pressed event rising detection disabled 0x1: Key-pressed event rising detection enabled	RW	0
0	ITKPFALLING	0x0: Key-pressed event falling detection disabled 0x1: Key-pressed event falling detection enabled	RW	1

Table 9-30. KEYP_SIH_CTRL

Address Offset	0x17		
Physical Address	0x0000 00E9	**Instance**	AUX_SCkeypad
Description	This KEYP SIH control register KEYP_SIH_CTRL lets the user disable a pending event incoming during software interrupt latency by programming 1 in the PENDDIS bit. By writing 0 in the EXCLEN bit, the user disables exclusivity between the interrupt request lines keyp_int1_n and keyp_int2_n. The ClearOnRead bit enables the clear-on-read feature. This means that any read access to the ISR clears this register and releases the associated interrupt line (default value). If disabled, a read access to a specific address value clears all ISRs within the SIH.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED					COR	PENDDIS	EXCLEN

Bits	Field Name	Description	Type	Reset
7:3	Reserved	Read returns 0.	R	0x00
2	COR	0x0: Clear ISR-specific bit field when write access mode. 0x1: Clear ISR when read mode.	RW	0
1	PENDDIS	0x0: Pending event feature is enabled. 0x1: Pending event feature is disabled.	RW	0
0	EXCLEN	0x0: Exclusivity is disabled. 0x1: Exclusivity is enabled.	RW	1

Vibrators

This chapter describes the vibrator control module of the device integrated power management/audio coder/decoder (codec) device. This chapter applies only to the TPS65930.

Topic **Page**

10.1 Vibrator Driver Overview

The device provides several ways to drive an external vibrator to signal an incoming call. The method used depends on the hardware and register configuration.

10.1.1 Vibrator H-Bridge

The audio subsection contains the vibrator H-bridge, which is a differential amplifier that can drive a vibrator controlled by a PWM. The PWM is controlled by registers through the I^2C bus or an audio signal.

10.2 Environment

10.2.1 Vibrator H-Bridge Drive Capabilities

A digital signal from the PWM generator is fed to the vibrator H-bridge driver. The vibrator H-bridge is a differential driver that drives vibrators. Differential output allows for bidirectional rotation.

Table 10-1 lists the capabilities of the vibrator H-bridge drive.

Table 10-1. Vibrator H-Bridge Drive Capabilities

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
VBAT voltage		2.8	3.6	4.8	V
Differential output swing	VBAT = 2.8 V	3.6			Vpp
	VBAT = 3.5 V	4.3			
Output resistance				4	Ω
Load capacitance				100	pF
Load resistance		8	16	60	Ω
Load inductance			30	300	µH
Total harmonic distortion	At –6 dBFs			10	%
Operating frequency		20		10K	Hz

10.3 Integration

The device vibrator capabilities (vibrator H-bridge) use the audio subchip function. The features are described in Chapter 13, *Audio*.

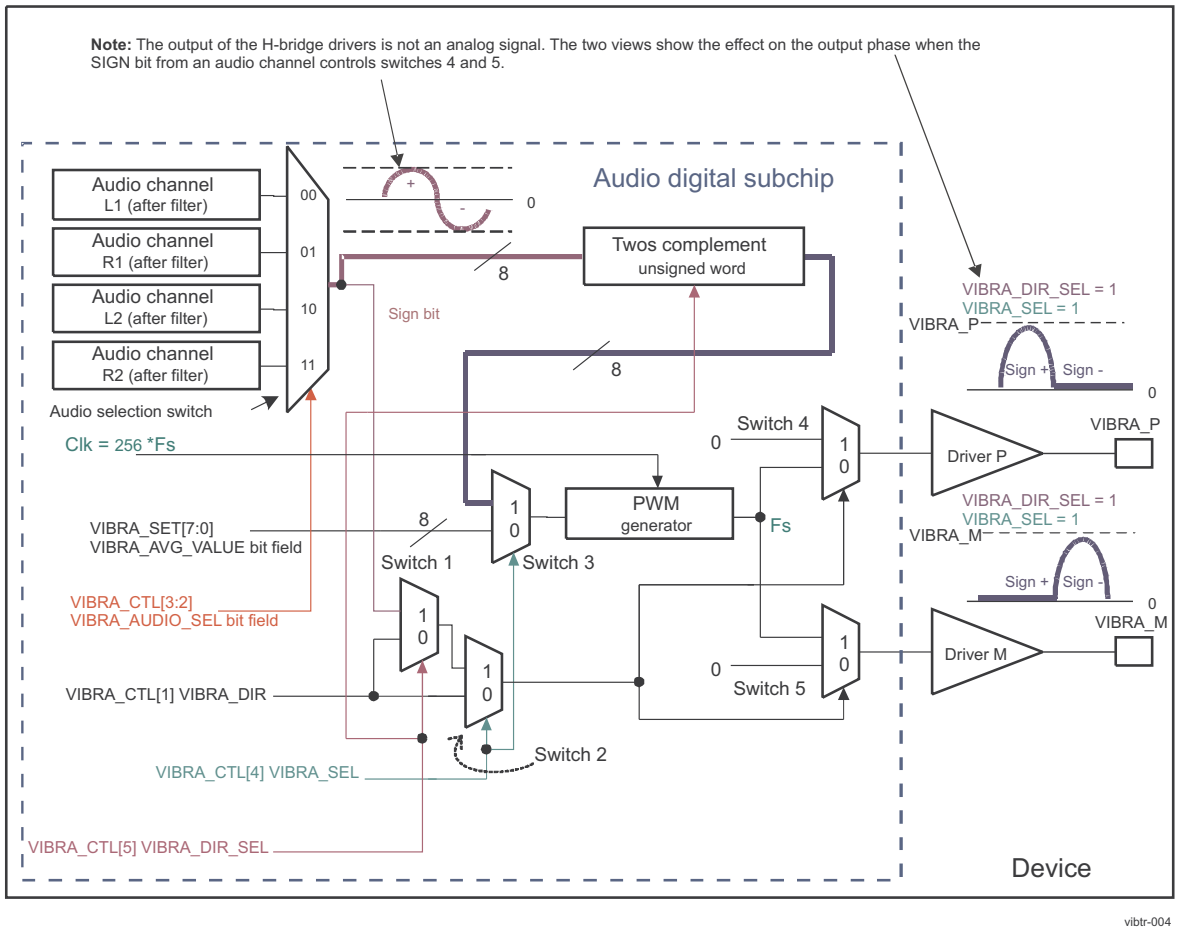
10.4 Functional Description

10.4.1 Vibrator H-Bridge Operation

In the device audio subchip, two vibrator modes are possible:

- One of the four audio channels is routed to a PWM modulator, which drives the H-bridge stage.
- A local digital pulse driver, controlled through the I^2C bus, is routed to the PWM generator, which drives the H-bridge stage. Figure 10-1 is a block diagram of the vibrator H-bridge driver.

Figure 10-1. Functional Diagram of the Vibrator H-Bridge Driver



NOTE: When the vibrator H-bridge is controlled by the audio signal (the VIBRA_CTL[4] VIBRA_SEL bit is set to 1), the rotation direction of the vibrator H-bridge must be controlled by the audio signal sign bit. Thus, the VIBRA_CTL[5] VIBRA_DIR_SEL bit must be set to 1.

10.4.1.1 Control

The VIBRA_CTL[0] VIBRA_EN bit controls power to the vibrator H-bridge (see Table 10-2).

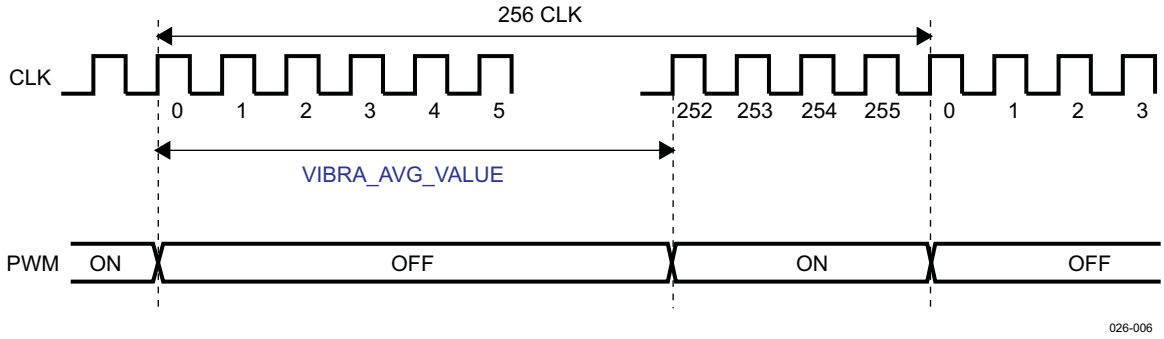
Table 10-2. Power Control of Vibrator H-Bridge by Register VIBRA_CTL

Bit	Field Name	Description	Type	Reset
0	VIBRA_EN	H-bridge power control 0x0: Vibrator H-bridge is off. 0x1: Vibrator H-bridge is on.	RW	0

10.4.1.2 PWM Operation

The PWM generator consists of an 8-bit counter (flip-flop) coupled to an 8-bit comparator. The 8-bit counter counts at a rate of 256 * Fs (where Fs is the sampling frequency). When the PWM generator is active, its counter continually steps through its 256 combinations. A PWM output signal (pulse-width-modulated output signal) is cleared to 0 when the counter passes from the 0xFF to the 0x00 value, and the PWM output signal is set to 1 when the counter equals the value of the 8-bit input comparator programmed in the VIBRA_SET[7:0] VIBRA_AVG_VALUE bit field. Figure 10-2 shows the pulse width-modulated output signal PWM with VIBRA_SET[7:0] VIBRA_AVG_VALUE = 0xFC (252 in decimal).

Figure 10-2. PWM Generator Output



10.4.1.3 Using Audio or Register VIBRA_SET to Determine the PWM Generator Output

Figure 10-1 shows how an audio signal (or the value in the VIBRA_SET register) is selected to control the PWM generator.

10.4.2 Analysis of the Vibrator H-Bridge Operation

This section analyzes the vibrator H-bridge operation and answers two questions:

- How is the relative phase of the output changed and what does it mean?
- How are the output phase and output level controlled?

10.4.2.1 Output Phase Change and Meaning

The signal on VIBRA_P and VIBRA_M is binary and is provided by driver P and driver M, respectively. The input to driver P is from switch 4, and the input to driver M is from switch 5. Input 1 of switch 4 and input 0 of switch 5 are tied to logical 0. Input 0 of switch 4 and input 1 of switch 5 are connected to the PWM generator output.

Control of switch 4 and switch 5 comes from the output of switch 2. Toggling the output of switch 2 between logical 1 and logical 0 causes the output from the PWM generator to be sent to VIBRA_P or VIBRA_M; at the same time, the other vibrator output connection (not connected to the PWM generator output) is connected to logical 0. Through this capability, the relative polarity of VIBRA_P with respect to VIBRA_M can be made positive or negative.

10.4.2.2 Output Level and Output Phase Controls

10.4.2.2.1 Vibrator H-Bridge Output

The PWM generator output determines the output of the vibrator H-bridge. Three issues control the PWM generator output:

- The duty cycle of the PWM generator (it runs at a constant rate fixed by 256 * Fs) is controlled by the 8 bits loaded into its comparator, which is set when its output turns off during the cyclical count from 0 to 255 (the output turns on when counting through 0).
- Is the output of the PWM generator switched between outputs VIBRA_P and VIBRA_M?
- If the output is switched, what controls the switching?

PWM Generator Duty Cycle

The outputs of switch 3 (8 bits wide) are the inputs to the comparators in the PWM generator (see Section 10.4.1.2, *PWM Operation*). Selecting input 0 or input 1 of switch 3 determines the source of the signal that turns off the output of the PWM generation as it continuously cycles through the counting sequence driven by its clock input (256 * Fs).

- Select the VIBRA_SET[7:0] VIBRA_AVG_VAL bit field to control the PWM generator duty cycle and load the desired values and clear the VIBRA_CTL[4] VIBRA_SEL bit to 0.

NOTE: The average value at the PWM generator output is the inverted value of the VIBRA_SET[7:0] VIBRA_AVG_VALUE bit field: The minimum average value is VIBRA_SET[7:0] VIBRA_AVG_VALUE = 0xFF, and the maximum average value is VIBRA_SET[7:0] VIBRA_AVG_VALUE = 0x01.

- Use a digitized audio signal to control the PWM generator duty cycle. The unsigned twos complement equivalent of the audio signal is selected to set the cutoff time of the PWM generator by setting the VIBRA_CTL[4] VIBRA_SEL bit so that input 1 of switch 3 is selected. Any of the four audio channels can be selected to control the PWM generator. Selection is made through the VIBRA_CTL[3:2] VIBRA_AUDIO_SEL bit field.

CAUTION

When the audio signal is used to control the PWM generator, the gain of the audio digital filters (registers ARXR1PGA, ARXL1PGA, ARXR2PGA, and ARXL2PGA) must be configured so as not to saturate at the input of the PWM generator (the maximum audio signal applied to the input of the PWM generator must be less than 0 dBFs). For a full-scale 16-bit audio signal at the input of the audio digital filters, the gain of the audio digital filters must not exceed 0 dB.

PWM Generator Output Phase

- If the value of the VIBRA_SET[7:0] VIBRA_AVG_VAL bit field is used to control the PWM generator duty cycle (an audio signal is not used), only one source is used to toggle the output phase of the PWM generator. When an audio signal is not used to control the PWM generator, there is no audio SIGN bit to select to toggle the phase. Switch 2 (controlled by VIBRA_SEL) selects input 0, which allows the VIBRA_DIR bit (in the VIBRA_CTL register) to control the output phase of the PWM generator.
- If an audio signal is used to control the PWM generator duty cycle, the audio sign bit must be used to toggle the output phase of the PWM generator. Thus, the VIBRA_CTL[5] VIBRA_DIR_SEL bit must be set to 1.

The VIBRA_DIR or the SIGN bit can control the output phase of the PWM generator when using audio to control the PWM generator duty cycle because when switch 3 is set to accept the audio twos complement signal to control the PWM generator duty cycle, the control signal (the VIBRA_CTL[4] VIBRA_SEL bit) also causes switch 2 to select its input 1, which is fed from the output of switch 1. Input 0 of switch 1 is fed by the VIBRA_CTL[5] VIBRA_DIR bit, and input 1 of switch 1 comes from the SIGN bit of the audio signal.

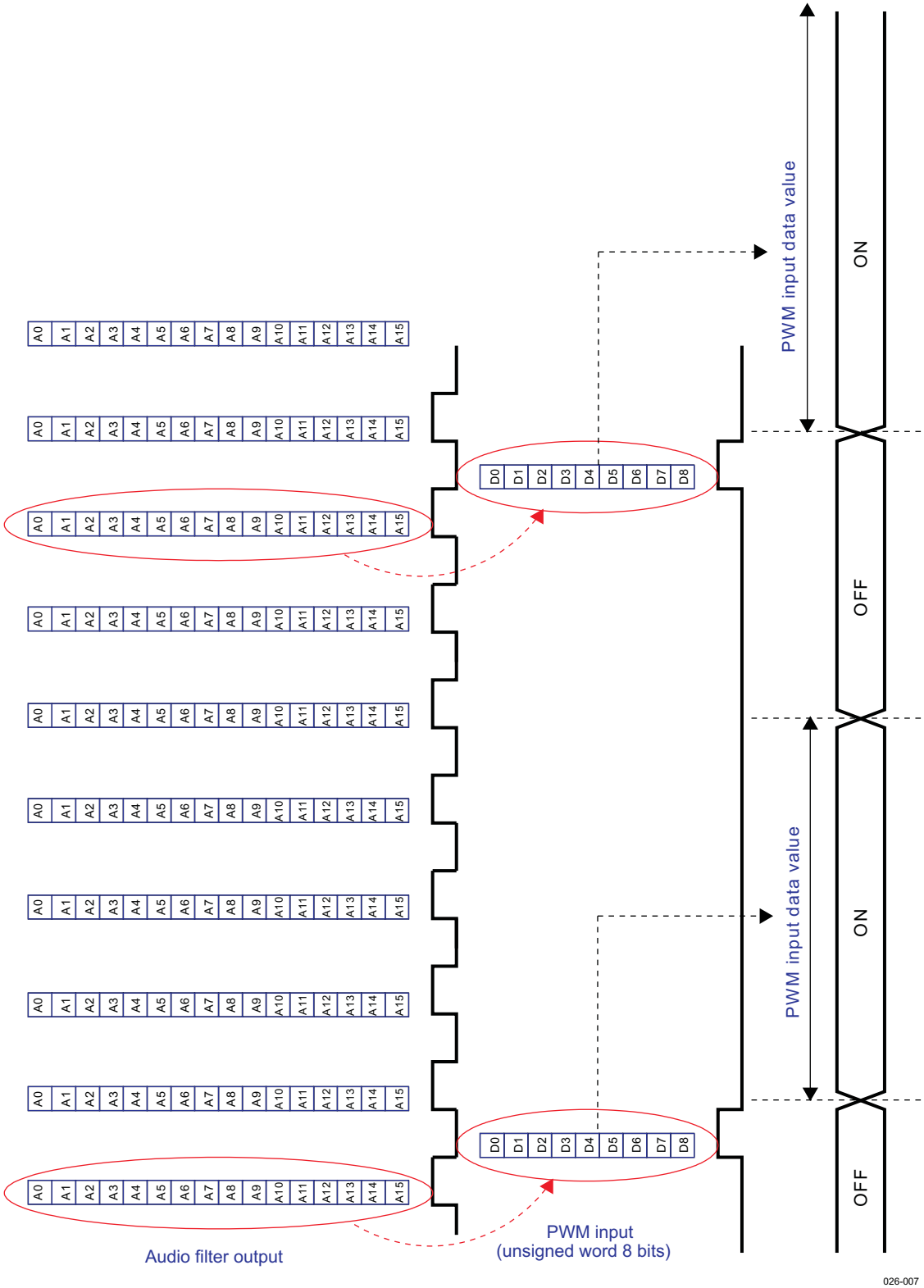
10.4.3 H-Bridge Capabilities

It is possible to provide a signal to an external vibrator (through VIBRA_P and VIBRA_M) that mimics an analog signal by controlling the PWM generator duty cycle (with the twos complement of the audio) and the PWM generator output phase (with the SIGN bit derived from the audio).

10.4.3.1 Audio Channel Control of the PWM Generator

Figure 10-3 shows how an audio signal is sampled and used to control the PWM generator.

Figure 10-3. Audio Channel Sampling to Control the PWM Generator



Every eighth sample of the audio signal is used to develop a value sent to the PWM generator. The ON/OFF trace in Figure 10-3 represents the output of the PWM generator. The PWM generator turns on every time its counter (as previously described) goes through 0. The binary value of the sampled audio signal is then used to select where in the counter cycle (from 0 to 255) the PWM generator output is turned off. When the relative amplitude of the audio signal changes, this has the effect of varying when the PWM generator turns off during the cycling of its counter. (The audio signal sampling rate and the clock frequency that runs the PWM generator counter are integrally related.)

NOTE: When the PWM generator is controlled by an audio signal, the AUDIO_IF[1] CLK256FS_EN bit must be set to 1.

CAUTION

When the audio signal is used to control the PWM generator, the gain of the audio digital filters (the ARXR1PGA, ARXL1PGA, ARXR2PGA, and ARXL2PGA registers) must be configured so as not to saturate at the input of the PWM generator (the maximum audio signal applied to the input of the PWM generator must be less than 0 dBFs). For a full-scale 16-bit audio signal at the input of the audio digital filters, the gain of the audio digital filters must not exceed 0 dB.

10.4.3.2 Vibrator Bridge Registers

Table 10-3 through Table 10-5 contain the register descriptions for control of the vibrator H-bridge.

Table 10-3. VIBRA_CTL Control Functions

Bits	Field Name	Description	Type	Reset
5	VIBRA_DIR_SEL	Vibrator H-bridge direction selection bit (available only if audio data drives the vibrator H-bridge) 0x0: Direction is given by bit VIBRA_DIR. 0x1: Direction is given by the audio data most-significant bit (MSB).	RW	0
4	VIBRA_SEL	Vibrator H-bridge driver selection 0x0: Local vibrator driver (controlled by OCP register, average value control word in the VIBRA_SET register) 0x1: Audio data as vibrator driver (the audio channel controlled by AUDIOCH word control)	RW	0
3:2	VIBRA_AUDIO_ SEL	Audio channel selection control 0x0: LEFT1 input selection 0x1: RIGHT1 input selection 0x2: LEFT2 input selection 0x3: RIGHT2 input selection	RW	0x0
1	VIBRA_DIR	H-bridge direction control bit 0x0: Positive polarity 0x1: Negative polarity	RW	0
0	VIBRA_EN	H-bridge power control 0x0: Vibrator H-bridge is off. 0x1: Vibrator H-bridge is on.	RW	0

Table 10-4. CODEC_MODE Power Control Bit

Bit	Field Name	Description	Type	Reset
1	CODECPDZ	Codec power control bit 0x0: Codec is off. 0x1: Codec is on.	RW	0

Table 10-5. VIBRA_SET Control Functions

Bits	Field Name	Description	Type	Reset
7:0	VIBRA_AVG_VAL	Sets the H-bridge PWM generator turnon value. The average value is the inverse of the VIBRA_AVG_VAL value. The minimal value is 0x01 and the value 0x00 is forbidden	RW	0x00

10.5 Programming Model

10.5.1 Vibrator H-Bridge

To use the vibrator H-bridge:

1. Disable LEDA: Set the LEDEN[0] LEDAON bit to logic 0.
2. Disable LEDB: Set the LEDEN[1] LEDBON bit to logic 0.
3. Turn on the codec:
   Set the CODEC_MODE[1] CODECPDZ bit to 1.

The H-bridge vibrator can get its operation from the following sources:

- An audio channel can provide the stimulus.
- A PWM in the audio subchip can generate the signal.

If an audio channel provides the motivating force for the vibrator (for example: the audio right 1 channel):

1. Set the VIBR_CTL[4] VIBRA_SEL bit to 1.
2. Set the VIBR_CTL[5] VIBRA_DIR_SEL bit to 1.
3. Set the VIBR_CTL[3:2] VIBRA_AUDIO_SEL bit field to 0x1 (audio right 1 channel).
4. Select the use of the SIGN bit to determine the output phase to VIBRA_P and VIBRA_M.
5. Set the VIBRA_CTL[0] VIBRA_EN bit to 1 (power to the H-bridge is driven by audio data).

NOTE:

- If audio data drives the vibrator H-bridge, set the VIBRA_SET register to 0xFF.
- The direction of the vibrator H-bridge controlled by the VIBRA_DIR bit can be changed on the fly.

6. Set the audio PLL input frequency: APLL_CTL [APLL_INFREQ] = 0x6.
7. Enable the audio PLL: APLL_CTL [APLL_EN] = 1.

NOTE: Do not enable LEDA/B and the H-vibrator simultaneously.

10.6 Register Manual

Table 10-6 through Table 10-6 describe the individual device registers for the operation of the vibrator.

10.6.1 Register Access

The device internal registers are accessed through the device I^2C buses. For more information, see Chapter 2, *Control Interface*.

Table 10-6. VIBRA_CTL

Address Offset	0x45		
Physical Address	0x0000 0045	**Instance**	AUDIO_SCAUDIO_VOICE
Description	Vibrator H-bridge control register If codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If CODECPDZ is off, the codec is powered down and this register setting has no effect.		
Type	RW		

7	6	5	4	3 2	1	0
Reserved	SPARE	VIBRA_DIR_SEL	VIBRA_SEL	VIBRA_AUDIO_SEL	VIBRA_DIR	VIBRA_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	SPARE	Spare bit	RW	0
5	VIBRA_DIR_SEL	Vibrator H-bridge direction selection bit (available only if audio data drive the vibrator H-bridge) 0x0: Direction is given by the VIBRA_DIR bit. 0x1: Direction is given by the audio data MSB.	RW	0
4	VIBRA_SEL	Vibrator H-bridge driver selection 0x0: Local vibrator driver (controlled by the OCP register, average value control word in the VIBRA_SET register) 0x1: Audio data as vibrator driver (the audio channel controlled by AUDIOCH word control)	RW	0
3:2	VIBRA_AUDIO_ SEL	Audio channel selection control 0x0: LEFT1 input selection 0x1: RIGHT1 input selection 0x2: LEFT2 input selection 0x3: RIGHT2 input selection	RW	0x0
1	VIBRA_DIR	H-bridge direction control bit 0x0: Positive polarity 0x1: Negative polarity	RW	0
0	VIBRA_EN	H-bridge power control 0x0: Vibrator H-bridge is off. 0x1: Vibrator H-bridge is on.	RW	0

Table 10-7. VIBRA_SET

Address Offset	0x46		
Physical Address	0x0000 0046	**Instance**	AUDIO_SCAUDIO_VOICE
Description	Vibrator H-bridge PWM generator turnoff control register		
Type	RW		

7	6	5	4	3	2	1	0
VIBRA_AVG_VAL							

Bits	Field Name	Description	Type	Reset
7:0	VIBRA_AVG_VAL	Sets the vibrator H-bridge PWM generator turnon value. The average value is the inverse of the VIBRA_AVG_VAL value. The minimal value is 0x01 and the value 0x00 is forbidden.	RW	0x00

Table 10-8. CODEC_MODE

Address Offset	0x01		
Physical Address	0x0000 0001	**Instance**	AUDIO_SCAUDIO_VOICE
Description	System mode control register		
Type	RW		

7	6	5	4	3	2	1	0
APLL_RATE				SEL_16K	SPARE	CODECPDZ	OPT_MODE

Bits	Field Name	Description	Type	Reset
7:4	APLL_RATE	Audio mode: Select sampling frequency (Fs) 0x0: 8 kHz 0x1: 11.025 kHz 0x2: 12 kHz 0x4: 16 kHz 0x5: 22.05 kHz 0x6: 24 kHz 0x8: 32 kHz 0x9: 44.1 kHz 0xA: 48 kHz 0xE: 96 kHz	RW	0x0
3	SEL_16K	Voice mode: Select 16-kHz mode. 0x0: Sample at 8 kHz. 0x1: Sample at 16 kHz.	RW	0
2	SPARE	Spare bit	RW	0
1	CODECPDZ	Codec power control bit 0x0: Codec is off. 0x1: Codec is on.	RW	0
0	OPT_MODE	Audio and voice option selection 0x0: Option 2: Voice uplink (stereo) and downlink (mono) + 1 RX and TX stereo audio path 0x1: Option 1: 2 RX and TX stereo audio path	RW	0

General-Purpose Inputs/Outputs

This chapter describes the general-purpose inputs and outputs (GPIOs) for the device power management/audio coder/decoder (codec) device.

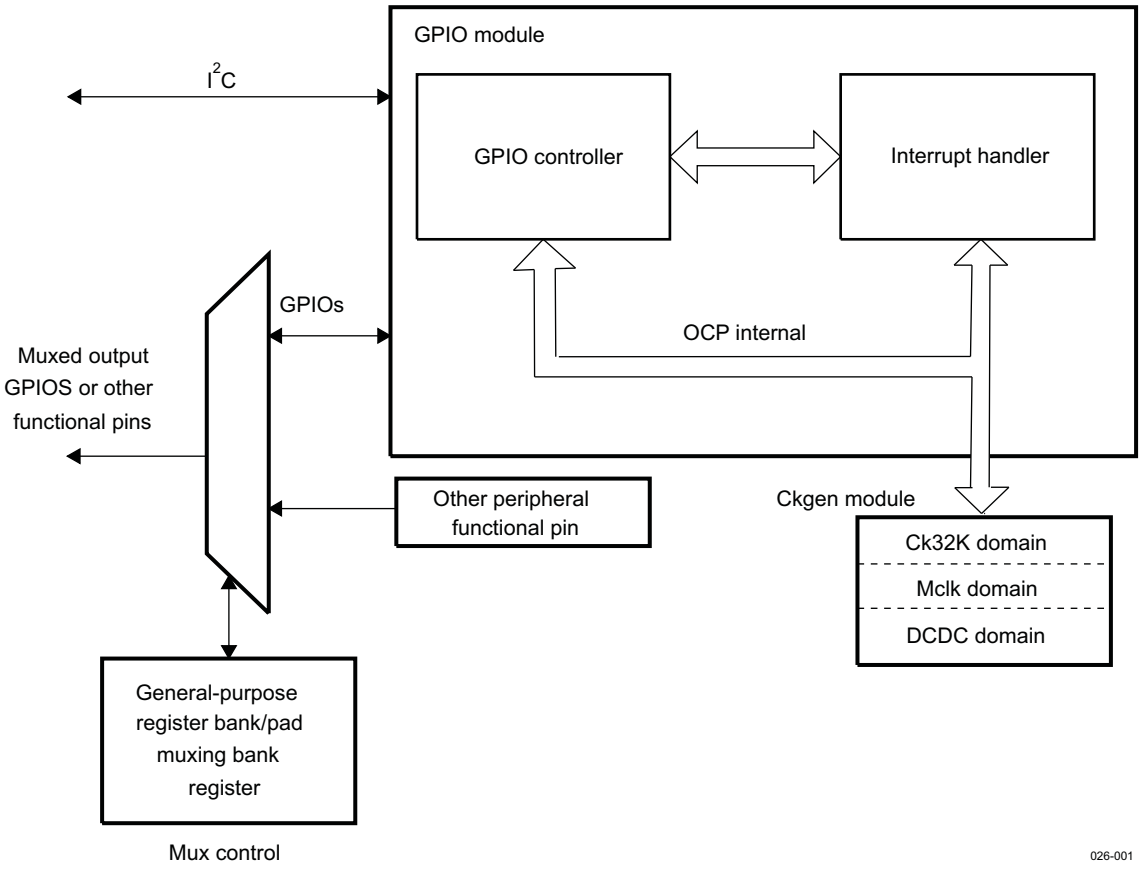
Topic **Page**

11.1 GPIO Overview

The device includes 18 level-compatible edge-triggered general-purpose inputs and outputs (GPIOs). This is another instance of the TPS65930 and TPS65920 having a reduced subset of the functions of the TPS65950 because of limited pin access on the package. The TPS65939 and TPS 65920 have access to only GPIO pins ADCIN0 and ADCIN2.

These GPIOs can be used as interrupts when configured as inputs and as card detectors, detecting memory cards and subscriber identity module (SIM) cards. Figure 11-1 is the top-level diagram of the GPIO module.

Figure 11-1. GPIO Overview



The GPIO module includes the following features:

- The input line value is sampled into the data-input register (GPIODATAIN) and can be read by the open-core protocol (OCP) bus.
- The output line level reflects the value written in the data-output register (GPIODATAOUT) through the OCP bus.
- The data-output register includes a set-and-clear feature.
- In active mode, the input line can be used through level- and edge-detectors to trigger synchronous interrupts. The edge used (rising, falling, or both) or the level used (logical 0, logical 1, or both) can be configured using the edge-detection register (GPIO_EDR).
- The direction of the GPIO line is configurable using the GPIODATADIR register.
- The debouncing feature on each GPIO line can be enabled or disabled through the debounce register (GPIO_DEBEN).

11.1.1 General-Purpose Register Bank

The 8-bit general-purpose (GP) register bank can enable and disable the PWM0/PWM1 (pulse-width modulation) feature used by peripherals, such as the vibrator and the LED. These output pins are multiplexed with GPIOs, and the register is accessible through the inter-integrated circuit (I²C™).

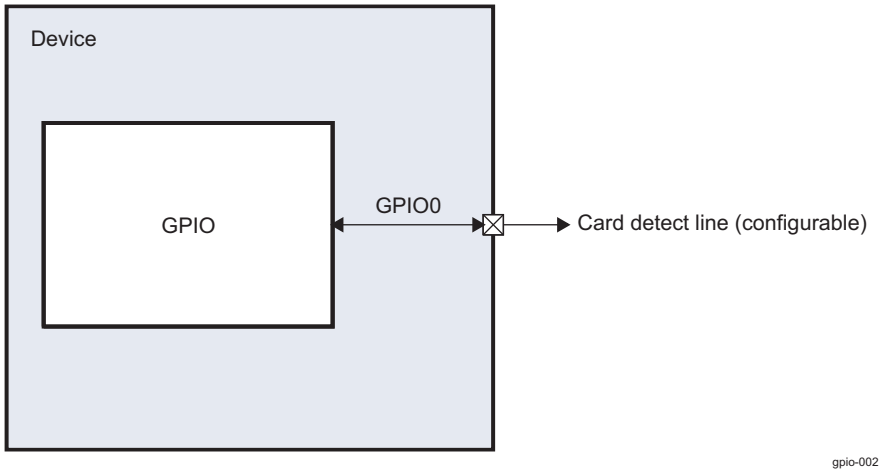
11.1.2 Pad-Multiplexing Register Bank – PMBR1 and PMBR2

The pad-multiplexing register bank selects functions based on the register configuration. GPIOs are multiplexed with the peripherals of the device. The register bank is 16 bits wide and is composed of the PMBR1 and PMBR2 registers, which are accessible through the I²C. Table 11-46 and Table 11-47 show the PMBR1 and PMBR2 registers, respectively.

11.2 GPIO Environment

The GPIO is a flexible user-programmable GP input/output controller. The GP pins can be connected to external devices. Figure 11-2 is the GPIO interface diagram.

Figure 11-2. GPIO Interface Diagram



GPIO line 0 can be used for card detection. It generates a particular behavior of the device.

11.2.1 GPIO Functional Interfaces

11.2.1.1 GPIO Interface Functional Description

Table 11-1 lists default values and the direction set for the GPIOs at reset.

Table 11-1. I/O Description

Signal	I/O	Description	Reset Value
GPIO[0:17]	I/O	GPIO signals	All GPIOs configured as inputs with the pulldown resistor active (0 except for those multiplexed with USB pins)

11.3 GPIO Module Integration

This section describes the clocks, the reset technique, and the power domain used by the GPIO module.

11.3.1 Clocking, Reset, and Power-Management Scheme

11.3.1.1 Clocks

The GPIO uses two clocks:

- The 3-MHz clock samples GPIO input lines. Sampling operations for data capture and event detection use the rising edge. The minimum pulse width detected by a GPIO signal is 666 ns, or twice the clock period of the 3-MHz clock.
- The OCP interface clock clocks all internal OCP-interfaced registers for bus read and write operations.

11.3.1.2 Reset

The device hardware reset generated from the power module performs a global reset on the GPIO module for the device subchips, except the power subchip. The reset is an active low signal.

The GPIO does not support a software reset.

11.3.1.3 Power Domain

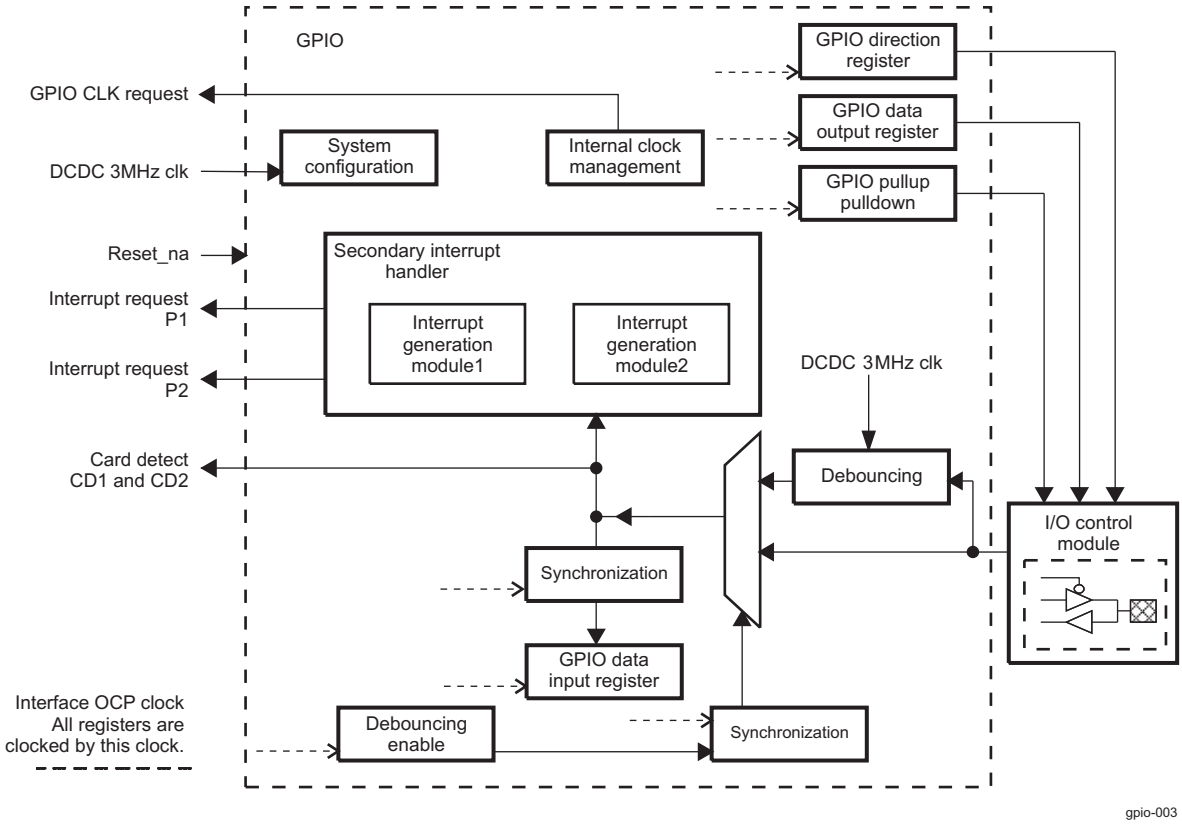
The GPIO is powered by the DIGITAL power domain (VINTDIG, 1.5 V).

11.4 GPIO Functional Description

11.4.1 Block Diagram

Figure 11-3 is the block diagram of the GPIO.

Figure 11-3. GPIO Block Diagram



For each GPIO pin, independent direction control is set by a programmable register (GPIODATADIR) that enables the GPIO pins to be configured individually as input or output. Two identical interrupt generation modules process synchronous interrupt requests from each GPIO for independent operation in a biprocessor environment. Each module controls its own synchronous interrupt request line and has its own interrupt mask register (IMR) and interrupt status register (ISR) (for more information about interrupt generation, see Chapter 4, *Interrupts*).

The IMR (GPIO_IMR) selects the GPIO(s) considered for interrupt request generation. The ISR indicates which GPIO(s) activates the interrupt request. The data direction register (GPIODATADIR) enables the input/output (I/O) capabilities of the GPIO pins by setting the direction in the correct bit field.

The edge-detection register (GPIO_EDR) allows a choice of interrupt level; it can be configured for a rising edge, falling edge, both edges, or no detection. Three ISRs are available for each interrupt-generation module (INT1 and INT2). These registers determine which GPIO triggered the interrupt line (INT1 or INT2).

All GPIO registers are clocked by the OCP clock and are resynchronized by the 3-MHz clock. Internal clock management, system configuration, and synchronization blocks synchronize the two clocks.

The set-and-clear feature is provided for the data-output register. To avoid the atomic test and set use for a register update, this peripheral offers the set-and-clear protocol register update.

11.4.1.1 Card-Detect

GPIO0 can be used for card detection. In the GPIO, the CD1 (Card Detect 1) signal goes to the power subchip (POWER_SC). Card detection can be on the rising or the falling edge of the GPIO signals (CD1). The DCDC_GLOBAL_CFG register can be modified to support this feature.

11.4.1.1.1 GPIO0 Card-Detect Feature (CD1)

The GPIO0 card-detect feature can be used as a card-detection function to generate a particular behavior on the device. When the card-detect functionality is enabled by writing 1 to the GPIO_CTRL[0]) GPIOCD1 bit, the device automatically turns off the VMMC1 low dropout (LDO) when a card is removed (depending on the configuration register in the power module). The DCDC_GLOBAL_CFG[6] CARD_DETECT_1_LEVEL bit can configure CD1 to be active high or active low.

To turn on the VMMC1 LDO, the system uses an interrupt signal generated by the insertion of the card.

11.4.1.2 Debouncing

Each GPIO input signal can be debounced for a fixed period. To enable or disable the feature independently, write 1 or 0, respectively, to the GPIO_DEBENx (where x = 1, 2, or 3) GPIOxDEB bit (where x = 0 to 17). The debounce time is fixed and set to 30 ms by the hardware and is not configurable.

11.4.1.3 Interrupts

The GPIO includes a secondary interrupt handler (SIH) to which interrupt events coming from the GPIO data register are connected (for more information about the SIH, see Chapter 4, *Interrupts*).

Because the GPIO module is synchronous, latency is minimal between the expected event occurrence and activation of the interrupt line(s). This should not exceed three 3-MHz interface clock cycles when the debouncing feature is not used.

When debouncing is active, latency should be less than three internal interface 3-MHz clock cycles plus GPIODEBOUNCINGTIME (30 ms).

11.4.1.4 Pullup and Pulldown

Each GPIO has a configurable pullup and a pulldown of a 100-kΩ internal resistor. The pulldown is enabled by default to avoid leakage when a GPIO is not connected externally.

Five 8-bit registers control the pullup and pulldown feature:

- GPIOPUPDCTR1
- GPIOPUPDCTR2
- GPIOPUPDCTR3
- GPIOPUPDCTR4
- GPIOPUPDCTR5

The pullup and pulldown feature can be activated by writing to the GPIOPUPDCTRx (where x = 1 to 5) GPIOyPU or GPIOyPD bit, (where y = 1 to 18).

11.5 GPIO Programming Model

11.5.1 Set-and-Clear Instruction

11.5.1.1 Description

To avoid the atomic test and set use for the data-output register update, the GPIO peripheral offers the set-and-clear protocol for register update. The set-and-clear protocol consists of writing instructions to dedicated addresses: one address for setting the bit(s) and one address for clearing the bit(s). Writing 1 at a particular bit position(s) clears or sets the bit. Writing 0 leaves the bit unaffected.

To clear the data-output register (GPIODATAOUTx), write 1 to the GPIOyOUT field (CLEARGPIODATAOUTx[y]).

To set the data-output register (GPIODATAOUTx), write 1 to the SETGPIODATAOUTx (where x = 1, 2, or 3) GPIOyOUT bit (where y = 0 to 17)..

11.5.1.2 Clear Instruction

11.5.1.2.1 Clear Register Address

The clear data-output registers are CLEARGPIODATAOUT1, CLEARGPIODATAOUT2, and CLEARGPIODATAOUT3.

A read of the clear data-output register returns the value of the data-output register.

11.5.1.2.2 Clear Instruction Example

Figure 11-4 is an example of a clear instruction.

Figure 11-4. Write to CLEARGPIODATAOUT Register Example

CLEARGPIODATAOUTn (where n = 1, 2, or 3)	0	1	0	0	0	0	0	1

to

CLEARGPIODATAOUTn (where n = 1, 2, or 3)	0	1	0	0	0	0	0	0

gpio-004

11.5.1.3 Set Instruction

11.5.1.3.1 Set Register Address

The set data-output registers are SETGPIODATAOUT1, SETGPIODATAOUT2, and SETGPIODATAOUT3.

A read of the set data-output register returns the value of the data-output register.

11.5.1.3.2 Set Instruction Example

Figure 11-5 is an example of a set instruction.

Figure 11-5. Write to SETGPIODATAOUT Register Example

SETGPIODATAOUTn (where n = 1, 2, or 3)	1	0	0	0	0	0	0	0

to

SETGPIODATAOUTn (where n = 1, 2, or 3)	1	0	0	0	1	1	1	0

gpio-005

11.5.2 Data Input (Capture)/Output (Drive)

The output enable register (GPIODATADIR1) controls the output capability of each GPIO pin (GPIOxDIR). At reset, all GPIO-related pins are configured as inputs, and output capabilities are disabled.

When configured as an output (GPIOxDIR = 1), the value in the GPIODATAOUT GPIOxOUT bit is driven on the corresponding GPIO pin. Data is written to the data-output register synchronously with the interface clock.

The data-output register can be accessed using read/write operations or the set-and-clear protocol register update. This feature enables specific bits in the register to be set or cleared with a single write access to the set output data register (SETGPIODATAOUT) or to the clear output data register (CLEARGPIODATAOUT) address.

When configured as an input (GPIOxDIR = 0), the state of the input can be read from the the GPIODATAIN GPIOxIN bit. Input data is sampled synchronously with the 3-MHz functional clock and captured in the data-input register after OCP clock resynchronization. Thus, after changing, GPIO pin levels are captured to the data-input register after two interface clock cycles (the cycles required to synchronize to write data), if debouncing is disabled. If debouncing is enabled, capture requires an additional 30 ms.

11.6 GPIO Register Manual

This section summarizes the GPIO module, including the GPIO instance and the module register map and bit definitions for each bit field.

11.6.1 GPIO Module Instance Summary

Table 11-2 lists the base address and address space for the interrupt subchip (INT_SC) module instances.

Table 11-2. Instance Summary

Module Name	Base Address	Size
GPIO	0x0000 0098	46 bytes

11.6.2 GPIO Module Register Mapping Summary

This section provides information about the GPIO module instance. Table 11-3 summarizes the GPIO registers. Table 11-4 through Table 11-47 describe the registers in the module instance.

Table 11-3. GPIO Register Summary

Register Name	Type	Register Width (Bits)	Physical Address
GPIODATAIN1	R	8	0x0000 0098
GPIODATAIN2	R	8	0x0000 0099
GPIODATAIN3	R	8	0x0000 009A
GPIODATADIR1	RW	8	0x0000 009B
GPIODATADIR2	RW	8	0x0000 009C
GPIODATADIR3	RW	8	0x0000 009D
GPIODATAOUT1	RW	8	0x0000 009E
GPIODATAOUT2	RW	8	0x0000 009F
GPIODATAOUT3	RW	8	0x0000 00A0
CLEARGPIODATAOUT1	RW	8	0x0000 00A1
CLEARGPIODATAOUT2	RW	8	0x0000 00A2
CLEARGPIODATAOUT3	RW	8	0x0000 00A3
SETGPIODATAOUT1	RW	8	0x0000 00A4
SETGPIODATAOUT2	RW	8	0x0000 00A5
SETGPIODATAOUT3	RW	8	0x0000 00A6
GPIO_DEBEN1	RW	8	0x0000 00A7
GPIO_DEBEN2	RW	8	0x0000 00A8
GPIO_DEBEN3	RW	8	0x0000 00A9
GPIO_CTRL	RW	8	0x0000 00AA
GPIOPUPDCTR1	RW	8	0x0000 00AB
GPIOPUPDCTR2	RW	8	0x0000 00AC
GPIOPUPDCTR3	RW	8	0x0000 00AD
GPIOPUPDCTR4	RW	8	0x0000 00AE
GPIOPUPDCTR5	RW	8	0x0000 00AF
GPIO_ISR1A	RW	8	0x0000 00B1
GPIO_ISR2A	RW	8	0x0000 00B2
GPIO_ISR3A	RW	8	0x0000 00B3
GPIO_IMR1A	RW	8	0x0000 00B4
GPIO_IMR2A	RW	8	0x0000 00B5
GPIO_IMR3A	RW	8	0x0000 00B6
GPIO_ISR1B	RW	8	0x0000 00B7

Table 11-3. GPIO Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address
GPIO_ISR2B	RW	8	0x0000 00B8
GPIO_ISR3B	RW	8	0x0000 00B9
GPIO_IMR1B	RW	8	0x0000 00BA
GPIO_IMR2B	RW	8	0x0000 00BB
GPIO_IMR3B	RW	8	0x0000 00BC
GPIO_EDR1	RW	8	0x0000 00C0
GPIO_EDR2	RW	8	0x0000 00C1
GPIO_EDR3	RW	8	0x0000 00C2
GPIO_EDR4	RW	8	0x0000 00C3
GPIO_EDR5	RW	8	0x0000 00C4
GPIO_SIH_CTRL	RW	8	0x0000 00C5
PMBR1	RW	8	0x0000 0092
PMBR2	RW	8	0x0000 0093

Table 11-4. GPIODATAIN1

Address Offset	0x00		
Physical Address	0x0000 0098	**Instance**	INT_SCGPIO
Description	This GPIODATAIN1 data-input register registers data read from the GPIO[0:7] pins. This data-input register is a read-only register. Input data is sampled synchronously with the interface clock and captured in the data-input register synchronously with the OCP bus clock.		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7IN	GPIO6IN	GPIO5IN	GPIO4IN	GPIO3IN	GPIO2IN	GPIO1IN	GPIO0IN

Bits	Field Name	Description	Type	Reset Off
7	GPIO7IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
6	GPIO6IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
5	GPIO5IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
4	GPIO4IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
3	GPIO3IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
2	GPIO2IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
1	GPIO1IN		R	0
		Read 0x0: GPIO input is 0.		

Bits	Field Name	Description	Type	Reset Off
		Read 0x1: GPIO input is 1.		
0	GPIO0IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		

Table 11-5. GPIODATAIN2

Address Offset	0x01
Physical Address	0x0000 0099 **Instance** INT_SCGPIO
Description	This GPIODATAIN2 data-input register registers data read from the GPIO[8:15] pins. This data-input register is a read-only register. Input data is sampled synchronously with the interface clock and captured in the data-input register synchronously with the OCP bus clock.
Type	R
Write Latency	

7	6	5	4	3	2	1	0
GPIO15IN	GPIO14IN	GPIO13IN	GPIO12IN	GPIO11IN	GPIO10IN	GPIO9IN	GPIO8IN

Bits	Field Name	Description	Type	Reset Off
7	GPIO15IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
6	GPIO14IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
5	GPIO13IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
4	GPIO12IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
3	GPIO11IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
2	GPIO10IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
1	GPIO9IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
0	GPIO8IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		

Table 11-6. GPIODATAIN3

Address Offset	0x02		
Physical Address	0x0000 009A	**Instance**	INT_SCGPIO
Description	This GPIODATAIN3 data-input register registers data read from the GPIO[16:17] pins. This data-input register is a read-only register. Input data is sampled synchronously with the interface clock and captured in the data-input register synchronously with the OCP bus clock.		
Type	R		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						CPIO17IN	GPIO16IN

Bits	Field Name	Description	Type	Reset Off
7:2	Reserved	Read returns 0.	R	0x00
1	CPIO17IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		
0	GPIO16IN		R	0
		Read 0x0: GPIO input is 0.		
		Read 0x1: GPIO input is 1.		

Table 11-7. GPIODATADIR1

Address Offset	0x03		
Physical Address	0x0000 009B	**Instance**	INT_SCGPIO
Description	This GPIODATADIRA data direction register enables the I/O capabilities of the pin by setting the direction (GPIODIR). At reset, all the GPIO[0:7] related pins are configured as inputs, and output capabilities are disabled. This register is not used in the module; its only function is to carry the configuration of the pads.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7DIR	GPIO6DIR	GPIO5DIR	GPIO4DIR	GPIO3DIR	GPIO2DIR	GPIO1DIR	GPIO0DIR

Bits	Field Name	Description	Type	Reset Off
7	GPIO7DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
6	GPIO6DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
5	GPIO5DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
4	GPIO4DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
3	GPIO3DIR		RW	0
		0x0: GPIO direction is input.		

Bits	Field Name	Description	Type	Reset Off
		0x1: GPIO direction is output.		
2	GPIO2DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
1	GPIO1DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
0	GPIO0DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		

Table 11-8. GPIODATADIR2

Address Offset	0x04		
Physical Address	0x0000 009C	**Instance**	INT_SCGPIO
Description	This GPIODATADIR2 data direction register enables the I/O capabilities of the pin by setting the direction (GPIODIR). At reset, all the GPIO[8:15] related pins are configured as inputs, and output capabilities are disabled. This register is not used in the module; its only function is to carry the configuration of the pads.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15DIR	GPIO14DIR	GPIO13DIR	GPIO12DIR	GPIO11DIR	GPIO10DIR	GPIO9DIR	GPIO8DIR

Bits	Field Name	Description	Type	Reset Off
7	GPIO15DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
6	GPIO14DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
5	GPIO13DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
4	GPIO12DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
3	GPIO11DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
2	GPIO10DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
1	GPIO9DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
0	GPIO8DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		

Table 11-9. GPIODATADIR3

Address Offset	0x05		
Physical Address	0x0000 009D	**Instance**	INT_SCGPIO
Description	This GPIODATADIR3 data direction register enables the I/O capabilities of the pin by setting the direction (GPIODIR). At reset, all the GPIO[16:17]-related pins are configured as inputs, and output capabilities are disabled. This register is not used in the module; its only function is to carry the configuration of the pads.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17DIR	GPIO16DIR

Bits	Field Name	Description	Type	Reset Off
7:2	Reserved	Read returns 0.	R	0x00
1	GPIO17DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		
0	GPIO16DIR		RW	0
		0x0: GPIO direction is input.		
		0x1: GPIO direction is output.		

Table 11-10. GPIODATAOUT1

Address Offset	0x06		
Physical Address	0x0000 009E	**Instance**	INT_SCGPIO
Description	This GPIODATAOUT1 data-output register sets the value of the GPIO[0:7] output pins. Data is written to the data-output register synchronously with the OCP clock. The data loaded in the data-output register is set at the output GPIO pins synchronously with the rising edge of the OCP clock.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7OUT	GPIO6OUT	GPIO5OUT	GPIO4OUT	GPIO3OUT	GPIO2OUT	GPIO1OUT	GPIO0OUT

Bits	Field Name	Description	Type	Reset Off
7	GPIO7OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
6	GPIO6OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
5	GPIO5OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
4	GPIO4OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
3	GPIO3OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		

Bits	Field Name	Description	Type	Reset Off
2	GPIO2OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
1	GPIO1OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
0	GPIO0OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		

Table 11-11. GPIODATAOUT2

Address Offset	0x07		
Physical Address	0x0000 009F	**Instance**	INT_SCGPIO
Description	This GPIODATAOUT2 data-output register sets the value of the GPIO[8:15] output pins. Data is written to the data-output register synchronously with the OCP clock. Data loaded in the data-output register is set at the output GPIO pins synchronously with the rising edge of the OCP clock.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15OUT	GPIO14OUT	GPIO13OUT	GPIO12OUT	GPIO11OUT	GPIO10OUT	GPIO9OUT	GPIO8OUT

Bits	Field Name	Description	Type	Reset Off
7	GPIO15OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
6	GPIO14OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
5	GPIO13OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
4	GPIO12OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
3	GPIO11OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
2	GPIO10OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
1	GPIO9OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
0	GPIO8OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		

Table 11-12. GPIODATAOUT3

Address Offset	0x08		
Physical Address	0x0000 00A0	**Instance**	INT_SCGPIO
Description	This GPIODATAOUT3 data-output register sets the value of the GPIO[16:17] output pins. Data is written to the data-output register synchronously with the OCP clock. Data loaded in the data-output register is set at the output GPIO pins synchronously with the rising edge of the OCP clock.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17OUT	GPIO16OUT

Bits	Field Name	Description	Type	Reset Off
7:2	Reserved	Read returns 0.	R	0x00
1	GPIO17OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		
0	GPIO16OUT		RW	0
		0x0: GPIO output is set to 0.		
		0x1: GPIO output is set to 1.		

Table 11-13. CLEARGPIODATAOUT1

Address Offset	0x09		
Physical Address	0x0000 00A1	**Instance**	INT_SCGPIO
Description	A write operation in the CLEAR data-output register clears the corresponding bit in this data-output register when the value written is 1; a write of 0 has no effect (see Section 11.5.1.2, *Clear Instruction*). A read of this CLEAR data-output register returns the value of the data-output register.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7OUT	GPIO6OUT	GPIO5OUT	GPIO4OUT	GPIO3OUT	GPIO2OUT	GPIO1OUT	GPIO0OUT

Bits	Field Name	Description	Type	Reset Off
7	GPIO7OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 0.		
6	GPIO6OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 0.		
5	GPIO5OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 0.		
4	GPIO4OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 0.		
3	GPIO3OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 0.		

Bits	Field Name	Description	Type	Reset Off
2	GPIO2OUT	0x0: No action 0x1: GPIO output is set to 0.	RW	0
1	GPIO1OUT	0x0: No action 0x1: GPIO output is set to 0.	RW	0
0	GPIO0OUT	0x0: No action 0x1: GPIO output is set to 0.	RW	0

Table 11-14. CLEARGPIODATAOUT2

Address Offset	0x0A		
Physical Address	0x0000 00A2	**Instance**	INT_SCGPIO
Description	A write operation in this CLEAR data-output register clears the corresponding bit in the data-output register when the value written is 1; a write of 0 has no effect (see Section 11.5.1.2, *Clear Instruction*). A read of this CLEAR data-output register returns the value of the data-output register.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15OUT	GPIO14OUT	GPIO13OUT	GPIO12OUT	GPIO11OUT	GPIO10OUT	GPIO9OUT	GPIO8OUT

Bits	Field Name	Description	Type	Reset Off
7	GPIO15OUT	0x0: No action 0x1: GPIO output is set to 0.	RW	0
6	GPIO14OUT	0x0: No action 0x1: GPIO output is set to 0.	RW	0
5	GPIO13OUT	0x0: No action 0x1: GPIO output is set to 0.	RW	0
4	GPIO12OUT	0x0: No action 0x1: GPIO output is set to 0.	RW	0
3	GPIO11OUT	0x0: No action 0x1: GPIO output is set to 0.	RW	0
2	GPIO10OUT	0x0: No action 0x1: GPIO output is set to 0.	RW	0
1	GPIO9OUT	0x0: No action 0x1: GPIO output is set to 0.	RW	0
0	GPIO8OUT	0x0: No action 0x1: GPIO output is set to 0.	RW	0

Table 11-15. CLEARGPIODATAOUT3

Address Offset	0x0B		
Physical Address	0x0000 00A3	**Instance**	INT_SCGPIO
Description	A write operation in this CLEAR data-output register clears the corresponding bit in the data-output register when the value written is 1; a write of 0 has no effect (see Section 11.5.1.2, *Clear Instruction*). A read of this CLEAR data-output register returns the value of the data-output register.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17OUT	GPIO16OUT

Bits	Field Name	Description	Type	Reset Off
7:2	Reserved	Read returns 0.	R	0x00
1	GPIO17OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 0.		
0	GPIO16OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 0.		

Table 11-16. SETGPIODATAOUT1

Address Offset	0x0C		
Physical Address	0x0000 00A4	**Instance**	INT_SCGPIO
Description	A write operation in this SET data-output register sets the corresponding bit in the data-output register when the value written is 1; a write of 0 has no effect (see Section 11.5.1.3, *Set Instruction*). A read of this SET data-output register returns the value of the data-output register.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7OUT	GPIO6OUT	GPIO5OUT	GPIO4OUT	GPIO3OUT	GPIO2OUT	GPIO1OUT	GPIO0OUT

Bits	Field Name	Description	Type	Reset Off
7	GPIO7OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 1.		
6	GPIO6OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 1.		
5	GPIO5OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 1.		
4	GPIO4OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 1.		
3	GPIO3OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 1.		

Bits	Field Name	Description	Type	Reset Off
2	GPIO2OUT	0x0: No action 0x1: GPIO output is set to 1.	RW	0
1	GPIO1OUT	0x0: No action 0x1: GPIO output is set to 1.	RW	0
0	GPIO0OUT	0x0: No action 0x1: GPIO output is set to 1.	RW	0

Table 11-17. SETGPIODATAOUT2

Address Offset	0x0D		
Physical Address	0x0000 00A5	**Instance**	INT_SCGPIO
Description	A write operation in this SET data-output register sets the corresponding bit in the data-output register when the value written is 1; a write of 0 has no effect (see Section 11.5.1.3, *Set Instruction*). A read of this SET data-output register returns the value of the data-output register.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15OUT	GPIO14OUT	GPIO13OUT	GPIO12OUT	GPIO11OUT	GPIO10OUT	GPIO9OUT	GPIO8OUT

Bits	Field Name	Description	Type	Reset Off
7	GPIO15OUT	0x0: No action 0x1: GPIO output is set to 1.	RW	0
6	GPIO14OUT	0x0: No action 0x1: GPIO output is set to 1.	RW	0
5	GPIO13OUT	0x0: No action 0x1: GPIO output is set to 1.	RW	0
4	GPIO12OUT	0x0: No action 0x1: GPIO output is set to 1.	RW	0
3	GPIO11OUT	0x0: No action 0x1: GPIO output is set to 1.	RW	0
2	GPIO10OUT	0x0: No action 0x1: GPIO output is set to 1.	RW	0
1	GPIO9OUT	0x0: No action 0x1: GPIO output is set to 1.	RW	0
0	GPIO8OUT	0x0: No action 0x1: GPIO output is set to 1.	RW	0

Table 11-18. SETGPIODATAOUT3

Address Offset	0x0E		
Physical Address	0x0000 00A6	**Instance**	INT_SCGPIO
Description	A write operation in this SET data-output register sets the corresponding bit in the data-output register when the value written is 1; a write of 0 has no effect (see Section 11.5.1.3, *Set Instruction*). A read of this SET data-output register returns the value of the data-output register.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17OUT	GPIO16OUT

Bits	Field Name	Description	Type	Reset Off
7:2	Reserved	Read returns 0.	R	0x00
1	GPIO17OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 1.		
0	GPIO16OUT		RW	0
		0x0: No action		
		0x1: GPIO output is set to 1.		

Table 11-19. GPIO_DEBEN1

Address Offset	0x0F		
Physical Address	0x0000 00A7	**Instance**	INT_SCGPIO
Description	This debouncing enable register enables/disables the debouncing feature for each input line.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7DEB	GPIO6DEB	GPIO5DEB	GPIO4DEB	GPIO3DEB	GPIO2DEB	GPIO1DEB	GPIO0DEB

Bits	Field Name	Description	Type	Reset Off
7	GPIO7DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
6	GPIO6DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
5	GPIO5DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
4	GPIO4DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
3	GPIO3DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
2	GPIO2DEB		RW	0
		0x0: GPIO debounce is not set.		

Bits	Field Name	Description	Type	Reset Off
		0x1: GPIO debounce is set.		
1	GPIO1DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
0	GPIO0DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		

Table 11-20. GPIO_DEBEN2

Address Offset	0x10		
Physical Address	0x0000 00A8	**Instance**	INT_SCGPIO
Description	This debouncing enable register enables/disables debouncing for each input line.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15DEB	GPIO14DEB	GPIO13DEB	GPIO12DEB	GPIO11DEB	GPIO10DEB	GPIO9DEB	GPIO8DEB

Bits	Field Name	Description	Type	Reset Off
7	GPIO15DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
6	GPIO14DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
5	GPIO13DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
4	GPIO12DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
3	GPIO11DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
2	GPIO10DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
1	GPIO9DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
0	GPIO8DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		

Table 11-21. GPIO_DEBEN3

Address Offset	0x11		
Physical Address	0x0000 00A9	**Instance**	INT_SCGPIO
Description	This debouncing enable register enables/disables the debouncing feature for each input line.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17DEB	GPIO16DEB

Bits	Field Name	Description	Type	Reset Off
7:2	Reserved	Read returns 0.	R	0x00
1	GPIO17DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		
0	GPIO16DEB		RW	0
		0x0: GPIO debounce is not set.		
		0x1: GPIO debounce is set.		

Table 11-22. GPIO_CTRL

Address Offset	0x12		
Physical Address	0x0000 00AA	**Instance**	INT_SCGPIO
Description	This GPIO_CTRL GPIO control register controls card-detection behavior and to power on/off the GPIO module GPIO_ON field. Reserved fields are read/write (can be used as a spare).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED_S5	RESERVED_S4	RESERVED_S3	RESERVED_S2	RESERVED_S1	GPIO_ON	GPIO1CD2	GPIO0CD1

Bits	Field Name	Description	Type	Reset Off
7	Reserved	Reserved for spare	RW	0
6	Reserved	Reserved for spare	RW	0
5	Reserved	Reserved for spare	RW	0
4	Reserved	Reserved for spare	RW	0
3	Reserved	Reserved for spare	RW	0
2	GPIO_ON		RW	1
		0x0 GPIO module is disabled. :		
		0x1 GPIO module is enabled. :		
1	GPIO1CD2		RW	0
		0x0 Card detect 2 feature is disabled. :		
		0x1 Card detect 2 feature is enabled. :		

Bits	Field Name	Description	Type	Reset Off
0	GPIO0CD1	0x0 Card detect 1 feature is disabled. : 0x1 Card detect 1 feature is enabled. :	RW	0

Table 11-23. GPIOPUPDCTR1

Address Offset	0x13		
Physical Address	0x0000 00AB	**Instance**	INT_SCGPIO
Description	GPIO pullup/pulldown control register 1 By default, pulldowns are enabled to avoid leakage when the GPIOs are not connected externally. Therefore, because GPIO3 is muxed with the DATA5 pin of USB ULPI and this functionality is the default, the default for this GPIO is not pullup- and pulldown-enabled.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO3PU	GPIO3PD	GPIO2PU	GPIO2PD	GPIO1PU	GPIO1PD	GPIO0PU	GPIO0PD

Bits	Field Name	Description	Type	Reset Off
7	GPIO3PU	0x0: GPIO pullup is disabled. 0x1: GPIO pullup is enabled.	RW	0
6	GPIO3PD	0x0: GPIO pulldown is disabled. 0x1: GPIO pulldown is enabled.	RW	0
5	GPIO2PU	0x0: GPIO pullup is disabled. 0x1: GPIO pullup is enabled.	RW	0
4	GPIO2PD	0x0: GPIO pulldown is disabled. 0x1: GPIO pulldown is enabled.	RW	0
3	GPIO1PU	0x0: GPIO pullup is disabled. 0x1: GPIO pullup is enabled.	RW	0
2	GPIO1PD	0x0: GPIO pulldown is disabled. 0x1: GPIO pulldown is enabled.	RW	0
1	GPIO0PU	0x0: GPIO pullup is disabled. 0x1: GPIO pullup is enabled.	RW	0
0	GPIO0PD	0x0: GPIO pulldown is disabled. 0x1: GPIO pulldown is enabled.	RW	0

Table 11-24. GPIOPUPDCTR2

Address Offset	0x14		
Physical Address	0x0000 00AC	**Instance**	INT_SCGPIO
Description	GPIO pullup/pulldown control register 2 By default, pulldowns are enabled to avoid leakage when the GPIOs are not connected externally. Therefore, because GPIO4/GPIO5 are muxed with the DATA6/DATA7 pins, respectively, of USB ULPI and because USB/USPI functionality is the default, the defaults for these GPIOs are not pullup- and pulldown-enabled.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7PU	GPIO7PD	GPIO6PU	GPIO6PD	GPIO5PU	GPIO5PD	GPIO4PU	GPIO4PD

Bits	Field Name	Description	Type	Reset Off
7	GPIO7PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
6	GPIO7PD		RW	1
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		
5	GPIO6PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
4	GPIO6PD		RW	1
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		
3	GPIO5PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
2	GPIO5PD		RW	1
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		
1	GPIO4PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
0	GPIO4PD		RW	1
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		

Table 11-25. GPIOPUPDCTR3

Address Offset	0x15		
Physical Address	0x0000 00AD	**Instance**	INT_SCGPIO
Description	GPIO pullup/pulldown control register 3 By default, pulldowns are enabled to avoid leakage when the GPIOs are not connected externally. Therefore, because GPIO9/GPIO10/GPIO11 are muxed with the STP/DIR/NXT pins, respectively, of USB ULPI and because USB/USPI functionality is the default, the default for these GPIOs is not pullup- and pulldown-enabled.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO11PU	GPIO11PD	GPIO10PU	GPIO10PD	GPIO9PU	GPIO9PD	GPIO8PU	GPIO8PD

Bits	Field Name	Description	Type	Reset Off
7	GPIO11PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
6	GPIO11PD		RW	0
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		
5	GPIO10PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
4	GPIO10PD		RW	0
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		
3	GPIO9PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
2	GPIO9PD		RW	0
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		
1	GPIO8PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
0	GPIO8PD		RW	1
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		

Table 11-26. GPIOPUPDCTR4

Address Offset	0x16		
Physical Address	0x0000 00AE	**Instance**	INT_SCGPIO
Description	GPIO pullup/pulldown control register 4 By default, pulldowns are enabled to avoid leakage when the GPIOs are not connected externally. Therefore, because GPIO12/GPIO14 are muxed with the DATA3/DATA4 pins of USB ULPI and because this functionality is the default, the default for these GPIOs is not pullup- and pulldown-enabled.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15PU	GPIO15PD	GPIO14PU	GPIO14PD	GPIO13PU	GPIO13PD	GPIO12PU	GPIO12PD

Bits	Field Name	Description	Type	Reset Off
7	GPIO15PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
6	GPIO15PD		RW	1
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		
5	GPIO14PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
4	GPIO14PD		RW	1
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		
3	GPIO13PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
2	GPIO13PD		RW	1
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		
1	GPIO12PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
0	GPIO12PD		RW	1
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		

Table 11-27. GPIOPUPDCTR5

Address Offset	0x17		
Physical Address	0x0000 00AF	**Instance**	INT_SCGPIO
Description	GPIO pullup/pulldown control register 5 By default, pulldowns are enabled to avoid leakage when the GPIOs are not externally connected.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED_6	RESERVED_5	RESERVED_4	RESERVED_3	GPIO17PU	GPIO17PD	GPIO16PU	GPIO16PD

Bits	Field Name	Description	Type	Reset Off
7	Reserved	Read returns 0.	R	0
6	Reserved	Read returns 0.	R	0
5	Reserved	Read returns 0.	R	0
4	Reserved	Read returns 0.	R	0
3	GPIO17PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
2	GPIO17PD		RW	1
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		
1	GPIO16PU		RW	0
		0x0: GPIO pullup is disabled.		
		0x1: GPIO pullup is enabled.		
0	GPIO16PD		RW	1
		0x0: GPIO pulldown is disabled.		
		0x1: GPIO pulldown is enabled.		

Table 11-28. GPIO_ISR1A

Address Offset	0x19		
Physical Address	0x0000 00B1	**Instance**	INT_SCGPIO
Description	This ISR1A interrupt status register determines which input GPIO[0:7] pins trigger the interrupt line gpio_int1_n request. As shown in this table, bit 0 corresponds to po_pad_gpio[0], bit 1 to po_pad_gpio[1], etc. When a bit in this register is set to 1, the corresponding GPIO pin requests the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR1 interrupt status register. If the user writes 0 to a bit in this register, the value stays the same when in COR mode. This ISR1A interrupt status register is synchronous with the interface OCP clock. A read of 1 in any bit field means that the corresponding interrupt event is active on interrupt request line 1.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7ISR1	GPIO6ISR1	GPIO5ISR1	GPIO4ISR1	GPIO3ISR1	GPIO2ISR1	GPIO1ISR1	GPIO0ISR1

Bits	Field Name	Description	Type	Reset Off
7	GPIO7ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line.		
		0x1: GPIO hardware interrupt is active on processor 1 request line.		
6	GPIO6ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line.		

Bits	Field Name	Description	Type	Reset Off
		0x1: GPIO hardware interrupt is active on processor 1 request line.		
5	GPIO5ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line.		
		0x1: GPIO hardware interrupt is active on processor 1 request line.		
4	GPIO4ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line.		
		0x1: GPIO hardware interrupt is active on processor 1 request line.		
3	GPIO3ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line.		
		0x1: GPIO hardware interrupt is active on processor 1 request line.		
2	GPIO2ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line.		
		0x1: GPIO hardware interrupt is active on processor 1 request line.		
1	GPIO1ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line.		
		0x1: GPIO hardware interrupt is active on processor 1 request line.		
0	GPIO0ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line.		
		0x1: GPIO hardware interrupt is active on processor 1 request line.		

Table 11-29. GPIO_ISR2A

Address Offset	0x1A		
Physical Address	0x0000 00B2	**Instance**	INT_SCGPIO
Description	This ISR2A interrupt status register determines which input GPIO[8:15] pins trigger the interrupt line gpio_int1_n request. As shown in this table, bit 0 corresponds to po_pad_gpio[8], bit 1 to po_pad_gpio[9], etc. When a bit in this register is set to 1, the corresponding GPIO pin requests the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR2 interrupt status register. If the user writes 0 to a bit in this register, the value stays the same when in change-on-read (COR) mode. This interrupt status register is synchronous with the interface OCP clock. A read of 1 in any bit field means that the corresponding interrupt event is active on interrupt request line 1.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15ISR2	GPIO14ISR2	GPIO13ISR2	GPIO12ISR2	GPIO11ISR2	GPIO10ISR2	GPIO9ISR2	GPIO8ISR2

Bits	Field Name	Description	Type	Reset Off
7	GPIO15ISR2		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line.		
		0x1: GPIO hardware interrupt is active on processor 1 request line.		
6	GPIO14ISR2		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line.		
		0x1: GPIO hardware interrupt is active on processor 1 request line.		
5	GPIO13ISR2		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line.		
		0x1: GPIO hardware interrupt is active on processor 1 request line.		
4	GPIO12ISR2		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line.		
		0x1: GPIO hardware interrupt is active on processor 1 request line.		
3	GPIO11ISR2		RW	0

Bits	Field Name	Description	Type	Reset Off
		0x0: GPIO hardware interrupt is inactive on processor 1 request line. 0x1: GPIO hardware interrupt is active on processor 1 request line.		
2	GPIO10ISR2		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line. 0x1: GPIO hardware interrupt is active on processor 1 request line.		
1	GPIO9ISR2		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line. 0x1: GPIO hardware interrupt is active on processor 1 request line.		
0	GPIO8ISR2		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line. 0x1: GPIO hardware interrupt is active on processor 1 request line.		

Table 11-30. GPIO_ISR3A

Address Offset	0x1B		
Physical Address	0x0000 00B3	**Instance**	INT_SCGPIO
Description	This ISR3A interrupt status register determines which input GPIO[16:17] pins trigger the interrupt line gpio_int1_n request. As shown in this table, bit 0 corresponds to po_pad_gpio[16], bit 1 to po_pad_gpio[17], etc. When a bit in this register is set to 1, the corresponding GPIO pin requests the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR3 interrupt status register. If the user writes 0 to a bit in this register, the value stays the same when in COR mode. This interrupt status register is synchronous with the interface OCP clock. A read of 1 in any bit field means that the corresponding interrupt event is active on interrupt request line 1.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17ISR3	GPIO16ISR3

Bits	Field Name	Description	Type	Reset Off
7:2	Reserved	Read returns 0.	R	0x00
1	GPIO17ISR3			
		0x0: GPIO hardware interrupt is inactive on processor 1 request line. 0x1: GPIO hardware interrupt is active on processor 1 request line.		
0	GPIO16ISR3		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 1 request line. 0x1: GPIO hardware interrupt is active on processor 1 request line.		

Table 11-31. GPIO_IMR1A

Address Offset	0x1C		
Physical Address	0x0000 00B4	**Instance**	INT_SCGPIO
Description	This IMR1A interrupt mask register allows masking/unmasking of the expected transition on input GPIO[0:7] from generating an interrupt request on gpio_int1_n. Interrupt masking registers are programmed synchronously with the interface OCP clock. Writing 0 in any bit field unmasks the corresponding GPIO interrupt event on interrupt request line 1. By default, all interrupts are masked.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7IMR1	GPIO6IMR1	GPIO5IMR1	GPIO4IMR1	GPIO3IMR1	GPIO2IMR1	GPIO1IMR1	GPIO0IMR1

Bits	Field Name	Description	Type	Reset Off
7	GPIO7IMR1		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
6	GPIO6IMR1		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
5	GPIO5IMR1		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
4	GPIO4IMR1		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
3	GPIO3IMR1		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
2	GPIO2IMR1		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
1	GPIO1IMR1		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
0	GPIO0IMR1		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		

Table 11-32. GPIO_IMR2A

Address Offset	0x1D		
Physical Address	0x0000 00B5	**Instance**	INT_SCGPIO
Description	This IMR12A interrupt mask register allows masking/unmasking of the expected transition on input GPIO[8:15] from generating an interrupt request on gpio_int1_n. Interrupt masking registers are programmed synchronously with the interface OCP clock. Writing 0 in any bit field unmasks the corresponding GPIO interrupt event on interrupt request line 1. By default, all interrupts are masked.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15IMR2	GPIO14IMR2	GPIO13IMR2	GPIO12IMR2	GPIO11IMR2	GPIO10IMR2	GPIO9IMR2	GPIO08MR2

Bits	Field Name	Description	Type	Reset Off
7	GPIO15IMR2		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
6	GPIO14IMR2		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
5	GPIO13IMR2		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
4	GPIO12IMR2		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
3	GPIO11IMR2		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
2	GPIO10IMR2		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
1	GPIO9IMR2		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
0	GPIO8IMR2		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		

Table 11-33. GPIO_IMR3A

Address Offset	0x1E		
Physical Address	0x0000 00B6	**Instance**	INT_SCGPIO
Description	This IMR3A interrupt mask register allows masking/unmasking of the expected transition on input GPIO[16:17] from generating an interrupt request on gpio_int1_n. Interrupt masking registers are programmed synchronously with the interface OCP clock. Writing 0 in any bit field unmasks the corresponding GPIO interrupt event on interrupt request line 1. By default, all interrupts are masked.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17IMR3	GPIO16IMR3

Bits	Field Name	Description	Type	Reset Off
7:2	Reserved	Read returns 0.	R	0x00
			RW	1
1	GPIO17IMR3			
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		
0	GPIO16IMR3		RW	1
		0x0: GPIO event is not masked on processor 1 request line.		
		0x1: GPIO event is masked on processor 1 request line.		

Table 11-34. GPIO_ISR1B

Address Offset	0x1F		
Physical Address	0x0000 00B7	**Instance**	INT_SCGPIO
Description	This ISR1B interrupt status register determines which input GPIO[0:7] pins trigger the interrupt line gpio_int2_n request. As shown in this table, bit 0 corresponds to po_pad_gpio[0], bit 1 to po_pad_gpio[7], etc. When a bit in this register is set to 1, the corresponding GPIO pin requests the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR1 interrupt status register. If the user writes 0 to a bit in this register, the value stays the same when in COR mode. This ISR1B interrupt status register is synchronous with the interface OCP clock. A read of 1 in any bit field means that the corresponding interrupt event is active on the interrupt request line 2.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7ISR1	GPIO6ISR1	GPIO5ISR1	GPIO4ISR1	GPIO3ISR1	GPIO2ISR1	GPIO1ISR1	GPIO0ISR1

Bits	Field Name	Description	Type	Reset Off
7	GPIO7ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		
		0x1: GPIO hardware interrupt is active on processor 2 request line.		
6	GPIO6ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		
		0x1: GPIO hardware interrupt is active on processor 2 request line.		
5	GPIO5ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		
		0x1: GPIO hardware interrupt is active on processor 2 request line.		
4	GPIO4ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		

Bits	Field Name	Description	Type	Reset Off
		0x1: GPIO hardware interrupt is active on processor 2 request line.		
3	GPIO3ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		
		0x1: GPIO hardware interrupt is active on processor 2 request line.		
2	GPIO2ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		
		0x1: GPIO hardware interrupt is active on processor 2 request line.		
1	GPIO1ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		
		0x1: GPIO hardware interrupt is active on processor 2 request line.		
0	GPIO0ISR1		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		
		0x1: GPIO hardware interrupt is active on processor 2 request line.		

Table 11-35. GPIO_ISR2B

Address Offset	0x20		
Physical Address	0x0000 00B8	**Instance**	INT_SCGPIO
Description	This ISR2B interrupt status register determines which input GPIO[8:15] pins trigger the interrupt line gpio_int2_n request. As shown in this table, bit 0 corresponds to po_pad_gpio[8], bit 1 to po_pad_gpio[9], etc. When a bit in this register is set to 1, the corresponding GPIO pin requests the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR2 interrupt status register. If the user writes 0 to a bit in this register, the value stays the same when in COR mode. This ISR2B interrupt status register is synchronous with the interface OCP clock. A read of 1 in any bit field means that the corresponding interrupt event is active on the interrupt request line 2.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15ISR2	GPIO14ISR2	GPIO13ISR2	GPIO12ISR2	GPIO11ISR2	GPIO10ISR2	GPIO9ISR2	GPIO08MR2

Bits	Field Name	Description	Type	Reset Off
7	GPIO15ISR2		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		
		0x1: GPIO hardware interrupt is active on processor 2 request line.		
6	GPIO14ISR2		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		
		0x1: GPIO hardware interrupt is active on processor 2 request line.		
5	GPIO13ISR2		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		
		0x1: GPIO hardware interrupt is active on processor 2 request line.		
4	GPIO12ISR2		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		
		0x1: GPIO hardware interrupt is active on processor 2 request line.		
3	GPIO11ISR2		RW	0
		0x0: GPIO hardware interrupt is inactive on processor 2 request line.		
		0x1: GPIO hardware interrupt is active on processor 2 request line.		

Bits	Field Name	Description	Type	Reset Off
2	GPIO10ISR2	0x0: GPIO hardware interrupt is inactive on processor 2 request line. 0x1: GPIO hardware interrupt is active on processor 2 request line.	RW	0
1	GPIO9ISR2	0x0: GPIO hardware interrupt is inactive on processor 2 request line. 0x1: GPIO hardware interrupt is active on processor 2 request line.	RW	0
0	GPIO8ISR2	0x0: GPIO hardware interrupt is inactive on processor 2 request line. 0x1: GPIO hardware interrupt is active on processor 2 request line.	RW	0

Table 11-36. GPIO_ISR3B

Address Offset	0x21		
Physical Address	0x0000 00B9	**Instance**	INT_SCGPIO
Description	This ISR3B interrupt status register determines which input GPIO[16:17] pins trigger the interrupt line gpio_int2_n request. As shown in this table, bit 0 corresponds to po_pad_gpio[16], bit 1 to po_pad_gpio[17], etc. When a bit in this register is set to 1, the corresponding GPIO pin requests the interrupt. However, the user cannot generate an interrupt by writing 1 to the ISR3 interrupt status register. If the user writes 0 to a bit in this register, the value stays the same when in COR mode. This ISR3B interrupt status register is synchronous with the interface OCP clock. A read of 1 in any bit field means that the corresponding interrupt event is active on the interrupt request line 2.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17ISR3	GPIO16ISR3

Bits	Field Name	Description	Type	Reset Off
7:2	Reserved	Read returns 0.	R	0x00
1	GPIO17ISR3	0x0 : GPIO hardware interrupt is inactive on processor 2 request line. 0x1 : GPIO hardware interrupt is active on processor 2 request line.	RW	0
0	GPIO16ISR3	0x0 : GPIO hardware interrupt is inactive on processor 2 request line. 0x1 : GPIO hardware interrupt is active on processor 2 request line.	RW	0

Table 11-37. GPIO_IMR1B

Address Offset	0x22		
Physical Address	0x0000 00BA	**Instance**	INT_SCGPIO
Description	This IMR1B interrupt mask register allows masking/unmasking of the expected transition on input GPIO[0:7] from generating an interrupt request on gpio_int2_n. Interrupt masking registers are programmed synchronously with the interface OCP clock. Writing 0 in any bit field unmasks the corresponding GPIO interrupt event on the interrupt request line 2. By default, all interrupts are masked.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7IMR1	GPIO6IMR1	GPIO5IMR1	GPIO4IMR1	GPIO3IMR1	GPIO2IMR1	GPIO1IMR1	GPIO0IMR1

Bits	Field Name	Description	Type	Reset Off
7	GPIO7IMR1		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
6	GPIO6IMR1		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
5	GPIO5IMR1		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
4	GPIO4IMR1		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
3	GPIO3IMR1		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
2	GPIO2IMR1		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
1	GPIO1IMR1		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
0	GPIO0IMR1		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		

Table 11-38. GPIO_IMR2B

Address Offset	0x23		
Physical Address	0x0000 00BB	**Instance**	INT_SCGPIO
Description	This IMR2B interrupt mask register allows masking/unmasking of the expected transition on input GPIO[8:15] from generating an interrupt request on gpio_int2_n. Interrupt masking registers are programmed synchronously with the interface OCP clock. Writing 0 in any bit field unmasks the corresponding GPIO interrupt event on the interrupt request line 2. By default, all interrupts are masked.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15IMR2	GPIO14IMR2	GPIO13IMR2	GPIO12IMR2	GPIO11IMR2	GPIO10IMR2	GPIO9IMR2	GPIO08MR2

Bits	Field Name	Description	Type	Reset Off
7	GPIO15IMR2		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
6	GPIO14IMR2		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
5	GPIO13IMR2		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
4	GPIO12IMR2		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
3	GPIO11IMR2		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
2	GPIO10IMR2		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
1	GPIO9IMR2		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
0	GPIO8IMR2		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		

Table 11-39. GPIO_IMR3B

Address Offset	0x24		
Physical Address	0x0000 00BC	**Instance**	INT_SCGPIO
Description	This IMR3B interrupt mask register allows masking/unmasking of the expected transition on input GPIO[16:17] from generating an interrupt request on gpio_int2_n. Interrupt masking registers are programmed synchronously with the interface OCP clock. Writing 0 in any bit field unmasks the corresponding GPIO interrupt event on the interrupt request line 2. By default, all interrupts are masked.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved						GPIO17IMR3	GPIO16IMR3

Bits	Field Name	Description	Type	Reset Off
7:2	Reserved	Read returns 0.	R	0x00
1	GPIO17IMR3		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		
0	GPIO16IMR3		RW	1
		0x0: GPIO event is not masked on processor 2 request line.		
		0x1: GPIO event is masked on processor 2 request line.		

Table 11-40. GPIO_EDR1

Address Offset	0x28		
Physical Address	0x0000 00C0	**Instance**	INT_SCGPIO
Description	This GPIO_EDR1 interrupt edge-detection register allows definition of the edge expected to trigger an interrupt request for each external GPIO[0:3] pin configured as input. The interrupt request can be generated from a high-to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions accruing (bits are 11). To disable edge detection, reset (00) the relevant bits corresponding to the GPIO.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO3RISING	GPIO3FALLING	GPIO2RISING	GPIO2FALLING	GPIO1RISING	GPIO1FALLING	GPIO0RISING	GPIO0FALLING

Bits	Field Name	Description	Type	Reset Off
7	GPIO3RISING		RW	0
		0x0: GPIO rising detection is disabled.		
		0x1: GPIO rising detection is enabled.		
6	GPIO3FALLING		RW	0
		0x0: GPIO falling detection is disabled.		
		0x1: GPIO falling detection is enabled.		
5	GPIO2RISING		RW	0
		0x0: GPIO rising detection is disabled.		
		0x1: GPIO rising detection is enabled.		

Bits	Field Name	Description	Type	Reset Off
4	GPIO2FALLING		RW	0
		0x0: GPIO falling detection is disabled.		
		0x1: GPIO falling detection is enabled.		
3	GPIO1RISING		RW	0
		0x0: GPIO rising detection is disabled.		
		0x1: GPIO rising detection is enabled.		
2	GPIO1FALLING		RW	0
		0x0: GPIO falling detection is disabled.		
		0x1: GPIO falling detection is enabled.		
1	GPIO0RISING		RW	0
		0x0: GPIO rising detection is disabled.		
		0x1: GPIO rising detection is enabled.		
0	GPIO0FALLING		RW	0
		0x0: GPIO falling detection is disabled.		
		0x1: GPIO falling detection is enabled.		

Table 11-41. GPIO_EDR2

Address Offset	0x29		
Physical Address	0x0000 00C1	**Instance**	INT_SCGPIO
Description	This GPIO_EDR2 interrupt edge-detection register allows definition of the edge expected to trigger an interrupt request for each external GPIO[4:7] pin configured as input. The interrupt request can be generated from a high-to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions accruing (bits are 11). To disable edge detection, reset (00) the relevant bits corresponding to the GPIO.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO7RISING	GPIO7FALLING	GPIO6RISING	GPIO6FALLING	GPIO5RISING	GPIO5FALLING	GPIO4RISING	GPIO4FALLING

Bits	Field Name	Description	Type	Reset Off
7	GPIO7RISING		RW	0
		0x0: GPIO rising detection is disabled.		
		0x1: GPIO rising detection is enabled.		
6	GPIO7FALLING		RW	0
		0x0: GPIO falling detection is disabled.		
		0x1: GPIO falling detection is enabled.		
5	GPIO6RISING		RW	0
		0x0: GPIO rising detection is disabled.		
		0x1: GPIO rising detection is enabled.		
4	GPIO6FALLING		RW	0
		0x0: GPIO falling detection is disabled.		
		0x1: GPIO falling detection is enabled.		
3	GPIO5RISING		RW	0
		0x0: GPIO rising detection is disabled.		
		0x1: GPIO rising detection is enabled.		
2	GPIO5FALLING		RW	0

Bits	Field Name	Description	Type	Reset Off
		0x0: GPIO falling detection is disabled. 0x1: GPIO falling detection is enabled.		
1	GPIO4RISING		RW	0
		0x0: GPIO rising detection is disabled. 0x1: GPIO rising detection is enabled.		
0	GPIO4FALLING		RW	0
		0x0: GPIO falling detection is disabled. 0x1: GPIO falling detection is enabled.		

Table 11-42. GPIO_EDR3

Address Offset	0x2A		
Physical Address	0x0000 00C2	**Instance**	INT_SCGPIO
Description	This GPIO_EDR3 interrupt edge-detection register allows definition of the edge expected to trigger an interrupt request for each external GPIO[8:1] pin configured as input. The interrupt request can be generated from a high-to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions accruing (bits are 11). To disable edge detection, reset (00) the relevant bits corresponding to the GPIO.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO11RISING	GPIO11FALLING	GPIO10RISING	GPIO10FALLING	GPIO9RISING	GPIO9FALLING	GPIO8RISING	GPIO8FALLING

Bits	Field Name	Description	Type	Reset Off
7	GPIO11RISING		RW	0
		0x0: GPIO rising detection is disabled. 0x1: GPIO rising detection is enabled.		
6	GPIO11FALLING		RW	0
		0x0: GPIO falling detection is disabled. 0x1: GPIO falling detection is enabled.		
5	GPIO10RISING		RW	0
		0x0: GPIO rising detection is disabled. 0x1: GPIO rising detection is enabled.		
4	GPIO10FALLING		RW	0
		0x0: GPIO falling detection is disabled. 0x1: GPIO falling detection is enabled.		
3	GPIO9RISING		RW	0
		0x0: GPIO rising detection is disabled. 0x1: GPIO rising detection is enabled.		
2	GPIO9FALLING		RW	0
		0x0: GPIO falling detection is disabled. 0x1: GPIO falling detection is enabled.		
1	GPIO8RISING		RW	0
		0x0: GPIO rising detection is disabled. 0x1: GPIO rising detection is enabled.		
0	GPIO8FALLING		RW	0

Bits	Field Name	Description	Type	Reset Off
		0x0: GPIO falling detection is disabled. 0x1: GPIO falling detection is enabled.		

Table 11-43. GPIO_EDR4

Address Offset	0x2B		
Physical Address	0x0000 00C3	**Instance**	INT_SCGPIO
Description	This GPIO_EDR4 interrupt edge-detection register allows definition of the edge expected to trigger an interrupt request for each external GPIO[13:15] pin configured as input. The interrupt request can be generated from a high-to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions accruing (bits are 11). To disable edge detection, reset (00) the relevant bits corresponding to the GPIO.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO15RISING	GPIO15FALLING	GPIO14RISING	GPIO14FALLING	GPIO13RISING	GPIO13FALLING	GPIO12RISING	GPIO12FALLING

Bits	Field Name	Description	Type	Reset Off
7	GPIO15RISING		RW	0
		0x0: GPIO rising detection is disabled.		
		0x1: GPIO rising detection is enabled.		
6	GPIO15FALLING		RW	0
		0x0: GPIO falling detection is disabled.		
		0x1: GPIO falling detection is enabled.		
5	GPIO14RISING		RW	0
		0x0: GPIO rising detection is disabled.		
		0x1: GPIO rising detection is enabled.		
4	GPIO14FALLING		RW	0
		0x0: GPIO falling detection is disabled.		
		0x1: GPIO falling detection is enabled.		
3	GPIO13RISING		RW	0
		0x0: GPIO rising detection is disabled.		
		0x1: GPIO rising detection is enabled.		
2	GPIO13FALLING		RW	0
		0x0: GPIO falling detection is disabled.		
		0x1: GPIO falling detection is enabled.		
1	GPIO12RISING		RW	0
		0x0: GPIO rising detection is disabled.		
		0x1: GPIO rising detection is enabled.		
0	GPIO12FALLING		RW	0
		0x0: GPIO falling detection is disabled.		
		0x1: GPIO falling detection is enabled.		

Table 11-44. GPIO_EDR5

Address Offset	0x2C		
Physical Address	0x0000 00C4	**Instance**	INT_SCGPIO
Description	This GPIO_EDR interrupt edge-detection register allows definition of the edge expected to trigger an interrupt request for each external GPIO[16:17] pin configured as input. The interrupt request can be generated from a high-to-low transition (bits are 01), a low-to-high transition (bits are 10), or both transitions accruing (bits are 11). To disable edge detection, reset (00) the relevant bits corresponding to the GPIO.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved				GPIO17RISING	GPIO17FALLING	GPIO16RISING	GPIO16FALLING

Bits	Field Name	Description	Type	Reset Off
7:4	Reserved	Read returns 0.	R	0x0
3	GPIO17RISING		RW	0
		0x0 GPIO rising detection is disabled. :		
		0x1 GPIO rising detection is enabled. :		
2	GPIO17FALLING		RW	0
		0x0 GPIO falling detection is disabled. :		
		0x1 GPIO falling detection is enabled. :		
1	GPIO16RISING		RW	0
		0x0 GPIO rising detection is disabled. :		
		0x1 GPIO rising detection is enabled. :		
0	GPIO16FALLING		RW	0
		0x0 GPIO falling detection is disabled. :		
		0x1 GPIO falling detection is enabled. :		

Table 11-45. GPIO_SIH_CTRL

Address Offset	0x2D		
Physical Address	0x0000 00C5	**Instance**	INT_SCGPIO
Description	This GPIO_SIH_CTRL GPIO SIH control register lets the user disable a pending event incoming during software interrupt latency by programming 0x1 in the PENDDIS bit. Writing 0x0 in the EXCLEN bit disables exclusivity between the interrupt request lines gpio_int1_n and gpio_int2_n.The COR bit enables the clear-on-read feature, which means that any read access to the interrupt status register clears this register and releases the associated interrupt line (default value). If disabled, a read access to a specific address value clears all ISRs in the SIH.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved					COR	PENDDIS	EXCLEN

Bits	Field Name	Description	Type	Reset Off
7:3	Reserved	Read returns 0.	R	0x00
2	COR		RW	0
		0x0: Clear ISR-specific bit field when in write access mode.		
		0x1: Clear ISR when in read mode.		
1	PENDDIS		RW	0
		0x0: Pending event feature is enabled.		
		0x1: Pending event feature is disabled.		
0	EXCLEN		RW	1
		0x0: Exclusivity is disabled.		
		0x1: Exclusivity is enabled.		

Table 11-46. PMBR1

Address Offset	0x0D		
Physical Address	0x0000 0092	**Instance**	INT_SCINTBR
Description	This pad muxing bank register 1 selects GPIO mode functionality versus USB mode, PWM functionality, vibrator synchronization, and other T2 features. By default, USB is selected in case of USB muxing; otherwise, GPIO is the default selected feature.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
GPIO_PCM_DIGMICCLK		GPIO7_VIBRASYNC_PWM1		GPIO6_PWM0_MUTE		GPIO_USB	

Bits	Field Name	Description	Type	Reset
7:6	GPIO_PCM_ DIGMICCLK	GPIO16_17/Bluetooth PCM and DIG_MIC functions pad-muxing control register	RW	0x0
		0x0: (Default) GPIO16 and GPIO17 functions are enabled.		
		0x1: Bluetooth function is enabled.		
		0x2: No action		
		0x3: Digital micro function is enabled.		
5:4	GPIO7_VIBRASYNC $\overline{\text{P}}$WM1	GPIO7/VIBRASYNC/PWM1 function pad-muxing control register	RW	0x0
		0x0: (Default) GPIO7 function is enabled.		
		0x1: VIBRASYNC function is enabled.		
		0x2: No action		

Bits	Field Name	Description	Type	Reset
		0x3: PWM1 function is enabled.		
3:2	GPIO6_PWM0_MUTE	GPIO6/PWM0 and audio mute functions pad-muxing control register 0x0: (Default) GPIO6 function is enabled. 0x1: PWM0 function is enabled. 0x2: Mute function is enabled. 0x3: Reserved	RW	0x0
1:0	GPIO_USB	GPIO3/4/5/9/10/11/12/14 and USB functions pad-muxing control register 0x0: (Default) Full USB ULPI 8D function is enabled. 0x1: GPIO function is enabled on GPIO9/10/11/12/14/3/4/5 and USB 3 pin on DATA0/DATA1/DATA2. 0x2: GPIO function is enabled on GPIO9/10/11/14/3/4/5 and USB 4 pin on DATA0/DATA1/DATA2/DATA3. 0x3: GPIO function is enabled on GPIO9/10/11/12/14/3/5 and USB 4 pin on DATA0/DATA1/DATA2/DATA6. This is a 4-pin USB mode with receive mapped on DATA6.	RW	0x0

Table 11-47. PMBR2

Address Offset	0x0E		
Physical Address	0x0000 0093	**Instance**	INT_SCINTBR
Description	This pad-muxing bank register 2 selects GPIO mode functionality versus LED driver synchronization mode functionality, and GPIO8 versus UART1 functionality (GPIO8 is the default). By default, GPIO is selected. Reserved fields are read/write (can be used for spare).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED_S6	RESERVED_S5	RESERVED_S4	RESERVED_S3	RESERVED_S2	MANU_GPIO7_INTSRC	GPIO8_UART1_RXD	GPIO13_LEDSYNC

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved for spare	RW	0
6	RESERVED	Reserved for spare	RW	0
5	RESERVED	Reserved for spare	RW	0
4	RESERVED	Reserved for spare	RW	0
3	RESERVED	Reserved for spare	RW	0
2	MANU_GPIO7_INTSRC	GPIO7/USB_MANU functions pad-muxing control register When 1, the MANU pin function of USB is enabled (the USB MANU pin is connected internally to GPIO7). When 0 and when GPIO7 is selected by the PMBR1 control register, the GPIO7 function is enabled (GPIO7 is disconnected internally from GPIO7). The MANU pin muxing level is priority regarding the GPIO7 muxing level (set by the PMBR1 register).	RW	0
1	GPIO8_UART1_RXD	GPIO8/UART1_RXD functions pad-muxing control register 0x0: (Default) GPIO8 function is enabled. 0x1: UART1 function is enabled.	RW	0
0	GPIO13_LEDSYNC	GPIO13/LEDSYNC functions pad-muxing control register	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: (Default) GPIO13 function is enabled. 0x1: LEDYNC function is enabled.		

Thermal Shutdown and Hot-Die Detector

This chapter describes the thermal shutdown and hot-die detector for the device integrated power management/audio coder/decoder (codec) device.

Topic **Page**

12.1 Thermal Shutdown and Hot-Die Detector Overview

The device is equipped with a hot-die detector function that provides the host power-management software with an early warning of over-temperature conditions.

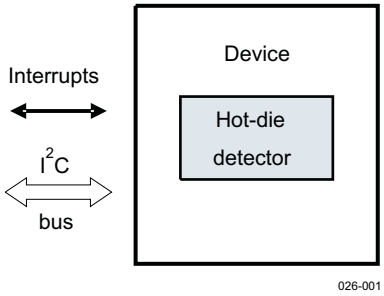
When the device is in master mode, a fail-safe protective feature is available. If corrective action is not taken, and the die temperature continues to rise, the second thermal feature, thermal shutdown, takes over and resets the system to protect it from overheating. Thermal shutdown is not available when the device is in slave mode.

12.2 Thermal Shutdown and Hot-Die Detector Environment

The device inter-integrated circuit (I^2C™) bus (see Chapter 2, *Control Interface*) is used by the host processor to access internal registers that define the operating range. See Section 12.4, *Thermal Shutdown and Hot-Die Detector Functional Description*.

Figure 12-1 is a view of the external interfaces for the hot-die detector.

Figure 12-1. Hot-Die Detector External Interfaces



12.2.1 Thermal Shutdown Internal to the Device

When the device is in master mode, thermal shutdown is an internal function that works without outside intervention. Thermal shutdown is not available in slave mode.

12.2.2 Hot-Die Detector External Interface

The hot-die detector function generates an interrupt that is visible to an external host processor. With suitable software, the host processor knows which temperature range is selected and, therefore, what temperature range is being transitioned. Interrupt status lines 1 and 2 can be selected and masked, as shown in Table 12-1, by configuring the registers in the device.

Table 12-1. Interrupt Status Line Selection and Masking

Bit	Bit Name	Register	Action
4	HOT_DIE	PWR_ISR1	Selects interrupt status line 1 to be triggered by hot-die detector thresholds
4	HOT_DIE	PWR_IMR1	Masks interrupt status line 1 from being triggered by hot-die detector thresholds
4	HOT_DIE	PWR_ISR2	Selects interrupt status line 2 to be triggered by hot-die detector thresholds
4	HOT_DIE	PWR_IMR2	Masks interrupt status line 2 from being triggered by hot-die detector thresholds

During software development, the PWR_SIR[4] HOT_DIE bit can be set to logical 1 to simulate the operation of the hot-die detector thresholds. This makes it possible to examine the operation of bit 4 in the PWR_ISR1, PWR_IMR1, PWR_ISR2, and PWR_IMR2 registers to ensure that the desired interrupt or masking operation is implemented.

The hot-die detector rising and falling thresholds can be turned on (enabled) and turned off (disabled) by configuring the registers, as shown in Table 12-2.

Table 12-2. Hot-Die Rising- and Falling-Edge Threshold Control

Bit	Bit Name	Register	Action
1	HOT_DIE_RISING	PWR_EDR2	0: Rising-edge detection disabled
			1: Rising-edge detection enabled
0	HOT_DIE_FALLING	PWR_EDR2	0: Rising-edge detection disabled
			1: Rising-edge detection enabled

The hot-die detector status can be examined when transitioning from OFF to ACTIVE power state, as shown in Table 12-3. For more information, see Chapter 5, *Resets and Power Management*.

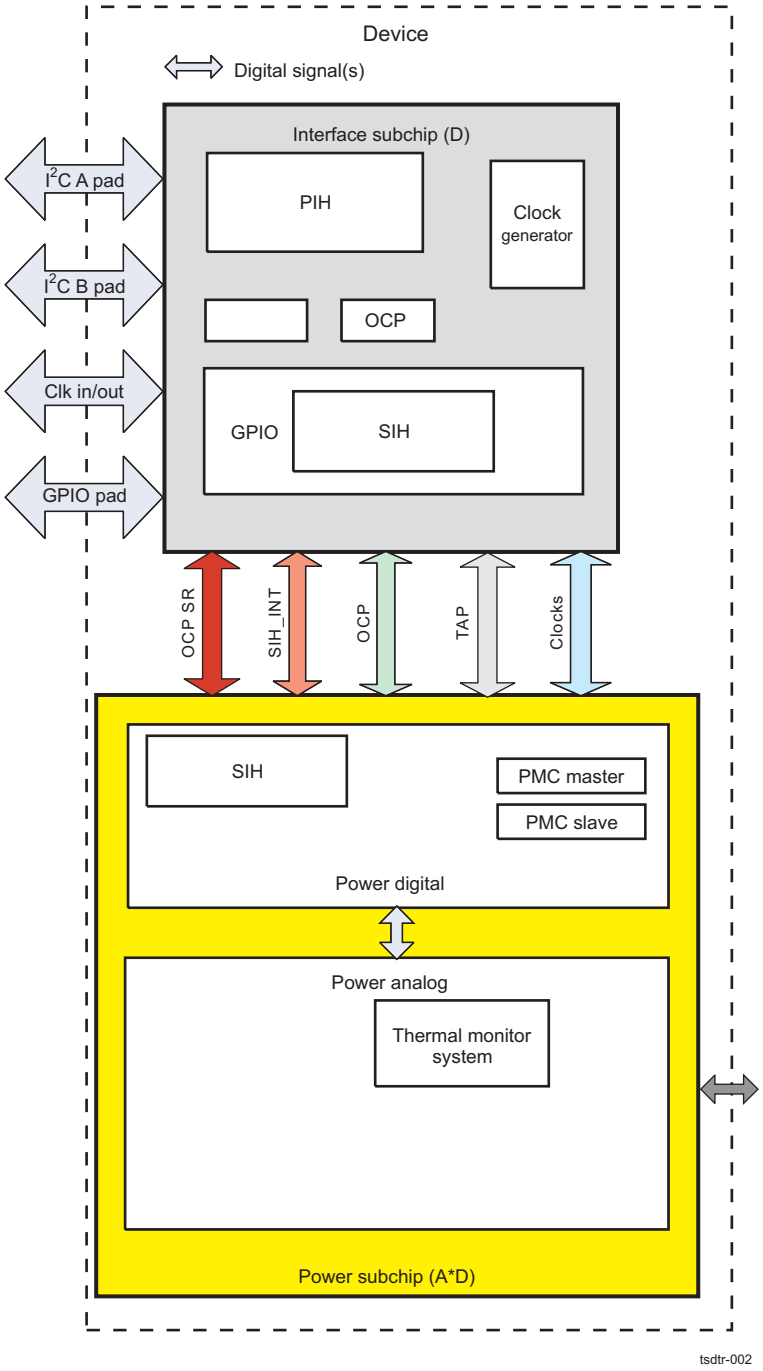
Table 12-3. Hot-Die Detector Examined for OFF-to-ACTIV State Transition

Bit	Bit Name	Register	Action
1	SEQ_MSK_THERM_HD	CFG_P123_TRANSITION	0: Used to check for valid OFF-to-ACTIVE transition
			1: Not used to check for valid OFF-to-ACTIVE transition

12.3 Thermal Shutdown and Hot-Die Detector Integration

Figure 12-2 is a simplified view of the device thermal monitoring system (thermal shutdown and hot-die detector) as it relates to the rest of the device.

Figure 12-2. Device Thermal Monitoring System



12.3.1 Thermal Shutdown Backup Mode

If the device gets too hot, the thermal shutdown mechanism protects it from damage caused by overheating by forcing it into wait-on mode. Thermal shutdown is available only in master mode.

12.3.2 Hot-Die Detector Interrupt

The hot-die detector function can generate an interrupt. For more information, see Section 12.2.2, *Hot-Die Detector External Interface*.

12.4 Thermal Shutdown and Hot-Die Detector Functional Description

12.4.1 Thermal Shutdown

When the device is in master mode, the thermal shutdown feature is available. If the junctions of the device reach a temperature at which damage can occur, all regulators are normally disabled and thermal shutdown information is written to a status register (the STS_BOOT[6] bit). All internal registers are reset, except the registers in the backup domain. For more information, see Chapter 5, *Resets and Power Management*. Thermal shutdown is not available in slave mode.

Operation of the thermal shutdown mechanism occurs when junction temperature increases past the rising-edge threshold temperature (a fixed temperature). As long as the device junction temperature remains higher than the hot-die falling-edge threshold (not the thermal shutdown falling-edge threshold; this avoids the possibility of oscillation), the device cannot be restarted.

See Table 12-4 for the thermal shutdown rising-edge and falling-edge temperature thresholds.

Table 12-4. Thermal Shutdown Thresholds

THERM Shutdown	Threshold (nominal)
Enable	Rising temperature: 150°C
	Falling temperature: 140°C

When the junction temperature falls below the hot-die falling-edge threshold, the device can be restarted. Restart from a thermal shutdown event can be manual (default) or automatic, as shown in Table 12-5.

Table 12-5. Restart from Thermal Shutdown

Bit	Bit Name	Register	Action
7	MSK_THERMAL_SHUTDOWN	CFG_P123_TRANSITION	0: Active
			1: Inactive

12.4.2 Hot-Die Detector

The hot-die detector monitors the junction temperature of the device, but does not shut it down. It provides an early warning to the host processor to reduce power dissipation and thus prevent a thermal shutdown. The highest hot-die threshold is 10°C below the thermal shutdown activation point; therefore, the host processor can note the rise in temperature and reduce the current drawn from the device before the thermal shutdown protective circuit activates.

If the device junction temperature reaches the hot-die detector junction temperature thresholds, an interrupt is sent, and this information is in the interrupt register. The application processor should then reduce the amount of power drawn from the device. If no corrective action is taken and the die temperature continues to rise, the thermal shutdown mechanism triggers a system reset to protect the device. The hot-die detector is always enabled (except in backup and wait-on modes), but an interrupt mask bit is available for it.

Three rising/falling pairs of temperatures can be set by configuring the MISC_CFG[7:6] TEMP_SEL bit field. When a emperature pair is selected, an interrupt is generated when the device junction temperature exceeds the rising temperature threshold or falls below the falling temperature threshold (see Table 12-6).

Table 12-6. Hot-Die Thresholds

Register MSC CFG	
TEMP_SEL[7:6]	**Threshold (nominal)**
00	Rising temperature: 120°C
First hot-die threshold	Falling temperature: 111°C

Table 12-6. Hot-Die Thresholds (continued)

Register MSC CFG	
01	Rising temperature: 130°C
Second hot-die threshold	Falling temperature: 121°C
10	Rising temperature: 140°C
Third hot-die threshold	Falling temperature: 131°C

NOTE: The value TEMP_SEL[7:6] = 11 is not used.

This flexibility allows two ways for the host processor to monitor the device junction temperature:

- Select a single temperature pair.
- Dynamically select temperature pairs as the device heats and cools.

Single temperature pair selection allows for conservative (low temperature settings) or aggressive (high temperature settings) operation of the device. Conservative operation dictates reducing current consumption well before junction temperature approaches thermal shutdown. Aggressive selection allows the device to function at higher temperatures and, therefore, nearer thermal shutdown.

Dynamically selecting the temperature pairs allows for monitoring of the device as its junction temperature changes over a 30°C range. The degree of sophistication in the software to use this capability is beyond the scope of this chapter.

Figure 12-3 shows the functioning of the thermal shutdown and hot-die detector mechanisms.

Figure 12-3. Thermal Shutdown and Hot-Die Temperature Operating Regions

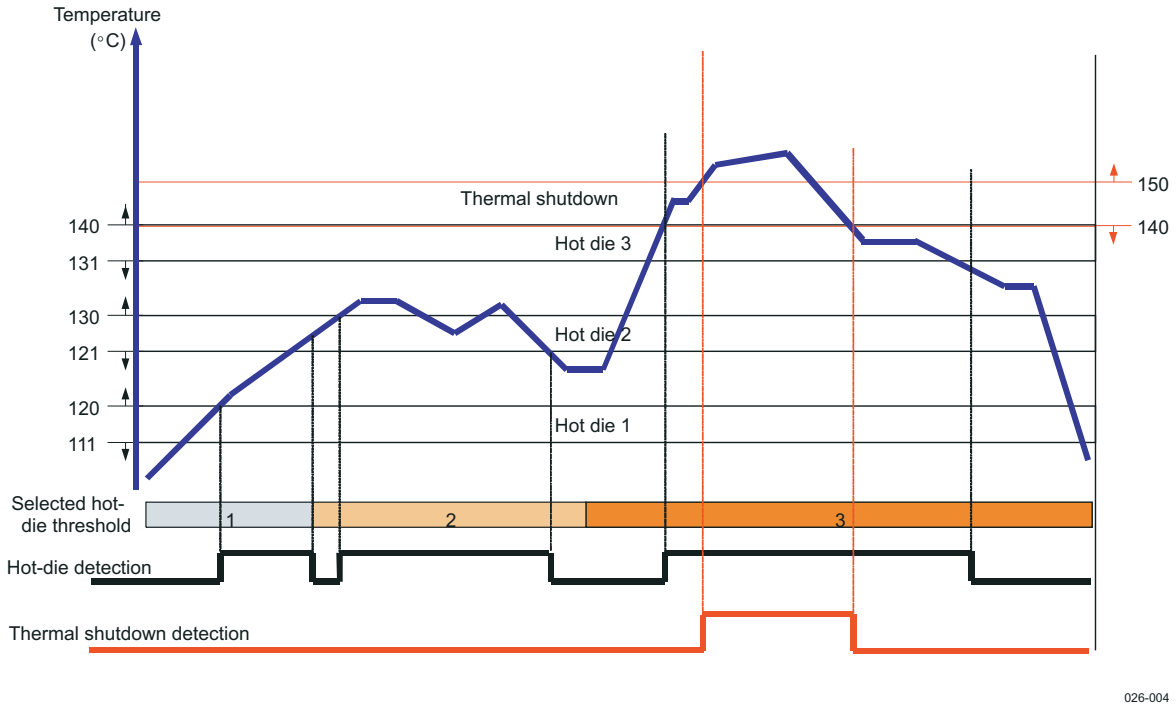


Table 12-7 describes the temperature ranges shown in Figure 12-3.

Table 12-7. Temperature Ranges of Thermal Shutdown and Hot-Die Operation

Thermal shutdown	Rising temperature: 150°C
	Falling temperature: 140°C
Hot-die 3	Rising temperature: 140°C
	Falling temperature: 131°C

Table 12-7. Temperature Ranges of Thermal Shutdown and Hot-Die Operation (continued)

Hot-die 2	Rising temperature: 130°C
	Falling temperature: 121°C
Hot-die 1	Rising temperature: 120°C
	Falling temperature: 111°C

12.5 Thermal Shutdown and Hot-Die Detector Programming Model

For the device thermal shutdown and hot-die detector mechanisms, a programming model is not useful, because internal to the device, the only programming possible is setting the register bits associated with the operation of the circuitry.

The actual programming of the thermal shutdown and hot-die detector features is in the device is in the host processor.

To configure the hot-die detector, perform the following steps:

1. Configure the hot-die detector for operation in its lowest temperature range (111 to 120°C):
   Set the MISC_CFGTEMP_SEL[7:6] bit field to [0:0].
2. Configure the hot-die detector so that it generates an interrupt on interrupt status line 1:
   Set the PWR_ISR1[4] HOT_DIE bit to 1.
3. Ensure that the interrupt is not masked:
   Confirm that the PWR_IMR1[4] HOT_DIE bit is set to 1.
4. Ensure that the hot-die detector rising threshold and the hot-die detector falling threshold are active (enabled):
   Confirm that the PWR_EDR2[1] HOT_DIE_RISING1 and PWR_EDR2[0] HOT_DIE_FALLING bits are set to 1.

12.6 Thermal Shutdown and Hot-Die Detector Register Manual

The following pages list the device registers related to thermal shutdown and hot-die detector operation.

In some of the registers, the thermal shutdown and hot-die related features are dispersed among other functions. In the following tables, they are highlighted to make them easily recognizable.

NOTE: Any appearance of Triton or Triton 2 is a direct reference to the device and indicates that the original source material is from TI's product-development organization.

12.6.1 Register Access

The device internal registers are accessed through its I^2C buses.

All hot-die and thermal shutdown-related registers are in the 4b(hex) register address group. For more information, see Chapter 2, *Control Interface*.

Table 12-8. PWR_ISR1

Address Offset	0x00		
Physical Address	0x0000 002E	**Instance**	POWERINT
Description	This interrupt status register ISR1 determines which input event triggered the interrupt line int1_n request (VRRTC domain).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	RESERVED	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset off
7	SC_DETECT		RW	0
6	MBCHG		RW	0
5	RESERVED		RW	0
4	HOT_DIE		RW	0
3	RTC_IT		RW	0
2	USB_PRES		RW	0
1	CHG_PRES		RW	0
0	PWRON	Because the PWRON signal is active low, this signal is used inverted.	RW	0

Table 12-9. PWR_IMR1

Address Offset	0x01		
Physical Address	0x0000 002F	**Instance**	POWERINT
Description	This interrupt mask register IMR1 allows masking an event to keep it from generating an interrupt request on _int1_n (VRRTC domain).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	RESERVED	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset off
7	SC_DETECT		RW	1
6	MBCHG		RW	1
5	RESERVED		RW	1

Bits	Field Name	Description	Type	Reset off
4	HOT_DIE		RW	1
3	RTC_IT		RW	1
2	USB_PRES		RW	1
1	CHG_PRES		RW	1
0	PWRON		RW	1

Table 12-10. PWR_ISR2

Address Offset	0x02		
Physical Address	0x0000 0030	**Instance**	POWERINT
Description	This interrupt status register ISR2 determines which input event triggered the interrupt line int2_n request (VRRTC domain).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	RESERVED	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset off
7	SC_DETECT		RW	0
6	MBCHG		RW	0
5	RESERVED		RW	0
4	HOT_DIE		RW	0
3	RTC_IT		RW	0
2	USB_PRES		RW	0
1	CHG_PRES		RW	0
0	PWRON	Because the PWRON signal is active low, this signal is used inverted	RW	0

Table 12-11. PWR_IMR2

Address Offset	0x03		
Physical Address	0x0000 0031	**Instance**	POWERINT
Description	This interrupt mask register IMR2 allows masking an event to keep it from generating an interrupt request on _int1_n (VRRTC domain).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	RESERVED	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset off
7	SC_DETECT		RW	1
6	MBCHG		RW	1
5	RESERVED		RW	1
4	HOT_DIE		RW	1
3	RTC_IT		RW	1
2	USB_PRES		RW	1
1	CHG_PRES		RW	1
0	PWRON		RW	1

Table 12-12. PWR_SIR

Address Offset	0x04		
Physical Address	0x0000 0032	**Instance**	POWERINT
Description	For testing, this software interrupt register PWR_SIR allows generating an interrupt event on the int1_n or int2_n request line by writing 1 to the targeted SIR bit in a specific test mode (VRRTC domain). This register is protected by the Triton2 global test key (write B6 at address 97 in the interfaces to unlock this key).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	RESERVED	HOT_DIE	RTC_IT	USB_PRES	CHG_PRES	PWRON

Bits	Field Name	Description	Type	Reset off
7	SC_DETECT		RW	0
6	MBCHG		RW	0
5	RESERVED		RW	0
4	HOT_DIE		RW	0
3	RTC_IT		RW	0
2	USB_PRES		RW	0
1	CHG_PRES		RW	0
0	PWRON		RW	0

Table 12-13. PWR_EDR2

Address Offset	0x06		
Physical Address	0x0000 0034	**Instance**	POWERINT
Description	Power edge detection register 2 short circuit detect, main battery charger, power ok, and hot-die presences (VRRTC domain)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SC_DETECT_RISING	SC_DETECT_FALLING	MBCHG_RISING	MBCHG_FALLING	RESERVED	RESERVED	HOT_DIE_RISING	HOT_DIE_FALLING

Bits	Field Name	Description	Type	Reset off
7	SC_DETECT_RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	0
6	SC_DETECT_FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled	RW	0
5	MBCHG_RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	0
4	MBCHG_FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled	RW	0

Bits	Field Name	Description	Type	Reset off
3	RESERVED		RW	0
2	RESERVED		RW	0
1	HOT_DIE_RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	0
0	HOT_DIE_FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled	RW	0

Table 12-14. MISC_CFG

Address Offset	0x0D–0x0D in 0x17 byte increments		
Physical Address	0x0000 0068–0x0000 0068	**Instance**	POWERPM_RECEIVER
Description	VRRTC domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
TEMP_SEL		VINTANA2_SWITCH_AUTO	CLK_HF_DRV	RFID_EN_PU_DISABLE	RFID_EN	CLKEN2_CFG	CLKEN2_ENABLE

Bits	Field Name	Description	Type	Reset off
7:6	TEMP_SEL	Hot-die interrupt temperature selection	RW	0x0
5	VINTANA2_ SWITCH_AUTO	0: Switch from 2V75 to 2V5 if battery voltage is below 3V0 manual. 1: Automatic switch enabled	RW	0
4	CLK_HF_DRV	Drive capability of the pad 0: 10 pF 1: 40 pF Default value for PG 1.0 was 0.	RW	1
3	RFID_EN_PU_ DISABLE	0: RFID_EN pullup enabled when the open drain is not driven. 1: RFID_EN pullup never enabled (Was CLK_32K_DRV; not used.)	RW	0
2	RFID_EN	0: RFID_EN pad is set to 0. 1: RFID_EN pad is set to 1.	RW	0
1	CLKEN2_CFG	0: The CLKEN clock enable is output on CLKEN2. 1: CLKEN2 pad is a GPIO.	RW	1
0	CLKEN2_ENABLE	If CLK2_CFG = 1: 0: CLK2 = 0 1: CLK2 = 1 If CLKEN2_CFG = 0: No action	RW	0

Table 12-15. CFG_P123_TRANSITION

Address Offset	0x03–0x03 in 0xE byte increments		
Physical Address	0x0000 0039–0x0000 0039	**Instance**	POWERPM_MASTER
Description	Configuration register for transition processors 1, 2, and 3 (backup domain). Write-protected with the KEY_CFG.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
MSK_THERMAL_SHUTDOWN	MSK_MBLO	SEQ_MSK_BAT_PRESENCE	SEQ_MSK_BAT_LEVEL	SEQ_MSK_THERM_HD	SEQ_FREEZE	SEQ_ONSYNC	SEQ_OFFSYNC

Bits	Field Name	Description	Type	Reset off
7	MSK_THERMAL_SHUTDOWN	When 0: PMC is reset when TS = 1. When 1: PMC is not reset when TS = 1.	RW	1
6	MSK_MBLO	When 0: PMC is reset when MBLO = 1. When 1: PMC is not reset when MBLO = 1.	RW	0
5	SEQ_MSK_BAT_PRESENCE	When 0: VBAT voltage comparator checks a valid OFF to ACTIVE transition. When 1: VBAT presence comparator does not check a valid OFF to ACTIVE transition; the comparator status is seen as equal to 1.	RW	1
4	SEQ_MSK_BAT_LEVEL	When 0: VBAT voltage comparator checks a valid OFF to ACTIVE transition. When 1: Vbat voltage comparator does not check a valid OFF to ACTIVE transition; the comparator status is seen as equal to 1.	RW	0
3	SEQ_MSK_THERM_HD	When 0: Thermal shutdown hot-die checks a valid OFF to ACTIVE transition. When 1: Thermal shutdown hot-die does not check a valid OFF to ACTIVE transition.	RW	1
2	SEQ_FREEZE	0: Sequencers can initiate a new transition. 1: Freeze all sequencers in their current state; all sequencers finish their current transition if one is ongoing.	RW	0
1	SEQ_ONSYNC	0: Sequencers do not wait for each other before any P[123]_OFF2ACT transition. This register can switch on part of the design by software rather than with a hardware condition. 1: Sequencers wait for each other before any P[123]_OFF2ACT transition. Any switch-on on one sequencer is applied to all sequencers. (Has priority on switch-on mask condition)	RW	1
0	SEQ_OFFSYNC	0: Sequencers do not wait for each other before any P[123]_ACT2WAITON transition. This register can switch on part of the design by software rather than with a hardware condition. 1: Sequencers wait for each other before any P[123]_ACT2WAITON transition.	RW	1

Bits	Field Name	Description	Type	Reset off
		Any write in P[123]_DEVOFF also writes the value in P[123]_DEVOFF.		

Table 12-16. STS_BOOT

Address Offset	0x04–0x04 in 0xE byte increments		
Physical Address	0x0000 003A–0x0000 003A	**Instance**	POWERPM_MASTER
Description	Backup domain		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
BACKUP	TS	WATCHDOG_RESET	ITCHECK_RESET	PWRON_8S	SETUP_DONE_BCK	SETUP_DONE_PMC	SYSEN_RESET

Bits	Field Name	Description	Type	Reset off
7	BACKUP	0: Triton2 did not enter backup mode since last register clear. 1: Triton2 entered backup mode since last register clear.	RW	0
6	TS	0: No thermal shutdown occurred since last register clear. 1: A thermal shutdown occurred since last register clear.	RW	0
5	WATCHDOG_RESET	1 : Reset caused by a warmreset occurred since last register clear. 0 : No reset caused by a warmreset occurred since last register clear	RW	0
4	ITCHECK_RESET	1 : Reset caused by an IT_Check occurred since last register clear. 0 : No reset caused by an IT_Check occurred since last register clear.	RW	0
3	PWRON_8S	1 : Restart caused by a PWRON low of more than 8s occurred since last register clear. 0 : No restart caused by a PWRON low of more than 8s occurred since last register clear.	RW	0
2	SETUP_DONE_BCK	Can indicate that the backup configuration is done (RTC, BACKUP registers, etc.). This bit is automatically reset to 0 when the backup configuration is lost. This bit can be set to 1 by the user when the PMC is configured.	RW	0
1	SETUP_DONE_PMC	Can determine that the PMC is configured. This bit is automatically reset to 0 when the PMC configuration is lost. This bit can be set to 1 by the user when the PMC is configured.	RW	0
0	SYSEN_RESET	0: SYSEN was not driven low by an external device since last register clear. 1: SYSEN was driven low by an external device since last register clear.	RW	0

Table 12-17. UNLOCK_TEST_REG

Address Offset	0x12		
Physical Address	0x0000 0097	**Instance**	INT_SCINTBR
Description	Writing 01001001 to this register allows unlocking of T2 EEPROM SW READ access through OCP.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
TEST_RESERVED_8	TEST_RESERVED_7	TEST_RESERVED_6	TEST_RESERVED_5	TEST_RESERVED_4	TEST_RESERVED_3	TEST_RESERVED_2	TEST_RESERVED_1

Bits	Field Name	Description	Type	Reset off
7	TEST_RESERVED_8	Reserved for test register access	RW	0
6	TEST_RESERVED_7	Reserved for test register access	RW	0
5	TEST_RESERVED_6	Reserved for test register access	RW	0
4	TEST_RESERVED_5	Reserved for test register access	RW	0
3	TEST_RESERVED_4	Reserved for test register access	RW	0
2	TEST_RESERVED_3	Reserved for test register access	RW	0
1	TEST_RESERVED_2	Reserved for test registers access	RW	0
0	TEST_RESERVED_1	Reserved for test register access 0x0: (Default) GPIO13 function is enabled. 0x1: LEDSYNC function is enabled.	RW	0

Audio

This chapter describes the audio subsystem for the TPS65930 integrated power-management/audio coder/decoder (codec) device. The TPS65920 has no audio functionality.

Topic **Page**

13.1 Overview

The device audio module contains several audio analog inputs and outputs. It is connected to a multimedia processor through the time-division multiplexing (TDM)/codec interface (audio interface). The audio module is controlled by internal registers that can be accessed by the high-speed (HS) inter-integrated circuit (I^2C™) control interface.

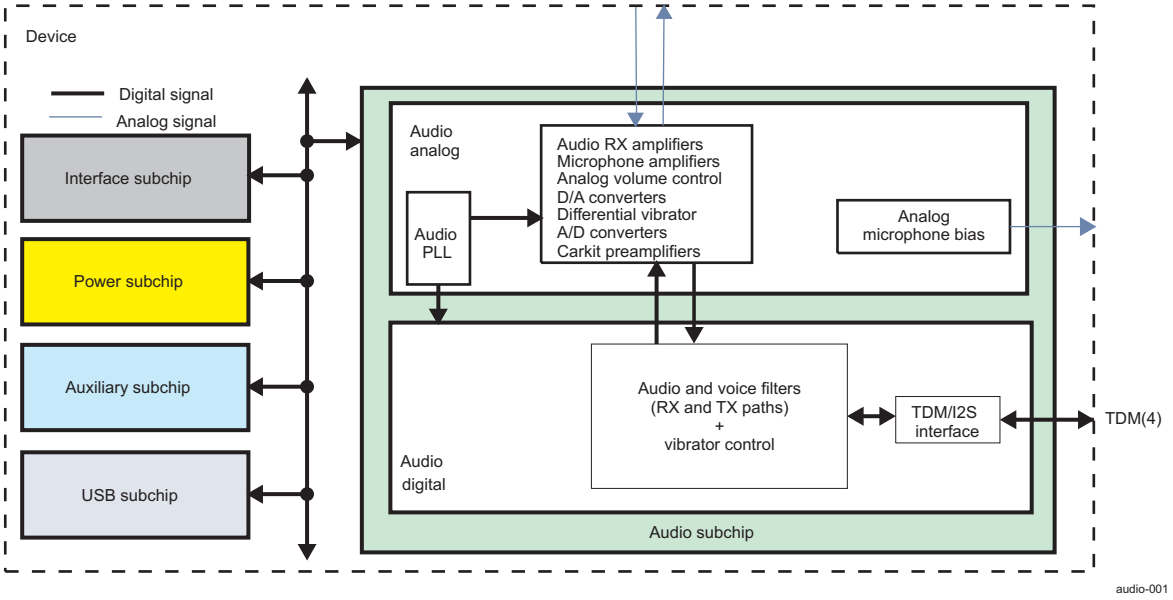
13.1.1 Feature List Overview

- Serial data ports:
  - One port: Port 2 is an audio inter-IC sound (I2S™)/TDM interface. (Port 1 is unavailable.)
  - No support for McBSP dynamic slot
  - In TDM mode, port 2 can act only as a master.
  - Tristate capability in I2S/TDM
- Audio channels:
  - Audio channel with 8-, 11.025-, 12-, 16-, 22.05-, 24-, 32-, 44.1-, or 48-kHz sampling modes, 96 kHz is supported on the RX path voice codec on MCLK = 26-MHz clock
  - Audio phase-locked loop (PLL) supports 26-, 19.2-, or 38.4-MHz ability to work with two ports with the clock frequencies 19.2 or 26 MHz, or with a single TDM port with the frequencies 19.2, 26, or 38.4 MHz.
  - Carkit, analog loop mode
  - One analog microphone bias
- Power and analog mixing
  - Analog/digital mixing capability (path-mixing capability)
  - Three lines for the uplink path (one differential input). FM input is mono.
  - Predrivers for external class D or piezoelectric speaker drivers
- Additional features
  - Pop-noise reduction circuitry for all paths
  - Data scramble function for I2S data received
  - Bass boost functions in one stereo audio RX path
  - Automatic gain control on the microphone paths
  - Independent gains on UL paths
  - Programmable gain amplifier on audio RX and TX
  - Wide gain programmable range on the microphone input
  - Dual-tone modulation frequency (DTMF) tone generator

13.1.2 Audio Block Diagram

Figure 13-1 is the audio block diagram.

Figure 13-1. Device Audio Subsystem Overview



13.2 Environment

This section describes the audio module from an environmental point of view (external connections). The audio module has three bidirectional digital interfaces. It has six paths for analog-to-digital conversion and five paths for digital-to-analog conversion.

13.2.1 Digital Interfaces

13.2.1.1 TDM codec Interface

Table 13-1 lists the TDM/codec interface pins.

Table 13-1. TDM/codec Interface

TDM/I2S Pin	I/O (1)	Description
tdm/codec.din	I	Audio data port (TDM/codec): Receive data
tdm/codec.dout	O/Z	Audio data port (TDM/codec): Transmit data
tdm/codec.sync	I/O/Z	Audio data port (TDM/codec): Frame synchronization
tdm/codec_clk	I/O/Z	Audio data port (TDM/codec): Clock
clk256fs	O	256 * Fs clock output or 128 * Fs (Fs = 96 kHz)

(1) I = Input, O = Output, Z = High-impedance state; no input or output

The multimedia audio path plays and records multichannel serial data. The digital interface supports a TDM protocol and can exchange data on four independent channels. It can also be configured to exchange stereo data using the I2S protocol. The following frequencies are supported:

- 8 kHz
- 11.025 kHz
- 12 kHz
- 16 kHz
- 22.05 kHz
- 24 kHz
- 32 kHz
- 44.1 kHz
- 48 kHz

The sampling rate of 96 kHz is also supported only with receive audio data from the host processor (the audio transmit path is not available in this case).

The device acts as a master or slave for the audio interface (except in TDM mode, where the device acts as a master only). If the device is master (the AUDIO_IF[7] AIF_SLAVE_EN bit is cleared to 0), it must provide the frame synchronization (TDM/I2S_SYNC) and bit clock (TDM/I2S_CLK) to the host processor. If the device is slave (the AUDIO_IF[7] AIF_SLAVE_EN bit is set to 1), it receives frame synchronization and the bit clock. In slave mode, the device provides 256*Fs (except in the 96-kHz sampling mode, where the device provides 128*Fs).

Data formats supported by the device are I2S, left-justified, right-justified, and TDM. TDM/I2S timing signals are generated from the external HFCLKIN clock. The supported HFCLKIN clock frequencies are 19.2, 26, and 38.4 MHz. A PLL in the device audio block generates the appropriate frequencies from HFCLKIN. The TDM/I2S interface can be placed in a high-impedance (HiZ) state under register control.

13.2.2 Analog Interfaces

13.2.2.1 Bias For Microphones

A bias generator provides external voltage to the analog microphone.

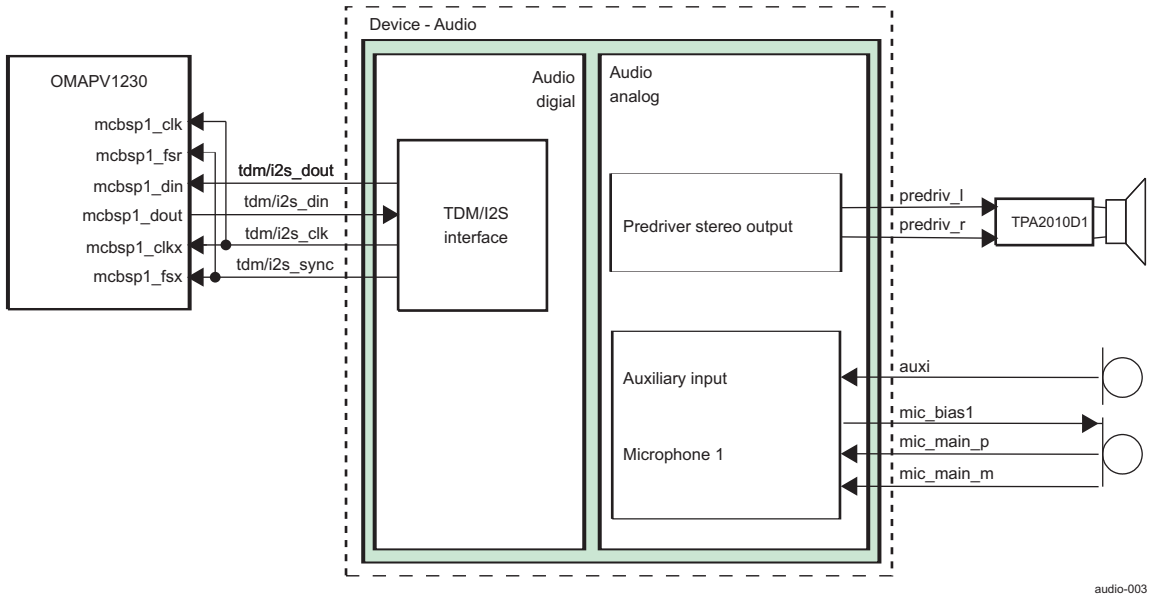
13.2.2.2 FM Radio/Auxiliary Input

The auxiliary input auxr/fmr can be used as an FM radio monaural input. In this case, because the input amplifier is busy, other input terminals are discarded and set to a high-impedance state. The microphone amplification stage (Ampli_R) amplifies the FM radio signal. the amplification stage output is connected to the analog-to-digital converter (ADC) input.

13.2.2.3 Audio Module External Connections

Figure 13-2 shows an example of the external connections of the audio module to an OMAPV1230 modem and application processor.

Figure 13-2. External Connections of the Audio Module to OMAPV1230 Application Processor



13.3 Integration

The audio subsystem interacts with the following device domains:

- The interface subchip: Access to the audio registers is from this interface.
- The power subchip: Table 13-2 details the power domains.
- The main clock input (HFCLKIN: 19.2, 26, or 38.4 MHz). The clocks for multimedia audio processing are generated by a PLL, the voice processing is usable when the input clock is 26 MHz, and the final sampling frequency (8 or 16 kHz) is obtained with an integer division of HFCLKIN. If the system master clock is not 26 MHz, the voice PCM interface is unavailable.

Table 13-2. Power Domains

Audio Pin	Supply Domain	Description
vbat		Direct connection to the main battery
vssa		Negative power supply
vdd_io		I/O port power supply: 1.8 V
vintana1		Analog 1.5-V power supply
vintana2		Analog 2.75-V power supply
clk256fs	vdd_io	256 Fs clock output or 128 Fs (Fs = 96 kHz)
clk64k.out	vdd_io	64-kHz clock output
tdm/codec_din	vdd_io	Audio data port (TDM/codec): Receive data
tdm/codec_dout	vdd_io	Audio data port (TDM/codec): Transmit data
tdm/codec_sync	vdd_io	Audio data port (TDM/codec): Frame synchronization
tdm/codec_clk	vdd_io	Audio data port (TDM/codec): Clock
gpio06 (mute)	vdd_io	Mute control for external FET
vref	vintana1	Band gap external filtering (external capacitor)
micbias1	vintana2	Analog microphone 1 bias supply
mic_main_m	vintana2	Main microphone (−)
mic_main_p	vintana2	Main microphone (+)
auxr	vintana2	Auxiliary input right
predriv_left	vintana2	Predriver for external class D, left amplifier output
predriv_right	vintana2	Predriver for external class D, right amplifier output

13.3.1 Audio Voice Registers

This section provides information about the audio voice module. The registers are described in Table 13-3.

Table 13-3. Register Summary

Register Name	Description
CODEC_MODE	System mode control register
	Audio PLL setup, voice frequency sampling, data path options, on/off
OPTION	Audio/voice digital filter power control
MICBIAS_CTL	Microphone bias and analog microphone amplifier power control register
ANAMICL	Analog microphone offset cancellation and routing to the ADC
ANAMICR	Analog microphone right control register
AVADC_CTL	Audio/voice ADC control register
ADCMICSEL	Digital audio/voice TX filter input select
DIGMIXING	Voice/audio digital mixing control register
ATXL1PGA	Audio TXL1 gain control register
ATXR1PGA	Audio TXR1 gain control register
AVTXL2PGA	Audio/voice TXL2 gain control register
AVTXR2PGA	Audio/voice TXR2 gain control register

Table 13-3. Register Summary (continued)

Register Name	Description
AUDIO_IF	Control mode for audio interface (master/slave, 16 or 32 bits, codec/TDM, 256Fs, high impedance)
VOICE_IF	Control mode for voice interface (master/slave, 16 or 32 bits, clock edges, I/O swap, high impedance)
ARXR1PGA	Audio RXR1 gain control register
ARXL1PGA	Audio RXL1 gain control register
ARXR2PGA	Audio RXR2 gain control register
ARXL2PGA	Audio RXL2 gain control register
AVDAC_CTL	Power control register for audio DAC
ARX2VTXPGA	Audio RX to voice TX PGA gain control
ARXL1_APGA_CTL	Audio RXL1 analog PGA control register (gains, FM loop path, digital path enable)
ARXR1_APGA_CTL	Audio RXR1 analog PGA control register (gains, FM loop path, digital path enable)
ARXL2_APGA_CTL	Audio RXL2 analog PGA control register (gains, FM loop path, digital path enable)
ARXR2_APGA_CTL	Audio RXR2 analog PGA control register (gains, FM loop path, digital path enable)
PREDL_CTL	Predriver class D left amplifier control register
PREDR_CTL	Predriver class D right amplifier control register
PRECKL_CTL	Preamplifier carkit left control register
PRECKR_CTL	Preamplifier carkit right control register
ALC_CTL	ALC control (microphone selection, release time)
ALC_SET1	ALC high and low threshold control
ALC_SET2	ALC release/attack time control
BOOST_CTL	Compensation of output capacitor high-pass effect
SOFTVOL_CTL	Soft volume control register
DTMF_FREQSEL	Tone frequency control
DTMF_TONEXT1H	Setting tone 1 (high frequency)
DTMF_TONEXT1L	Setting tone 1 (low frequency)
DTMF_TONEXT2H	Setting tone 2 (high frequency)
DTMF_TONEXT2L	Setting tone 2 (low frequency)
DTMF_TONOFF	Setting time for tone on/off
DTMF_WANONOFF	Wobble on/off control
CODEC_RX_SCRAMBLE_H	CODEC_RX_SCRAMBLE_H
CODEC_RX_SCRAMBLE_M	CODEC_RX_SCRAMBLE_M
CODEC_RX_SCRAMBLE_L	CODEC_RX_SCRAMBLE_L
APLL_CTL	Audio PLL control register
DTMF_CTL	DTMF generator control
DTMF_PGA_CTL2	DTMF gain control register 2 (gains)
DTMF_PGA_CTL1	Tone gain control register 1 (fine gains)
MISC_SET_1	Miscellaneous 1 (CLK64, scrambling, FM loop, digital microphone swap)
PCMBTMUX	PCM/BT multiplexer and tone adder control register
RX_PATH_SEL	RX path select control register
VDL_APGA_CTL	Voice downlink analog PGA control register
ANAMIC_GAIN	Gain control of the microphone amplifier
MISC_SET_2	Miscellaneous 2 (high-pass, bypass)

13.4 Functional Description

The audio functions are described by splitting the audio submodule into three parts:

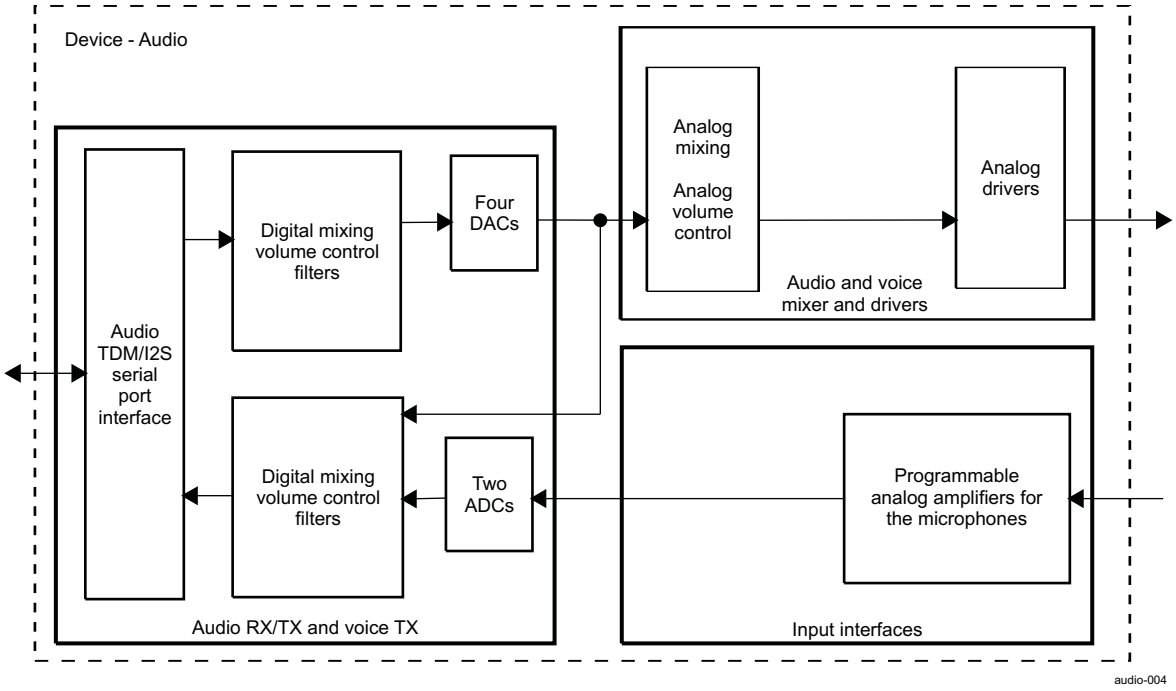
- The audio and voice mixers and drivers with analog gain, mixing, and power amplification

- The audio RX/TX paths, which include the digital uplink paths and the audio converters (There are up to two stereo TX paths: audio TXL1/audio TXR1 and audio TXL2/audio TXR2. There are up to two stereo RX paths: audio RXL1/audio RXR1 and audio RXL2/audio RXR2.)
- The analog input connected to the analog auxiliary input and the microphones

NOTE: The modem or the OMAP™ device and audio interfaces must use the same clock provider as the device.

Figure 13-3 is an architecture overview of the audio subsystem. For a detailed block diagram, see Figure 13-4.

Figure 13-3. Device Audio Subsystem Architectural Overview



13.4.1 Data Paths

After the audio submodule is powered up (by the CODEC_MODE[1] CODECPDZ bit, see Table 13-7), its mode of operation is option 1: four simultaneous multimedia analog channels (four multimedia DACs and no modem voice path) and two simultaneous ADCs. Option 1 is configurable through the CODEC_MODE[0] OPT_MODE bit.

Table 13-4 lists operations for option 1.

Table 13-4. Voice and Audio Option Selection

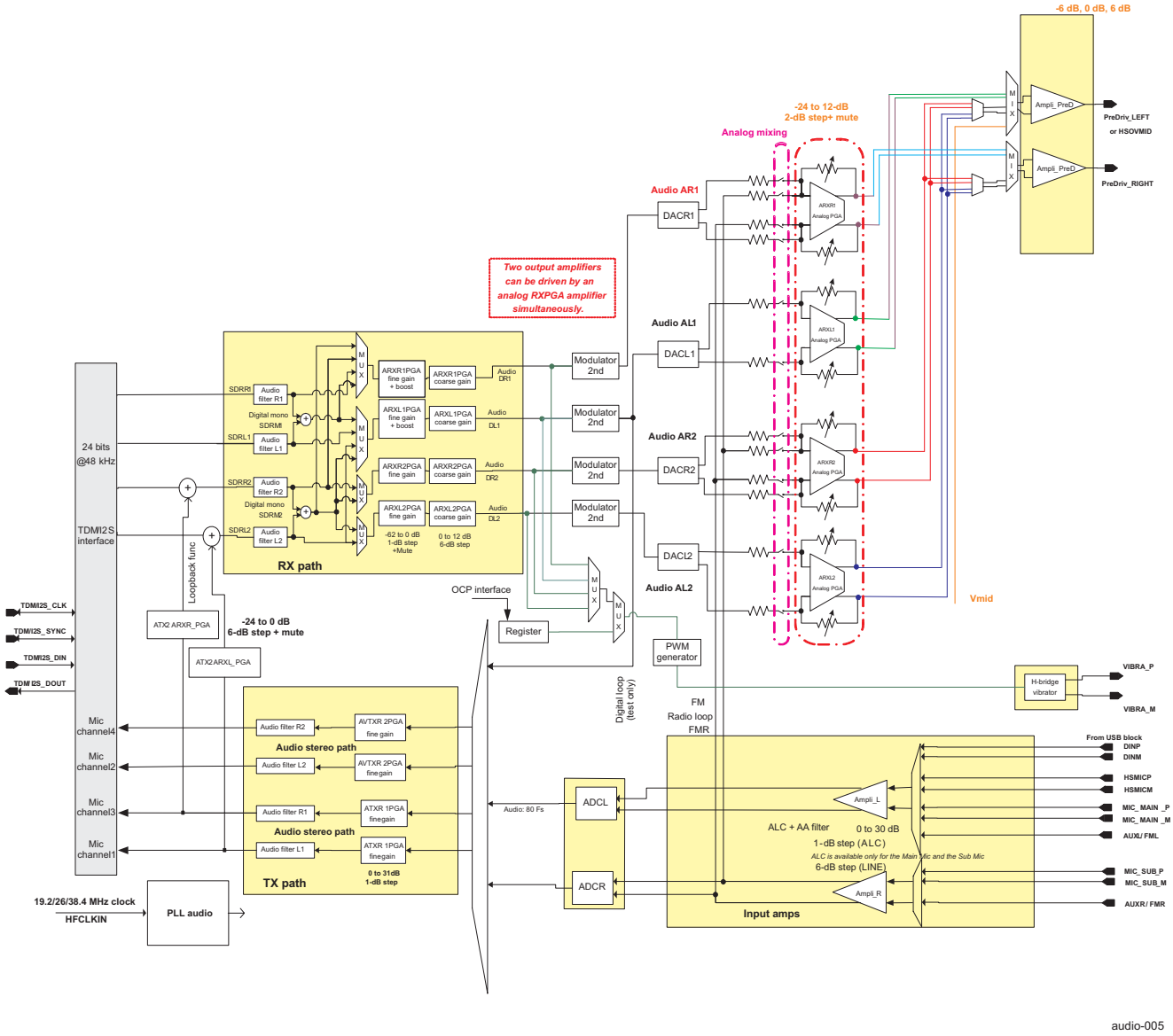
	TX Audio Path 1 (Left and Right)	TX Audio Path 2 (Left and Right)	Audio Filter 1 (Left and Right)	Audio Filter 2 (Left and Right)
Option 1	X(1)	X	X	X

(1) X indicates paths that can be used simultaneously.

13.4.1.1 Audio Option 1 Block Diagram

Figure 13-4 is the block diagram for audio option 1 (OPT_MODE = 1).

Figure 13-4. Audio Option 1 (OPT_MODE = 1) Block Diagram



13.4.2 Configuration of the Paths

13.4.2.1 Audio RX/TX and Voice TX Channel Configuration

Stereo Audio Path

The two stereo audio paths receive left and right signal samples at the rate of a programmable frequency, from 8 to 96 kHz:

- 8 kHz
- 11.025 kHz
- 12 kHz
- 22.05 kHz
- 24 kHz

- 32 kHz
- 44.1 kHz
- 48 kHz
- 96 kHz

The paths receive the signal samples through the TDM/codec configurable serial interface and convert them to analog signals to drive the external audio signal or speech transducers. This is accomplished by programming the CODEC_MODE[7:4] APLL_RATE bit field.

The digital audio signal is first fed to an audio digital filter that has two functions:

- Interpolates the input signal and increases the sampling rate to allow digital-to-analog conversion to be performed by an oversampling digital modulator
- Band-limits the audio signal with a low-pass transfer function

The interpolated and band-limited signal is fed to a second-order σ–Δ digital modulator to generate an oversampled signal. This signal is passed through a dynamic element matching block and then to a DAC.

Volume control is performed in the analog domain and/or the digital domain. Analog volume control is performed in 2-dB steps from –24 to 12 dB (the ARXR1_APGA_CTL[7:3] ARXR1_GAIN_SET bit field, the ARXL2_APGA_CTL[7:3] ARXL2_GAIN_SET bit field, and the ARXR2_APGA_CTL[7:3] ARXR2_GAIN_SET bit field). In mute state, attenuation is higher than 40 dB. The gain is independently programmable on the left and right channels. Digital volume control is performed in 1_dB steps from –62 to 12 dB, left and right paths separately. Programming is performed by the ARXR1PGA[5:0] ARXR1PGA_FGAIN bit field and the ARXL1PGA[5:0] ARXL1PGA_FGAIN bit field. The gain setting of all paths is performed separately: right 1 by the ARXR1PGA register, left 1 by the ARXL1PGA register, right 2 by the ARXR2PGA register (see Table 13-23), and left 2 by the ARXL2PGA register (see Table 13-24).

Soft Volume

The audio volume control function controls transition time between two audio gain selections. This function allows definition of a smooth transition between signal levels.

The soft volume function is applied to the audio RX1 and RX2 paths.

Soft volume sweep time is the transition time from MUTE to MAX or MAX to MUTE. The sweep time is controlled by the SOFTVOL_SET bits of the SOFTVOL_CTL register between 0.8*Fs to 0.8*1024*Fs (see Table 13-52).

NOTE: When Fs = 96 kHz, the sweep time is twice (the same transition time when Fs = 96 kHz and Fs = 48 kHz).

Data Scramble

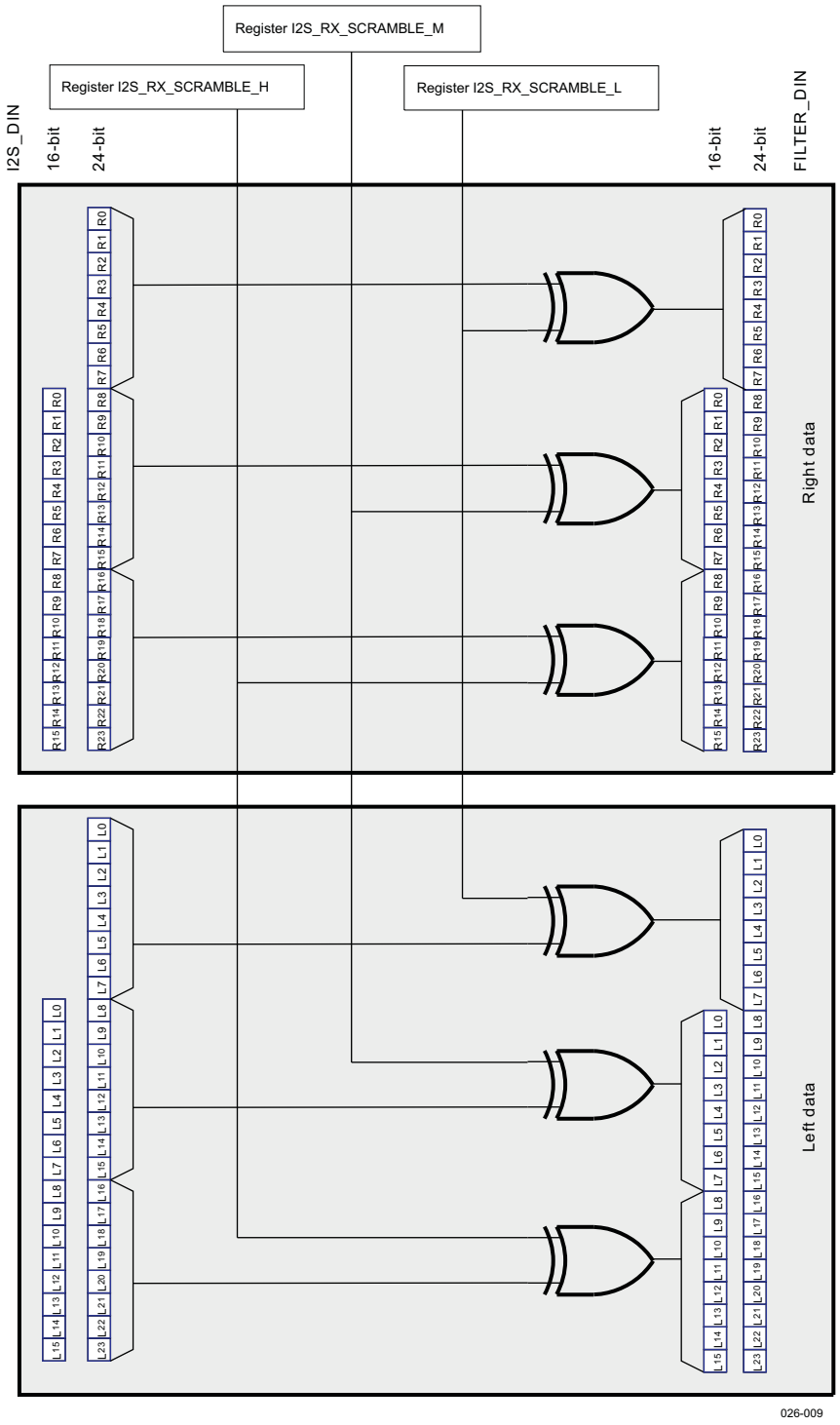
I2S data can be inverted or not inverted by a register control: 1 in the register controls means that the data is inverted and 0 means that the data is not inverted. The scramble circuit is equivalent to an XOR.

The CODEC_RX_SCRAMBLE_H register controls the most-significant bit (MSB) of the audio DAC input data for L and R. The CODEC_RX_SCRAMBLE_M and CODEC_RX_SCRAMBLE_L registers control the least-significant bit (LSB) of the audio DAC input data.

To enable scrambling, set the MISC_SET_1[6] SCRAMBLE_EN bit. The scrambling bits CODEC_RX_SCRAMBLE_L/M/H are in Table 13-62, Table 13-61, and Table 13-60, respectively.

Figure 13-5 is the data scramble diagram.

Figure 13-5. Data Scramble Diagram



13.4.2.2 Input Interfaces Configuration

Microphone Amplification Stage

These stages perform single-to-differential conversion for single-ended inputs. Two programmable gains from 0 to 30 dB can be set:

- Automatic level control for main microphone or submicrophone input.

- Level control by register for line-in or carkit input or headset microphone. The gain step is 6 dB (the MICAMPL_GAIN and MICAMPR_GAIN bits of the ANAMIC_GAIN register).

Amplification stage outputs are connected to the ADC input (ADC left and right).

13.4.2.3 Audio Mixer and Driver Configuration

This section describes the analog mixing and amplification of the audio path.

Predriver Output

These amplifiers provide a stereo signal on the terminals predrv_l and predrv_r to drive an external class D amplifier.

The following bits control this path:

- The PREDL_CTL[7] PREDL_OUTLOW_ EN bit enables amplification. Input selection from among the voice, audio left 1, audio left 2, and audio right 2 channels is performed with the PREDL_VOICE_EN, PREDL_AL1_EN, PREDL_AL2_EN, and PREDL_AR2_EN bits, respectively. The PREDL_GAIN bits control the gain.
- The PREDR_CTL[7] PREDR_OUTLOW_EN bit enables amplification. Input selection from among the voice, audio right 1, audio right 2, and audio left 2 channels is performed with the PREDR_VOICE_EN, PREDR_AR1_EN, PREDR_AR2_EN, and PREDL_AL2_EN bits, respectively. The PREDR_GAIN bits control the gain.

Analog Volume Control Pop-Noise Reduction

To reduce pop noise when the analog volume control changes, the MISC_SET_1[1] SMOOTH_ANAVOL_EN bit is enabled before and after performing the RX path offset cancellation described in *Earphone Pop-Noise Attenuation*.

Pop reduction is achieved by allowing analog gain change only when the analog PGA output signal crosses 0, or after a time-out of 25 ms.

Microphone Bias Module

A bias generator provides an external voltage of 2.2 V to bias the analog microphone (micbias1).

Mixing Capabilities on the Analog Path

The following list shows available signals at the audio outputs, depending on the selected signal sources:

Available Input Sources

- Two audio mono/stereo paths:
  - tdm/codec_din pin: Left and right samples from the audio tdm/codec serial port
  - Audio mono signals are built in the audio digital control.
- Auxiliary mono (auxr pin only) analog input path
- Handset main microphone (mic_main_p and mic_main_m pins)
- Local digital pulse driver (DPD) controlled by the I^2C changes the average voltage and the polarity (direction) of the vibrator H-bridge.

Available Outputs

- Audio transmit samples tdm/codec_dout through the TDM/codec audio serial port
- Predriver for external class D amplifier (predriv_right and predriv_left pins) available if hsovmid is not used
- Analog vibrator drive capability (can be driven by audio signal)

Table 13-5 lists the multiplexing and mixing capabilities for the available outputs; a left-most column output can be connected to a first-line input channel if there is an X at the intersection of the respective row and column.

Table 13-5. Multiplexing and Mixing Capabilities for the Available Outputs

SOURCE: EXT [1] → / INT [3] → / OUT ↓	MAIN MIC	AUXR	D+	SDR R1 [2]	SDR L1	SDR M1	SDR R2	SDR L2	SDR M2	DPD
Pre-carkit R		X[4]		X		X	X		X	
Pre-carkit L			X[4]		X	X		X	X	
Predriver R		X		X		X	X	X	X	
Predriver L					X	X	X	X	X	
DOUT (TDM/codec interface)	X	X	X							
Vibrator				X	X	X	X	X	X	X

(1) EXT: Available analog or digital input sources at the dedicated pins

(2) Blue boxes show path available only in option 1.

(3) INT: Additional input sources that can be generated internally and used as inputs

(4) When analog FM loop from AUXL/R to Hand-Free L/R is enabled on the device:

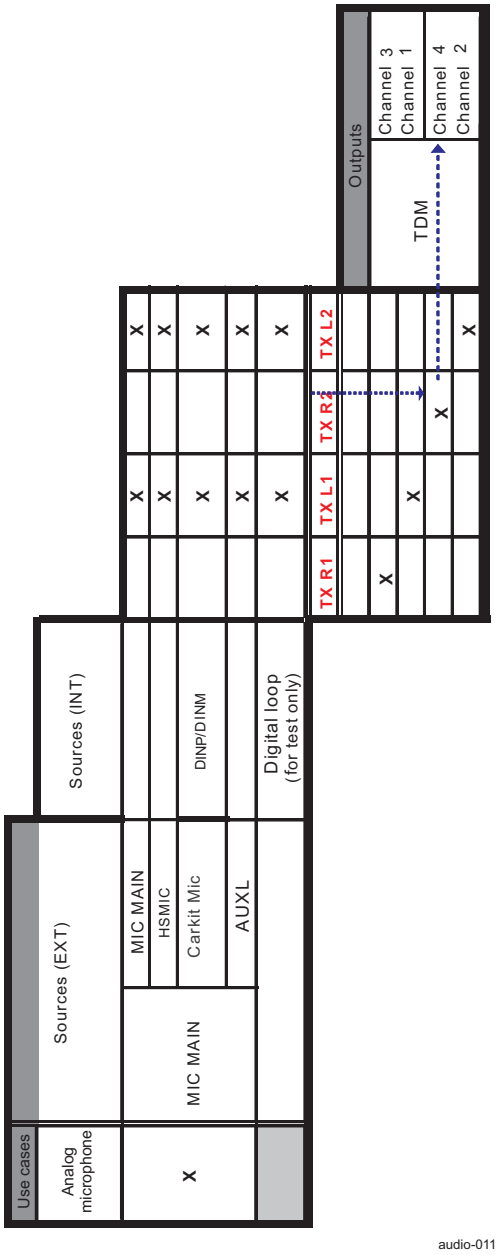
- If Hand-Free input selected comes from Audio domain (HFL_CTL[HFL_INPUT_SEL]<>0 and/or HFR_CTL[HFR_INPUT_SEL]<>0) the Audio clock (APLL_CTL[APLL_EN]=1) and one of the Audio Rx filter (OPTION[ARXR2_EN]=1 or/and OPTION[ARXL2_EN]=1) must be enabled.
- If Hand-Free input selected comes from Voice domain (HFL_CTL[HFL_INPUT_SEL] = 0 and HFR_CTL[HFR_INPUT_SEL] = 0) the Voice Rx filter (OPTION[ARXL1_VRX_EN]=1) must be enabled.

NOTE: For analog output mixing please note that the mixing operation is a summing and not an averaging operation. So if the inputs are close to Full scale, mixing the channels may cause saturation.

Mixing Capabilities on the Digital Transmit Path

Figure 13-6 lists the mixing capabilities of the uplink path for option 1. A connection between the left and right paths is possible if there is an X at the intersection of the respective row and column.

Figure 13-6. Available TX Path (Option 1)

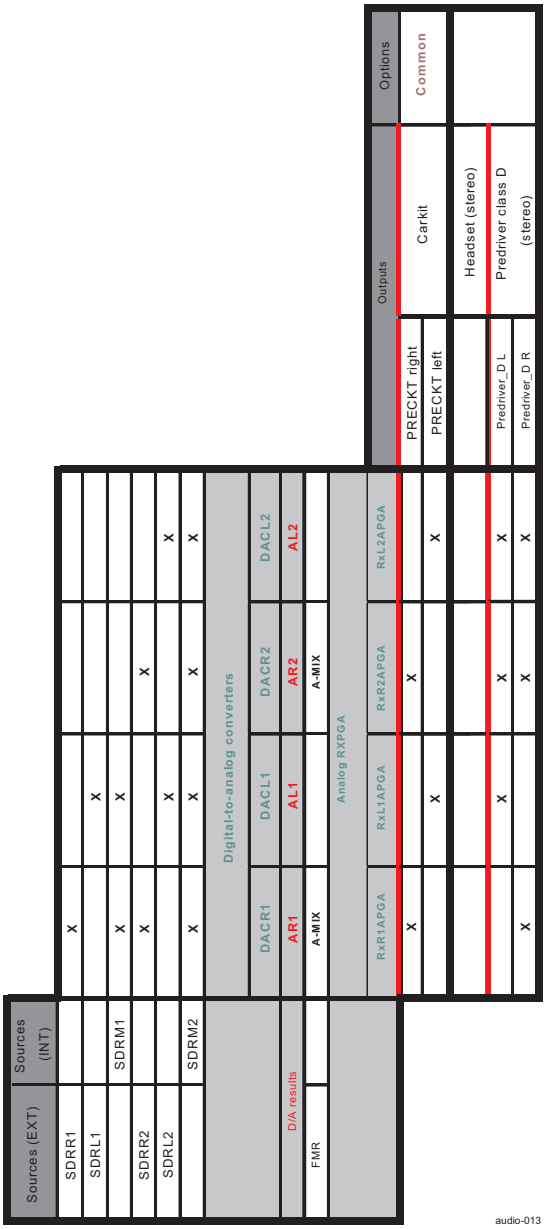


NOTE: X indicates possible path connection.
Example: MIC_SUB is routed to voice TDM/I2C interface channel 3.

13.4.3 RX Path

Figure 13-7 lists the available receiver paths for option 1.

Figure 13-7. Available RX Path (Option 1)



NOTE: X indicates possible path connection.
X* indicates path inverted (cross plus/minus).
D-MIX indicates possible digital mixing.
A-MIX indicates possible analog mixing.
Two output amplifiers can be driven simultaneously by an analog RXPGA amplifier.
Example: SDRR2 can be mixed with PCM DIN (or BT DIN) in the digital domain. The DAC output (AR2) can be mixed with FMR (in analog domain). The result can be routed to:

- Option A:
  - Hands-free right or left
  - Carkit right
  - Single-ended HS (ac-coupled) right
  - Predriver class D right or left (two maximum)
- Option B:
  - Hands-free right or left
  - Carkit right
  - Single-ended HS (dc-coupled) right (two maximum)

13.4.4 Digital Interface Details

13.4.4.1 Audio TDM/Codec Interface

The host processor uses the TDM/codec interface to send and receive audio data. Frame synchronization (tdmcodec_sync) defines the frame length in the TDM/I2S interface. Each frame consists of a fixed number of channels. Bits of each channel (sample) are clocked using tdmcodec_clk. Channels are in fixed order (1, 2, …) each 16 bits or 32 bits per sample. Serial data is transmitted in twos complement with the MSB first (signed word). LSBs are zero-padded because the true sample word width is less than 32 bits (16 or 24 bits).

The TDM/I2S interface clock (tdmcodec_clock) and frame synchronization (tdmcodec_sync) are generated from the 256*Fs (generated by the audio PLL).

The device supports the I2S, TDM, left-justified, and right-justified data formats.

The selection bits of the data formats are in the AUDIO_IF[4:3] AIF_FORMAT bit field:

- 00: Codec data format
- 01: Left-justified data format
- 10: Right-justified data format
- 11: TDM data format

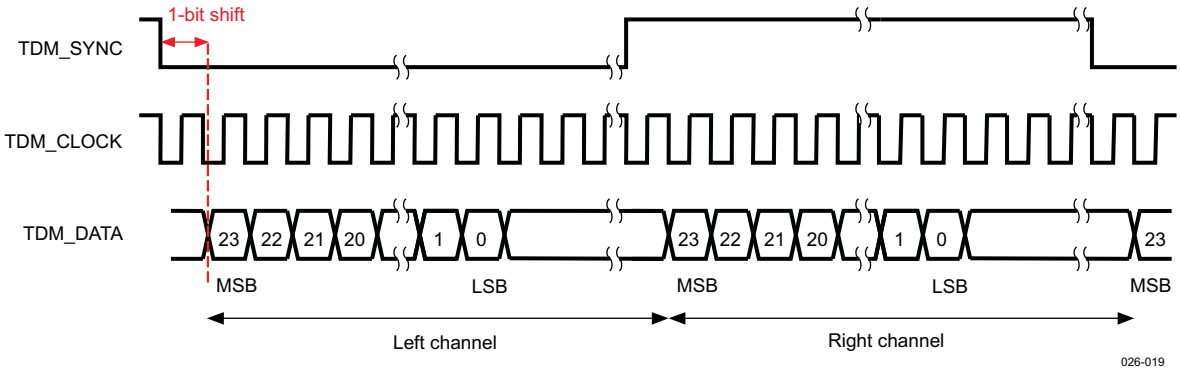
Sample length and word width are defined in the AUDIO_IF[6:5] DATA_WIDTH bit field:

- 00: Sample length: 16 bits; word width: 16 bits
- 01: Reserved
- 10: Sample length: 32 bits; word width: 16 bits
- 11: Sample length: 32 bits; word width: 24 bits

32 Bits Per Channel

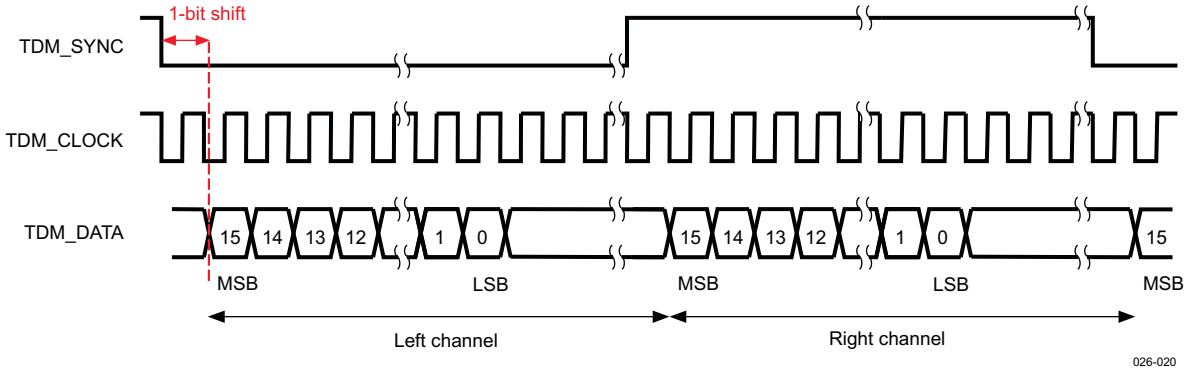
- Codec data format:
  - 24-bit data (see Figure 13-8)
    32-bit word size (for each left and right word):
    - TX: 24 bits of data (MSB first) and 8 padding bits at 0
    - RX: 24 bits of data (MSB first) and 8 dummy bits

Figure 13-8. Codec Mode; Sample Length 32 Bits; Word Width 24 Bits



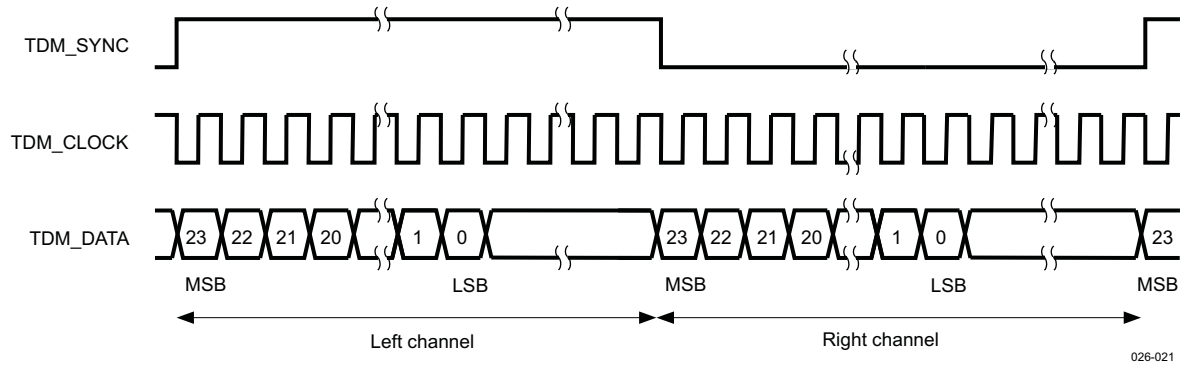
  - 16-bit data (see Figure 13-9)
    32-bit word size (for each left and right word):
    - TX: 16 bits of data (MSB first) and 16 padding bits at 0
    - RX: 16 bits of data (MSB first) and 16 dummy bits

Figure 13-9. Codec Mode; Sample Length 32 Bits; Word Width 16 Bits



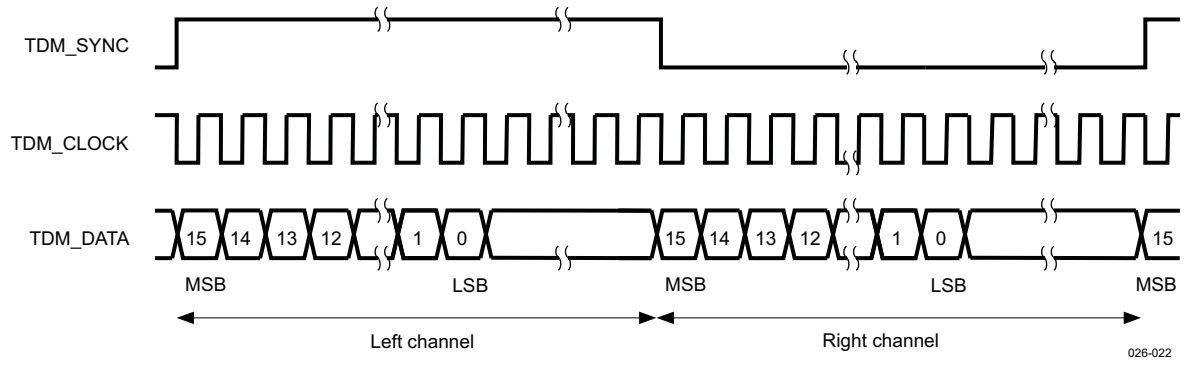
- Left-justified data format:
  - 24-bit data (see Figure 13-10)
    32-bit word size (for each left and right word):
    - TX: 24 bits of data (MSB first) and 8 padding bits at 0
    - RX: 24 bits of data (MSB first) and 8 dummy bits

Figure 13-10. Left-Justified Mode; Sample Length 32 Bits; Word Width 24 Bits



  - 16-bit data (see Figure 13-11)
    32-bit word size (for each left and right word):
    - TX: 16 bits of data (MSB first) and 16 padding bits at 0
    - RX: 16 bits of data (MSB first) and 16 dummy bits

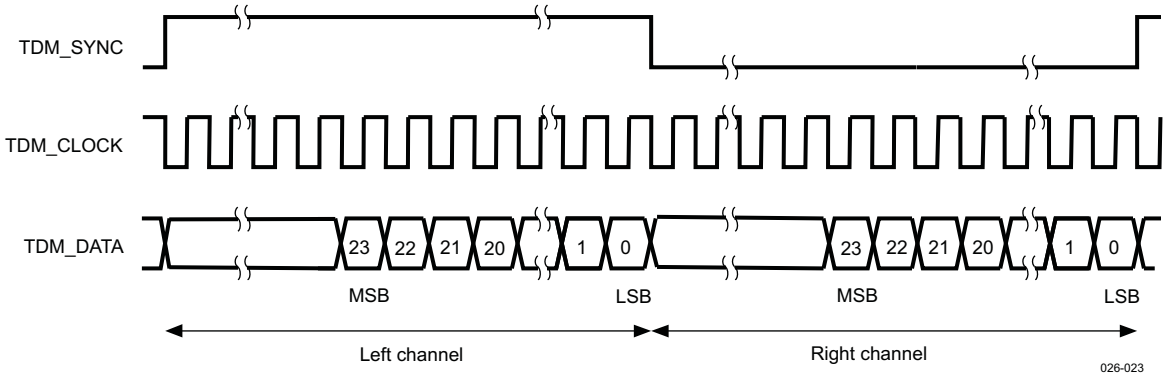
Figure 13-11. Left-Justified Mode; Sample Length 32 Bits; Word Width 16 Bits



- Right-justified data format:
  - 24-bit data (see Figure 13-12)
    32-bit word size (for each left and right word):

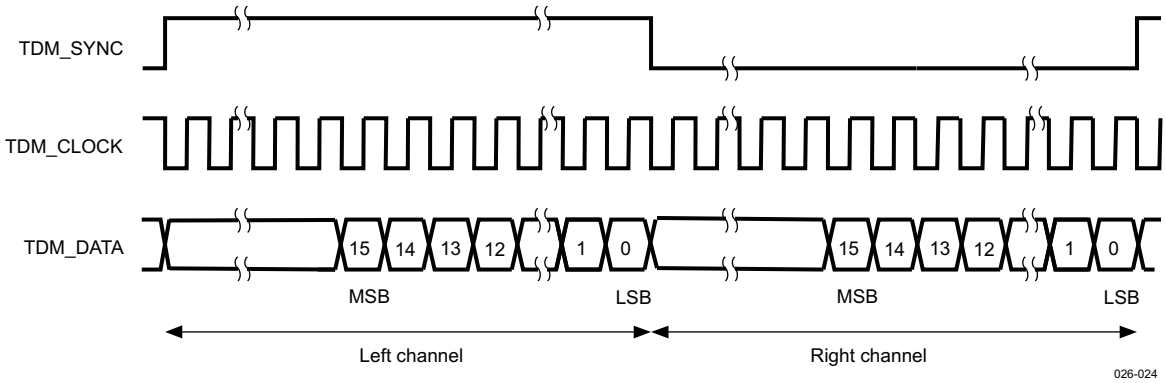
- TX: 8 padding bits at 0 and 24 bits of data (MSB first)
- RX: 8 dummy bits and 24 bits of data (MSB first)

Figure 13-12. Right-Justified Mode; Sample Length 32 Bits; Word Width 24 Bits



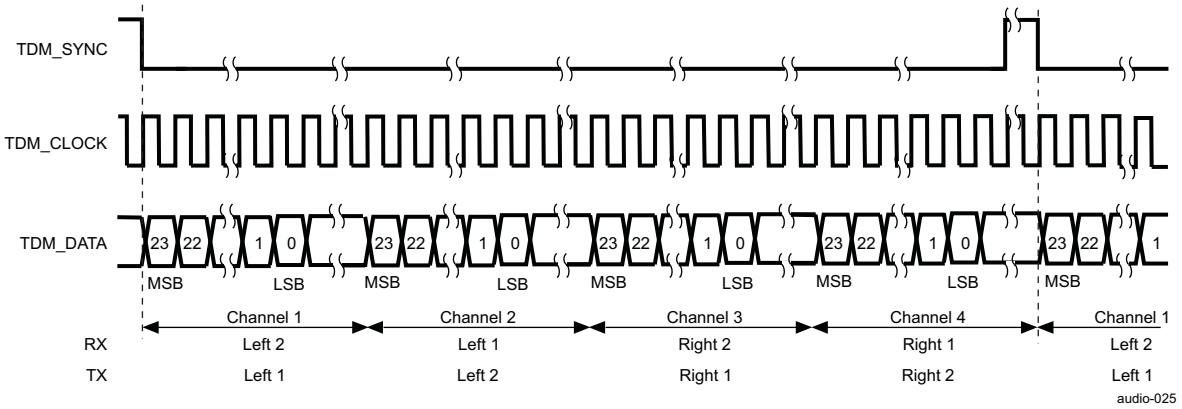
– 16-bit data (see Figure 13-13)
32-bit word size (for each left and right word):
- TX: 16 padding bits at 0 and 16 bits of data (MSB first)
- RX: 16 dummy bits and 16 bits of data (MSB first)

Figure 13-13. Right-Justified Mode; Sample Length 32 Bits; Word Width 16 Bits



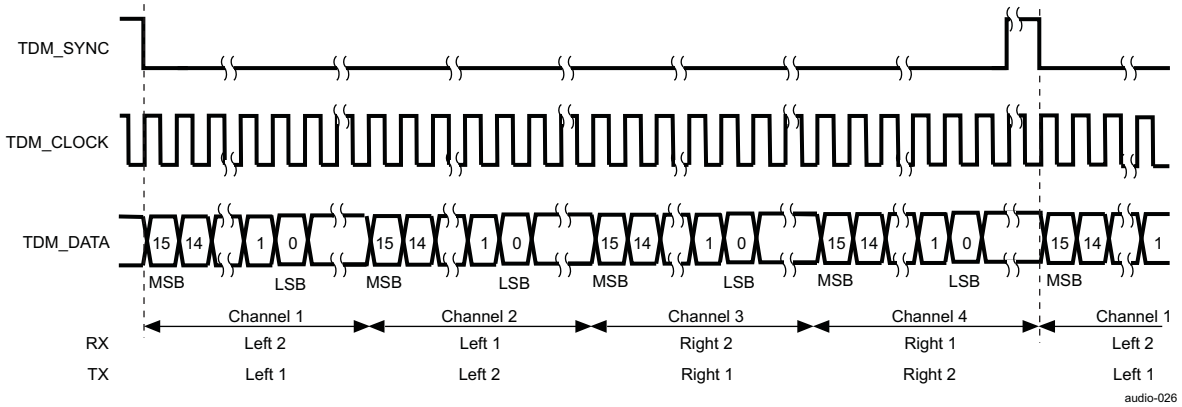
- TDM data format
Time slot mode defines a 128-bit-long frame composed of four time slots. Each slot is 32 bits long and corresponds to one of four RX paths (tdm/ codec_din) or one of four TX paths (tdm/codec_dout).
– 24-bit data (see Figure 13-14)
32-bit word size (for each left and right word):
  - TX: 24 bits of data (MSB first) and 8 padding bits at 0
  - RX: 24 bits of data (MSB first) and 8 dummy bits

Figure 13-14. TDM Mode; Sample Length 32 Bits; Word Width 24 Bits



– 16-bit data (see Figure 13-15)
  32-bit word size (for each left and right word):
  - TX: 16 bits of data (MSB first) and 16 padding bits at 0
  - RX: 16 bits of data (MSB first) and 16 dummy bits

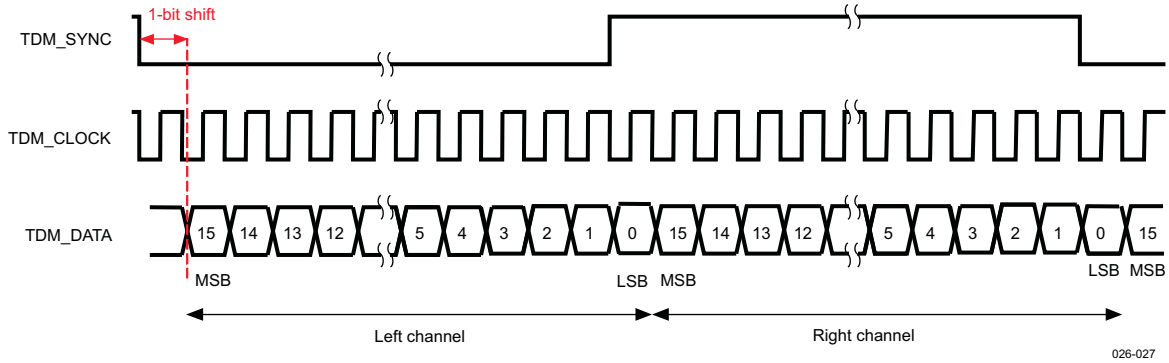
Figure 13-15. TDM Mode; Sample Length 32 Bits; Word Width 16 Bits



16 Bits Per Channel

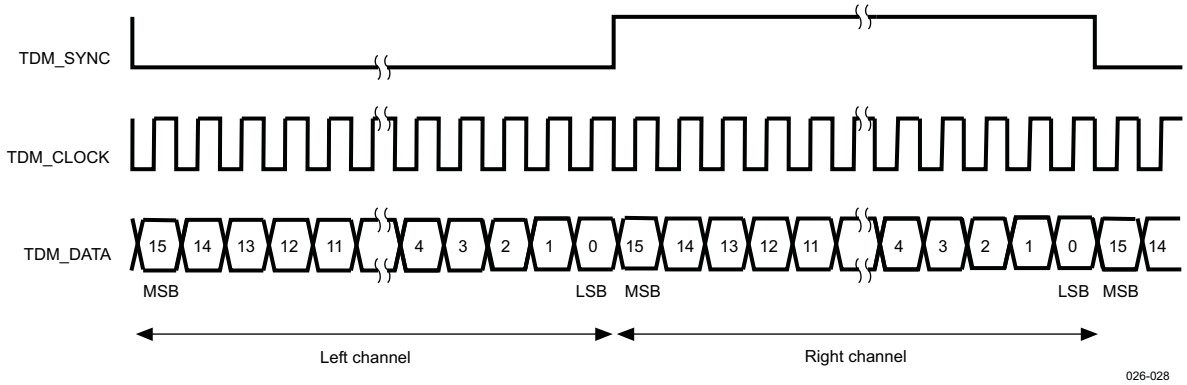
- Codec data format (see Figure 13-16)
  16-bit word size (for each left and right word): 16-bit data (MSB first)

Figure 13-16. Codec Mode; Sample Length 16 Bits; Word Width 16 Bits



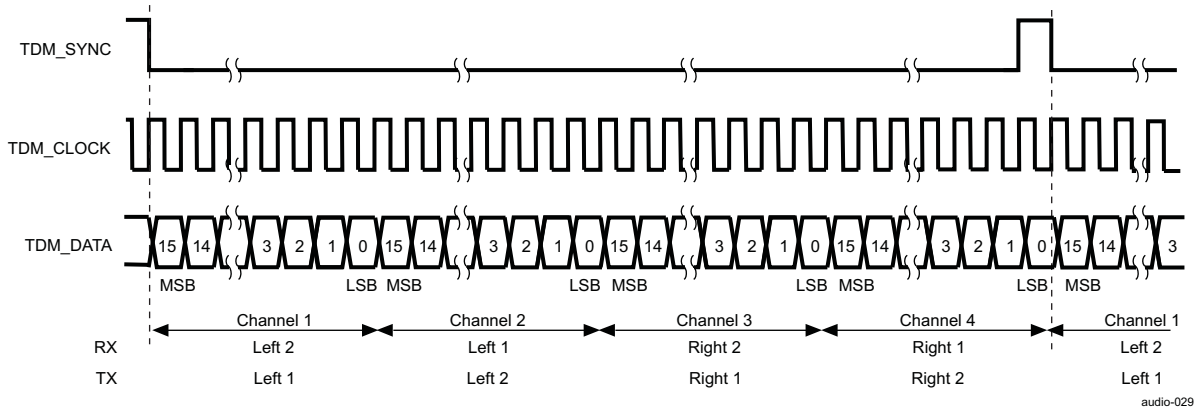
- Left-/right-justified data format (see Figure 13-17)
  16-bit word size (for each left and right word): 16-bit data (MSB first)

Figure 13-17. Left-/Right-Justified Mode; Sample Length 16 Bits; Word Width 16 Bits



- TDM data format (see Figure 13-18)
  Time-slot mode defines a 64-bit-long frame composed of four time slots. Each slot is 16 bits long and corresponds to one of four RX paths (tdm/codec_din) or one of four TX paths (tdm/codec_dout). 16-bit word size (for each left and right word): 16-bit data (MSB first).

Figure 13-18. TDM Mode; Sample Length 16 Bits; Word Width 16 Bits



Codec Right- and Left-Justified Interface

Output: tdm/codec_dout samples: Results from stereo audio A/D conversion or from the two stereo digital microphones (dig_mic_0 and dig_mic_1)

The audio A/D path can convert the following analog inputs:

- Differential stereo microphone (MIC)
- Single-ended auxiliary stereo microphone (AUX)
- Differential headset microphone (HSMIC)
- CEA-936A carkit through the device universal serial bus (USB) block (DIN)

The host processor uses the TDM/codec interface to send and receive audio data. Frame synchronization (TDMCODEC_SYNC) defines the frame length in the TDM/CODEC interface. Each frame consists of a fixed number of channels. Bits of each channel (sample) are clocked using tdmcodec_clk. Channels are in fixed order (1, 2, …) each 16 bits or 32 bits per sample, MSB first. LSBs are zero-padded because the true sample word width is less than 32 bits (16 or 24 bits).

The TDM/CODEC interface clock (tdmcodec_clock) and frame synchronization (tdmcodec_sync) are generated from the 256*Fs (generated by the audio PLL).

The device supports the codec, TDM, left-justified, and right-justified data formats.

The AUDIO_IF[4:3] AIF_FORMAT bit field selects the data format:

- 00: Codec
- 01: Left-justified
- 10: Right-justified
- 11: TDM

The sample length and word width are defined by the AUDIO_IF[6:5] DATA_WIDTH bit field:

- 00: Sample length: 16 bits; word width: 16 bits
- 01: Reserved
- 10: Sample length: 32 bits; word width: 16 bits
- 11: Sample length: 32 bits; word width: 24 bits

13.5 Programming Guide

This section provides general information about programming the audio section.

13.5.1 Voice/Audio Registers: Order of Programming

What can be changed on the fly (when the codec is running):

- Gain (digital or analog)
- Selection of output drivers

What cannot be changed on the fly:

- Enable/disable bits for high-pass filters
- TDM interface modes
- Sidetone when filter is running
- Priority bit for ADC clock (AVADV_CLK_PRIORITY)
- Digital mixing
- Bit swapping and master/slave selection for interfaces
- ALC setting
- Enable/disable boost or change effect setting while ARX is running
- Neither OPT_MODE nor sampling rates while an affected filter is running
- APLL frequency setting when the APLL is running

Special precautions for the following points:

- Changing from stereo to mono in application mode can be performed, but if the amplitude of the signals is large enough, the output saturates. To avoid this possibility, reduce the left and right gain by 6 dB before programming the mono mode.
- Changes cannot be made to enabled paths of a filter while it is running, but it is possible to turn them on or off at any time. For example, if both channels are enabled on audio RX2, one can be turned off and back on later. If voice is running RX and TX1, turning on TX2 on-the-fly is not possible. However, if audio RX2 is running, voice can be turned on at any time (enabling any combination of its RX/TX paths), and audio RX can be turned off later without disturbing voice.
- For ALC to be enabled, the codec must be on (CODEC_PDZ set to 1). ALC settings (threshold, release/attach/wait time, and interlock or separated ALC modes) can be changed only when ALC is off; when ALC is enabled, the settings cannot be changed.

Codec in off mode:

When the codec is off (CODECPDZ = 0), the digital filter, analog section, and audio interfaces are switched off; only the register interface is active. The registers can be accessed.

13.6 Registers

Table 13-6 lists the registers for programming the audio module. Table 13-10 through Table 13-34 describe the registers in detail.

Table 13-6. AUDIO_VOICE Register Summary

Register Name	Type	Register Width (Bits)	Physical Address	Reference
CODEC_MODE	RW	8	0x0000 0001	Table 13-7
OPTION	RW	8	0x0000 0002	Table 13-8
MICBIAS_CTL	RW	8	0x0000 0004	Table 13-9
ANAMICL	RW	8	0x0000 0005	Table 13-10
ANAMICR	RW	8	0x0000 0006	Table 13-11
AVADC_CTL	RW	8	0x0000 0007	Table 13-12
ADCMICSEL	RW	8	0x0000 0008	Table 13-13
DIGMIXING	RW	8	0x0000 0009	Table 13-14
ATXL1PGA	RW	8	0x0000 000A	Table 13-15
ATXR1PGA	RW	8	0x0000 000B	Table 13-16
AVTXL2PGA	RW	8	0x0000 000C	Table 13-17
AVTXR2PGA	RW	8	0x0000 000D	Table 13-18
AUDIO_IF	RW	8	0x0000 000E	Table 13-19
VOICE_IF	RW	8	0x0000 000F	Table 13-20
ARXR1PGA	RW	8	0x0000 0010	Table 13-21
ARXL1PGA	RW	8	0x0000 0011	Table 13-22
ARXR2PGA	RW	8	0x0000 0012	Table 13-23
ARXL2PGA	RW	8	0x0000 0013	Table 13-24
VRXPGA	RW	8	0x0000 0014	Table 13-25
VSTPGA	RW	8	0x0000 0015	Table 13-26
VRX2ARXPGA	RW	8	0x0000 0016	Table 13-27
AVDAC_CTL	RW	8	0x0000 0017	Table 13-28
ARX2VTXPGA	RW	8	0x0000 0018	Table 13-29
ARXL1_APGA_CTL	RW	8	0x0000 0019	Table 13-30
ARXR1_APGA_CTL	RW	8	0x0000 001A	Table 13-31
ARXL2_APGA_CTL	RW	8	0x0000 001B	Table 13-32
ARXR2_APGA_CTL	RW	8	0x0000 001C	Table 13-33
ATX2ARXPGA	RW	8	0x0000 001D	Table 13-34
BT_IF	RW	8	0x0000 001E	Table 13-35
BTPGA	RW	8	0x0000 001F	Table 13-36
BTSTPGA	RW	8	0x0000 0020	Table 13-37
EAR_CTL	RW	8	0x0000 0021	Table 13-38
HS_SEL	RW	8	0x0000 0022	Table 13-39
HS_GAIN_SET	RW	8	0x0000 0023	Table 13-40
HS_POPN_SET	RW	8	0x0000 0024	Table 13-41
PREDL_CTL	RW	8	0x0000 0025	Table 13-42
PREDR_CTL	RW	8	0x0000 0026	Table 13-43
PRECKL_CTL	RW	8	0x0000 0027	Table 13-44
PRECKR_CTL	RW	8	0x0000 0028	Table 13-45
HFL_CTL	RW	8	0x0000 0029	Table 13-46
HFR_CTL	RW	8	0x0000 002A	Table 13-47
ALC_CTL	RW	8	0x0000 002B	Table 13-48
ALC_SET1	RW	8	0x0000 002C	Table 13-49
ALC_SET2	RW	8	0x0000 002D	Table 13-50

Table 13-6. AUDIO_VOICE Register Summary (continued)

Register Name	Type	Register Width (Bits)	Physical Address	Reference
BOOST_CTL	RW	8	0x0000 002E	Table 13-51
SOFTVOL_CTL	RW	8	0x0000 002F	Table 13-52
DTMF_FREQSEL	RW	8	0x0000 0030	Table 13-53
DTMF_TONEXT1H	RW	8	0x0000 0031	Table 13-54
DTMF_TONEXT1L	RW	8	0x0000 0032	Table 13-55
DTMF_TONEXT2H	RW	8	0x0000 0033	Table 13-56
DTMF_TONEXT2L	RW	8	0x0000 0034	Table 13-57
DTMF_TONOFF	RW	8	0x0000 0035	Table 13-58
DTMF_WANONOFF	RW	8	0x0000 0036	Table 13-59
CODEC_RX_SCRAMBLE_H	RW	8	0x0000 0037	Table 13-60
CODEC_RX_SCRAMBLE_M	RW	8	0x0000 0038	Table 13-61
CODEC_RX_SCRAMBLE_L	RW	8	0x0000 0039	Table 13-62
APLL_CTL	RW	8	0x0000 003A	Table 13-63
DTMF_CTL	RW	8	0x0000 003B	Table 13-64
DTMF_PGA_CTL2	RW	8	0x0000 003C	Table 13-65
DTMF_PGA_CTL1	RW	8	0x0000 003D	Table 13-66
MISC_SET_1	RW	8	0x0000 003E	Table 13-67
PCMBTMUX	RW	8	0x0000 003F	Table 13-68
RX_PATH_SEL	RW	8	0x0000 0043	Table 13-69
VDL_APGA_CTL	RW	8	0x0000 0044	Table 13-70
VIBRA_CTL	RW	8	0x0000 0045	Table 13-71
VIBRA_SET	RW	8	0x0000 0046	Table 13-72
ANAMIC_GAIN	RW	8	0x0000 0048	Table 13-73
MISC_SET_2	RW	8	0x0000 0049	Table 13-74

Table 13-7. CODEC_MODE Register

Address Offset	0x01		
Physical Address	0x0000 0001	**Instance**	AUDIO_VOICE
Description	System mode control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
APLL_RATE				SEL_16K	SPARE	CODECPDZ	OPT_MODE

Bits	Field Name	Description	Type	Reset Off
7:4	APLL_RATE	Audio mode: Select sampling frequence (Fs). 0x0: 8 kHz 0x1: 11.025 kHz 0x2: 12 kHz 0x4: 16 kHz 0x5: 22.05 kHz 0x6: 24 kHz 0x8: 32 kHz 0x9: 44.1 kHz 0xA: 48 kHz	RW	0x0

Bits	Field Name	Description	Type	Reset Off
		0xE: 96 kHz		
3	SEL_16K	Voice mode: Select 16-kHz mode. 0x0: Sample at 8 kHz. 0x1: Sample at 16 kHz.	RW	0
2	SPARE	Spare bit	RW	0
1	CODEECPDZ	Codec power control bit 0x0: Codec is off. 0x1: Codec is on.	RW	0
0	OPT_MODE	Audio and voice option selection 0x0: Option 2: Voice uplink (stereo) and downlink (Mono) + 1 RX and TX stereo audio paths 0x1: Option 1: 2 RX and TX stereo audio paths	RW	0

Table 13-8. OPTION Register

Address Offset	0x02		
Physical Address	0x0000 0002	**Instance**	AUDIO_VOICE
Description	Audio/voice digital filter power control Two interpretations of the option register, depending on whether option 1 or option 2 is enabled (CODEC_MODE register, OPT_MODE bit)		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ARXR2_EN	ARXL2_EN	ARXR1_EN	ARXL1_VRX_EN	ATXR2_VTXR_EN	ATXL2_VTXL_EN	ATXR1_EN	ATXL1_EN

Bits	Field Name	Description	Type	Reset Off
7	ARXR2_EN	Audio RX right 2 enable (options 1 and 2) 0x0: Disabled 0x1: Enabled	RW	0
6	ARXL2_EN	Audio RX left 2 enable (options 1 and 2) 0x0: Disabled 0x1: Enabled	RW	0
5	ARXR1_EN	Audio RX right 1 enable (option 1 only). Two interpretations: Option 1 is ARXR1_EN; option 2 is reserved. 0x0: Disabled 0x1: Enabled	RW	0
4	ARXL1_VRX_EN	Audio RX left 1 enable (option 1) or voice RX enable (option 2). Two interpretations: Option 1 is ARXL1_EN; option 2 is VRX_EN. 0x0: Disabled 0x1: Enabled	RW	0
3	ATXR2_VTXR_EN	Audio TX right 2 enable (option 1) or voice TX right enable (option 2). Two interpretations: Option 1 is ATXR2_EN; option 2 is VTXR_EN. 0x0: Disabled 0x1: Enabled	RW	0

Bits	Field Name	Description	Type	Reset Off
2	ATXL2_VTXL_EN	Audio TX left 2 enable (option 1) or voice TX left enable (option 2). Two interpretations: Option 1 is ATXL2_EN; 2 is VTXL_EN. 0x0: Disabled 0x1: Enabled	RW	0
1	ATXR1_EN	Audio TX right 1 enable (options 1 and 2) 0x0: Disabled 0x1: Enabled	RW	0
0	ATXL1_EN	Audio TX left 1 enable (options 1 and 2) 0x0: Disabled 0x1: Enabled	RW	0

Table 13-9. MICBIAS_CTL Register

Address Offset	0x04		
Physical Address	0x0000 0004	**Instance**	AUDIO_VOICE
Description	Microphone bias and analog microphone amplifier power control register. If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SPARE	MICBIAS2_CTL	MICBIAS1_CTL	Reserved		HSMICBIAS_EN	MICBIAS2_EN	MICBIAS1_EN

Bits	Field Name	Description	Type	Reset Off
7	SPARE	Spare bit	RW	0
6	MICBIAS2_CTL	MICBIAS2 control bit 0x0: Analog microphone bias 0x1: Digital microphone bias	RW	0
5	MICBIAS1_CTL	MICBIAS1 control bit 0x0: Analog microphone bias 0x1: Digital microphone bias	RW	0
4:3	Reserved		RW	0x0
2	HSMICBIAS_EN	Headset microphone bias power control 0x0: Disabled 0x1: Enabled	RW	0
1	MICBIAS2_EN	Submicrophone/digital microphone 1 bias power control 0x0: Disabled 0x1: Enabled	RW	0
0	MICBIAS1_EN	Main microphone/digital microphone 0 bias power control 0x0: Disabled 0x1: Enabled	RW	0

Table 13-10. ANAMICL Register

Address Offset	0x05		
Physical Address	0x0000 0005	**Instance**	AUDIO_VOICE
Description	Analog microphone left control and offset cancellation control register Analog microphone left: Main microphone, headset microphone, carkit microphone, or auxiliary left microphone can be routed to the input of the A/D converters separately (only one enable bit at 1). If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
CNCL_OFFSET_START	OFFSET_CNCL_SEL		MICAMPL_EN	CKMIC_EN	AUXL_EN	HSMIC_EN	MAINMIC_EN

Bits	Field Name	Description	Type	Reset Off
7	CNCL_OFFSET_ START	Control bit to initiate offset cancellation of the five RX paths. A 1 initiates offset cancellation. When the offset has been calculated, this bit goes back to 0 (self-clearing bit). 0x0: Application mode 0x1: Offset cancellation initiated	RW	0
6:5	OFFSET_CNCL_SEL	Control word to select the paths for the offset cancellation. 0x0: Audio RX left 1 and right 1 selected 0x1: Audio RX left 2 and right 2 selected 0x2: Voice RX selected 0x3: All channels selected	RW	0x0
4	MICAMPL_EN	Left microphone amplifier power control 0x0: Power-down mode 0x1: Application mode	RW	0
3	CKMIC_EN	Carkit microphone input enable control bit 0x0: Disabled 0x1: Enabled	RW	0
2	AUXL_EN	AUXL input enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1	HSMIC_EN	Headset microphone enable control bit 0x0: Disabled 0x1: Enabled	RW	0
0	MAINMIC_EN	Main microphone input enable control bit 0x0: Disabled 0x1: Enabled	RW	0

Table 13-11. ANAMICR Register

Address Offset	0x06		
Physical Address	0x0000 0006	**Instance**	AUDIO_VOICE
Description	Analog microphone right control register Analog microphone right: Submicrophone or auxiliary right microphone can be routed to the input of the A/D converters separately (only one enable bit at 1). If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED			MICAMPR_EN	RESERVED	AUXR_EN	RESERVED	SUBMIC_EN

Bits	Field Name	Description	Type	Reset Off
7:5	Reserved		RW	0x0
4	MICAMPR_EN	Right microphone amplifier power control 0x0: Power-down mode 0x1: Application mode	RW	0
3	Reserved		RW	0
2	AUXR_EN	AUXR input enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1	Reserved		RW	0
0	SUBMIC_EN	Submicrophone input enable control bit 0x0: Disabled 0x1: Enabled	RW	0

Table 13-12. AVADC_CTL Register

Address Offset	0x07		
Physical Address	0x0000 0007	**Instance**	AUDIO_VOICE
Description	Audio/voice ADC control register If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED				ADCL_EN	AVADC_CLK_PRIORITY	ADCR_EN	RESERVED

Bits	Field Name	Description	Type	Reset Off
7:4	Reserved	Reserved	RW	0x0
3	ADCL_EN	ADCL power control 0x0: Power-down mode 0x1: Application mode	RW	0
2	AVADC_CLK_ PRIORITY	When the codec is in option 2, and if for the TX channel, the audio and voice are enabled at the same time, then this bit defines the priority. 0x0: Voice high priority 0x1: Audio high priority	RW	0
1	ADCR_EN	ADCR power control 0x0: Disabled 0x1: Enabled	RW	0
0	Reserved		RW	0

Table 13-13. ADCMICSEL Register

Address Offset	0x08		
Physical Address	0x0000 0008	**Instance**	AUDIO_VOICE
Description	Digital audio/voice TX filter input select		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED				DIGMIC1_EN	TX2IN_SEL	DIGIC0_EN	TX1IN_SEL

Bits	Field Name	Description	Type	Reset Off
7:4	Reserved	Reserved	RW	0x0
3	DIGMIC1_EN	Digital microphone 1 interface power control 0x0: Power-down mode 0x1: Application mode	RW	0
2	TX2IN_SEL	TX2 input select in audio mode 0x0: ADC input. ADCL routed to TXL2, ACDR routed to TXR2 0x1: Digital microphone 1	RW	0
1	DIGMIC0_EN	Digital microphone 0 interface power control 0x0: Power-down mode 0x1: Application mode	RW	0
0	TX1IN_SEL	TX1 input select in audio mode 0x0: ADC input. ADCL routed to TXL1, ADCR routed to TXR1 0x1: Digital microphone 0	RW	0

Table 13-14. DIGMIXING Register

Address Offset	0x09		
Physical Address	0x0000 0009	**Instance**	AUDIO_VOICE
Description	Voice/audio digital mixing control register The mixing between audio and voice is available only in option 2 (OPT_MODE = 0). In option 1, the setting of this register must be 0x0 (reset value).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ARX1_MIXING		ARX2_MIXING		VTX_MIXING		RESERVED	

Bits	Field Name	Description	Type	Reset Off
7:6	ARX1_MIXING	Audio RX digital mixing control word (VRX to ARX1) 0x0: Off 0x1: Voice RX added to the audio RX left 1 0x2: Voice RX added to the audio RX right 1 0x3: Voice RX added to both audio RX left 1 and audio RX right 1	RW	0x0
5:4	ARX2_MIXING	Audio RX digital mixing control word (VRX to ARX2) 0x0: Off 0x1: Voice RX added to the audio RX left 2 0x2: Voice RX added to the audio RX right 2 0x3: Voice RX added to both audio RX left 2 and audio RX right 2	RW	0x0
3:2	VTX_MIXING	Voice TX digital mixing control word (ARX to VTX2) 0x0: Off 0x1: Audio RX added to the voice TX left 2 0x2: Audio RX added to the voice TX right 2 0x3: Audio RX added to both voice TX left 2 and voice TX right 2	RW	0x0
1:0	Reserved		RW	0x0

Table 13-15. ATXL1PGA Register

Address Offset	0x0A		
Physical Address	0x0000 000A	**Instance**	AUDIO_VOICE
Description	Audio TXL1 gain control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED			ATXL1PGA_GAIN				

Bits	Field Name	Description	Type	Reset Off
7:5	Reserved		RW	0x0
4:0	ATXL1PGA_GAIN	TXL1 digital gain control 0x0: 0 dB 0x1: 1 dB 0x2: 2 dB 0x3: 3 dB 0x4: 4 dB 0x5: 5 dB 0x6: 6 dB	RW	0x0F

Bits	Field Name	Description		Type	Reset Off
		0x7:	7 dB		
		0x8:	8 dB		
		0x9:	9 dB		
		0xA:	10 dB		
		0xB:	11 dB		
		0xC:	12 dB		
		0xD:	13 dB		
		0xE:	14 dB		
		0xF:	15 dB		
		0x10:	16 dB		
		0x11:	17 dB		
		0x12:	18 dB		
		0x13:	19 dB		
		0x14:	20 dB		
		0x15:	21 dB		
		0x16:	22 dB		
		0x17:	23 dB		
		0x18:	24 dB		
		0x19:	25 dB		
		0x1A:	26 dB		
		0x1B:	27 dB		
		0x1C:	28 dB		
		0x1D:	29 dB		
		0x1E:	30 dB		
		0x1F:	31 dB		

Table 13-16. ATXR1PGA Register

Address Offset	0x0B		
Physical Address	0x0000 000B	**Instance**	AUDIO_VOICE
Description	Audio TXR1 gain control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED				ATXR1PGA_GAIN			

Bits	Field Name	Description		Type	Reset Off
7:5	Reserved			RW	0x0
4:0	ATXR1PGA_GAIN	TXL1 digital gain control		RW	0x0F
		0x0:	0 dB		
		0x1:	1 dB		
		0x2:	2 dB		
		0x3:	3 dB		
		0x4:	4 dB		
		0x5:	5 dB		
		0x6:	6 dB		
		0x7:	7 dB		
		0x8:	8 dB		
		0x9:	9 dB		

Bits	Field Name	Description		Type	Reset Off
		0xA:	10 dB		
		0xB:	11 dB		
		0xC:	12 dB		
		0xD:	13 dB		
		0xE:	14 dB		
		0xF:	15 dB		
		0x10:	16 dB		
		0x11:	17 dB		
		0x12:	18 dB		
		0x13:	19 dB		
		0x14:	20 dB		
		0x15:	21 dB		
		0x16:	22 dB		
		0x17:	23 dB		
		0x18:	24 dB		
		0x19:	25 dB		
		0x1A:	26 dB		
		0x1B:	27 dB		
		0x1C:	28 dB		
		0x1D:	29 dB		
		0x1E:	30 dB		
		0x1F:	31 dB		

Table 13-17. AVTXL2PGA Register

Address Offset	0x0C		
Physical Address	0x0000 000C	**Instance**	AUDIO_VOICE
Description	Audio/voice TXL2 gain control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED			AVTXL2PGA_GAIN				

Bits	Field Name	Description		Type	Reset Off
7:5	Reserved			RW	0x0
4:0	AVTXL2PGA_GAIN	TXL1 digital gain control		RW	0x0F
		0x0:	0 dB		
		0x1:	1 dB		
		0x2:	2 dB		
		0x3:	3 dB		
		0x4:	4 dB		
		0x5:	5 dB		
		0x6:	6 dB		
		0x7:	7 dB		
		0x8:	8 dB		
		0x9:	9 dB		
		0xA:	10 dB		
		0xB:	11 dB		
		0xC:	12 dB		

Bits	Field Name	Description		Type	Reset Off
		0xD:	13 dB		
		0xE:	14 dB		
		0xF:	15 dB		
		0x10:	16 dB		
		0x11:	17 dB		
		0x12:	18 dB		
		0x13:	19 dB		
		0x14:	20 dB		
		0x15:	21 dB		
		0x16:	22 dB		
		0x17:	23 dB		
		0x18:	24 dB		
		0x19:	25 dB		
		0x1A:	26 dB		
		0x1B:	27 dB		
		0x1C:	28 dB		
		0x1D:	29 dB		
		0x1E:	30 dB		
		0x1F:	31 dB		

Table 13-18. AVTXR2PGA Register

Address Offset	0x0D		
Physical Address	0x0000 000D	**Instance**	AUDIO_VOICE
Description	Audio/voice TXR2 gain control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED			AVTXR2PGA_GAIN				

Bits	Field Name	Description		Type	Reset Off
7:5	Reserved			RW	0x0
4:0	AVTXR2PGA_GAIN	TXL1 digital gain control		RW	0x0F
		0x0:	0 dB		
		0x1:	1 dB		
		0x2:	2 dB		
		0x3:	3 dB		
		0x4:	4 dB		
		0x5:	5 dB		
		0x6:	6 dB		
		0x7:	7 dB		
		0x8:	8 dB		
		0x9:	9 dB		
		0xA:	10 dB		
		0xB:	11 dB		
		0xC:	12 dB		
		0xD:	13 dB		
		0xE:	14 dB		
		0xF:	15 dB		

Bits	Field Name	Description	Type	Reset Off
		0x10: 16 dB		
		0x11: 17 dB		
		0x12: 18 dB		
		0x13: 19 dB		
		0x14: 20 dB		
		0x15: 21 dB		
		0x16: 22 dB		
		0x17: 23 dB		
		0x18: 24 dB		
		0x19: 25 dB		
		0x1A: 26 dB		
		0x1B: 27 dB		
		0x1C: 28 dB		
		0x1D: 29 dB		
		0x1E: 30 dB		
		0x1F: 31 dB		

Table 13-19. AUDIO_IF Register

Address Offset	0x0E		
Physical Address	0x0000 000E	**Instance**	AUDIO_VOICE
Description	Control mode for audio interface If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
AIF_SLAVE_EN	DATA_WIDTH		AIF_FORMAT		AIF_TRI_EN	CLK256FS_EN	AIF_EN

Bits	Field Name	Description	Type	Reset Off
7	AIF_SLAVE_EN	0x0: TDM/CODEC master mode	RW	0
		0x1: TDM/CODEC in slave mode		
		Caution: In the TDM mode (AIF_FORMAT = 0x3), the TDM/CODEC must be configured in master mode.		
6:5	DATA_WIDTH	Word width and sample length control for audio interface	RW	0x0
		0x0: 16-bit sample length (slot), 16-bit word width		
		0x1: Reserved		
		0x2: 32-bit sample length (slot), 16-bit word width		
		0x3: 32-bit sample length (slot), 24-bit word width		
4:3	AIF_FORMAT	Select audio interface data format	RW	0x0
		0x0: codec mode data format		
		0x1: Left-justified mode data format		
		0x2: Right-justified mode data format		
		0x3: TDM mode data format (available only in option 1)		
2	AIF_TRI_EN	High impedance for audio interface output pins	RW	0

Bits	Field Name	Description	Type	Reset Off
		0x0: Application mode		
		0x1: High impedance		
1	CLK256FS_EN	Control for 256FS CLK output (128 or 256 * Fs)	RW	0
		0x0: Disabled		
		0x1: Enabled		
0	AIF_EN	Audio serial interface control mode	RW	0
		0x0: Off mode DIN/DOUT/SYN/CLK = L		
		0x1: Application mode		

Table 13-20. VOICE_IF Register

Address Offset	0x0F		
Physical Address	0x0000 000F	**Instance**	AUDIO_VOICE
Description	Control mode for voice interface If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
VIF_SLAVE_EN	VIF_DIN_EN	VIF_DOUT_EN	VIF_SWAP	VIF_FORMAT	VIF_TRI_EN	VIF_SUB_EN	VIF_SUB_EN

Bits	Field Name	Description	Type	Reset Off
7	VIF_SLAVE_EN	Select slave mode for voice PCM and Bluetooth PCM interfaces	RW	0
		0x0: Voice PCM master mode		
		0x1: Voice PCM slave mode		
6	VIF_DIN_EN	Enable voice input	RW	0
		0x0: Off mode vdr = L		
		0x1: Application mode		
5	VIF_DOUT_EN	Enable voice output	RW	0
		0x0: Off mode pcm_vdx = L		
		0x1: Application mode		
4	VIF_SWAP	Control to swap PCM_VDX and PCM_VDR	RW	0
		0x0: I/O not swapped		
		0x1: I/O swapped		
3	VIF_FORMAT	Select voice and Bluetooth interface data format	RW	0
		0x0: Mode 1 (writing on PCM_VCK rising edge)		
		0x1: Mode 2 (writing on PCM_VCK falling edge)		
2	VIF_TRI_EN	Set the voice interface output pins to high impedance	RW	0
		0x0: Application mode		
		0x1: High impedance		
1	VIF_SUB_EN	Voice and Bluetooth interface power control PCM_VCK and PCM_VFS in low state (L) if VIF_EN = 0 and BT_EN = 0 (see Table 13-35)	RW	0
		0x0: Disabled (mono TX)		
		0x1: Enabled (stereo TX)		

Bits	Field Name	Description	Type	Reset Off
0	VIF_EN	Voice interface power control 0x0: Mode VDR and PCM_VDX = L 0x1: Application mode	RW	0

Table 13-21. ARXR1PGA Register

Address Offset	0x10		
Physical Address	0x0000 0010	**Instance**	AUDIO_VOICE
Description	Audio RXR1 gain control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ARXR1PGA_CGAIN		ARXR1PGA_FGAIN					

Bits	Field Name	Description	Type	Reset Off
7:6	ARXR1PGA_CGAIN	Digital coarse gain control 0x0: 0 dB 0x1: 6 dB 0x2: 12 dB 0x3: 12 dB	RW	0x0
5:0	ARXR1PGA_FGAIN	Digital fine gain control 0x0: Mute 0x1: –62 dB 0x2: –61 dB 0x3: –60 dB 0x4: –59 dB 0x5: –58 dB 0x6: –57 dB 0x7: –56 dB 0x8: –55 dB 0x9: –54 dB 0xA: –53 dB 0xB: –52 dB 0xC: –51 dB 0xD: –50 dB 0xE: –49 dB 0xF: –48 dB 0x10: –47 dB 0x11: –46 dB 0x12: –45 dB 0x13: –44 dB 0x14: –43 dB 0x15: –42 dB 0x16: –41 dB 0x17: –40 dB 0x18: –39 dB 0x19: –38 dB 0x1A: –37 dB 0x1B: –36 dB 0x20: –31 dB 0x21: –30 dB 0x22: –29 dB 0x23: –28 dB 0x24: –27 dB 0x25: –26 dB 0x26: –25 dB 0x27: –24 dB 0x28: –23 dB 0x29: –22 dB 0x2A: –21 dB 0x2B: –20 dB 0x2C: –19 dB 0x2D: –18 dB 0x2E: –17 dB 0x2F: –16 dB 0x30: –15 dB 0x31: –14 dB 0x32: –13 dB 0x33: –12 dB 0x34: –11 dB 0x35: –10 dB 0x36: –9 dB 0x37: –8 dB 0x38: –7 dB 0x39: –6 dB 0x3A: –5 dB 0x3B: –4 dB	RW	0x3F

Bits	Field Name	Description				Type	Reset Off
		0x1C:	–35 dB	0x3C:	–3 dB		
		0x1D:	–34 dB	0x3D:	–2 dB		
		0x1E:	–33 dB	0x3E:	–1 dB		
		0x1F:	–32 dB	0x3F:	0 dB		

Table 13-22. ARXL1PGA Register

Address Offset	0x11		
Physical Address	0x0000 0011	**Instance**	AUDIO_VOICE
Description	Audio RXL1 gain control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ARXL1PGA_CGAIN		ARXL1PGA_FGAIN					

Bits	Field Name	Description				Type	Reset Off
7:6	ARXL1PGA_CGAIN	Digital coarse gain control				RW	0x0
		0x0:	0 dB				
		0x1:	6 dB				
		0x2:	12 dB				
		0x3:	12 dB				
5:0	ARXL1PGA_FGAIN	Digital fine gain control				RW	0x3F
		0x0:	Mute	0x20:	–31 dB		
		0x1:	–62 dB	0x21:	–30 dB		
		0x2:	–61 dB	0x22:	–29 dB		
		0x3:	–60 dB	0x23:	–28 dB		
		0x4:	–59 dB	0x24:	–27 dB		
		0x5:	–58 dB	0x25:	–26 dB		
		0x6:	–57 dB	0x26:	–25 dB		
		0x7:	–56 dB	0x27:	–24 dB		
		0x8:	–55 dB	0x28:	–23 dB		
		0x9:	–54 dB	0x29:	–22 dB		
		0xA:	–53 dB	0x2A:	–21 dB		
		0xB:	–52 dB	0x2B:	–20 dB		
		0xC:	–51 dB	0x2C:	–19 dB		
		0xD:	–50 dB	0x2D:	–18 dB		
		0xE:	–49 dB	0x2E:	–17 dB		
		0xF:	–48 dB	0x2F:	–16 dB		
		0x10:	–47 dB	0x30:	–15 dB		
		0x11:	–46 dB	0x31:	–14 dB		
		0x12:	–45 dB	0x32:	–13 dB		
		0x13:	–44 dB	0x33:	–12 dB		
		0x14:	–43 dB	0x34:	–11 dB		
		0x15:	–42 dB	0x35:	–10 dB		
		0x16:	–41 dB	0x36:	–9 dB		
		0x17:	–40 dB	0x37:	–8 dB		
		0x18:	–39 dB	0x38:	–7 dB		
		0x19:	–38 dB	0x39:	–6 dB		
		0x1A:	–37 dB	0x3A:	–5 dB		

Bits	Field Name	Description				Type	Reset Off
		0x1B:	–36 dB	0x3B:	–4 dB		
		0x1C:	–35 dB	0x3C:	–3 dB		
		0x1D:	–34 dB	0x3D:	–2 dB		
		0x1E:	–33 dB	0x3E:	–1 dB		
		0x1F:	–32 dB	0x3F:	0 dB		

Table 13-23. ARXR2PGA Register

Address Offset	0x12		
Physical Address	0x0000 0012	**Instance**	AUDIO_VOICE
Description	Audio RXR2 gain control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ARXL2PGA_CGAIN		ARXL2PGA_FGAIN					

Bits	Field Name	Description				Type	Reset Off
7:6	ARXR2PGA_CGAIN	Digital coarse gain control				RW	0x0
		0x0:	0 dB				
		0x1:	6 dB				
		0x2:	12 dB				
		0x3:	12 dB				
5:0	ARXR2PGA_FGAIN	Digital fine gain control				RW	0x3F
		0x0:	Mute	0x20:	–31 dB		
		0x1:	–62 dB	0x21:	–30 dB		
		0x2:	–61 dB	0x22:	–29 dB		
		0x3:	–60 dB	0x23:	–28 dB		
		0x4:	–59 dB	0x24:	–27 dB		
		0x5:	–58 dB	0x25:	–26 dB		
		0x6:	–57 dB	0x26:	–25 dB		
		0x7:	–56 dB	0x27:	–24 dB		
		0x8:	–55 dB	0x28:	–23 dB		
		0x9:	–54 dB	0x29:	–22 dB		
		0xA:	–53 dB	0x2A:	–21 dB		
		0xB:	–52 dB	0x2B:	–20 dB		
		0xC:	–51 dB	0x2C:	–19 dB		
		0xD:	–50 dB	0x2D:	–18 dB		
		0xE:	–49 dB	0x2E:	–17 dB		
		0xF:	–48 dB	0x2F:	–16 dB		
		0x10:	–47 dB	0x30:	–15 dB		
		0x11:	–46 dB	0x31:	–14 dB		
		0x12:	–45 dB	0x32:	–13 dB		
		0x13:	–44 dB	0x33:	–12 dB		
		0x14:	–43 dB	0x34:	–11 dB		
		0x15:	–42 dB	0x35:	–10 dB		
		0x16:	–41 dB	0x36:	–9 dB		
		0x17:	–40 dB	0x37:	–8 dB		
		0x18:	–39 dB	0x38:	–7 dB		
		0x19:	–38 dB	0x39:	–6 dB		

Bits	Field Name	Description				Type	Reset Off
		0x1A:	–37 dB	0x3A:	–5 dB		
		0x1B:	–36 dB	0x3B:	–4 dB		
		0x1C:	–35 dB	0x3C:	–3 dB		
		0x1D:	–34 dB	0x3D:	–2 dB		
		0x1E:	–33 dB	0x3E:	–1 dB		
		0x1F:	–32 dB	0x3F:	0 dB		

Table 13-24. ARXL2PGA Register

Address Offset	0x13		
Physical Address	0x0000 0013	**Instance**	AUDIO_VOICE
Description	Audio RXL2 gain control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ARXL2PGA_CGAIN		ARXL2PGA_FGAIN					

Bits	Field Name	Description				Type	Reset Off
7:6	ARXL2PGA_CGAIN	Digital coarse gain control				RW	0x0
		0x0:	0 dB				
		0x1:	6 dB				
		0x2:	12 dB				
		0x3:	12 dB				
5:0	ARXL2PGA_FGAIN	Digital fine gain control				RW	0x3F
		0x0:	Mute	0x20:	–31 dB		
		0x1:	–62 dB	0x21:	–30 dB		
		0x2:	–61 dB	0x22:	–29 dB		
		0x3:	–60 dB	0x23:	–28 dB		
		0x4:	–59 dB	0x24:	–27 dB		
		0x5:	–58 dB	0x25:	–26 dB		
		0x6:	–57 dB	0x26:	–25 dB		
		0x7:	–56 dB	0x27:	–24 dB		
		0x8:	–55 dB	0x28:	–23 dB		
		0x9:	–54 dB	0x29:	–22 dB		
		0xA:	–53 dB	0x2A:	–21 dB		
		0xB:	–52 dB	0x2B:	–20 dB		
		0xC:	–51 dB	0x2C:	–19 dB		
		0xD:	–50 dB	0x2D:	–18 dB		
		0xE:	–49 dB	0x2E:	–17 dB		
		0xF:	–48 dB	0x2F:	–16 dB		
		0x10:	–47 dB	0x30:	–15 dB		
		0x11:	–46 dB	0x31:	–14 dB		
		0x12:	–45 dB	0x32:	–13 dB		
		0x13:	–44 dB	0x33:	–12 dB		
		0x14:	–43 dB	0x34:	–11 dB		
		0x15:	–42 dB	0x35:	–10 dB		
		0x16:	–41 dB	0x36:	–9 dB		
		0x17:	–40 dB	0x37:	–8 dB		
		0x18:	–39 dB	0x38:	–7 dB		

Bits	Field Name	Description				Type	Reset Off
		0x19:	–38 dB	0x39:	–6 dB		
		0x1A:	–37 dB	0x3A:	–5 dB		
		0x1B:	–36 dB	0x3B:	–4 dB		
		0x1C:	–35 dB	0x3C:	–3 dB		
		0x1D:	–34 dB	0x3D:	–2 dB		
		0x1E:	–33 dB	0x3E:	–1 dB		
		0x1F:	–32 dB	0x3F:	0 dB		

Table 13-25. VRXPGA Register

Address Offset	0x14		
Physical Address	0x0000 0014	**Instance**	AUDIO_VOICE
Description	Voice downlink gain control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Reserved		VRXLPGA_FGAIN					

Bits	Field Name	Description				Type	Reset Off
7:6	Reserved	Other				RW	0x0
5:0	VRXPGA_GAIN	Voice RX PGA gain				RW	0x25
		0x0:	Mute	0x20:	–5 dB		
		0x1:	–36 dB	0x21:	–4 dB		
		0x2:	–35 dB	0x22:	–3 dB		
		0x3:	–34 dB	0x23:	–2 dB		
		0x4:	–33 dB	0x24:	–1 dB		
		0x5:	–32 dB	0x25:	0 dB		
		0x6:	–31 dB	0x26:	1 dB		
		0x7:	–30 dB	0x27:	2 dB		
		0x8:	–29 dB	0x28:	3 dB		
		0x9:	–28 dB	0x29:	4 dB		
		0xA:	–27 dB	0x2A:	5 dB		
		0xB:	–26 dB	0x2B:	6 dB		
		0xC:	–25 dB	0x2C:	7 dB		
		0xD:	–24 dB	0x2D:	8 dB		
		0xE:	–23 dB	0x2E:	9 dB		
		0xF:	–22 dB	0x2F:	10 dB		
		0x10:	–21 dB	0x30:	11 dB		
		0x11:	–20 dB	0x31:	12 dB		
		0x12:	–19 dB				
		0x13:	–18 dB				
		0x14:	–17 dB				
		0x15:	–16 dB				
		0x16:	–15 dB				
		0x17:	–14 dB				
		0x18:	–13 dB				
		0x19:	–12 dB				
		0x1A:	–11 dB				
		0x1B:	–10 dB				

Bits	Field Name	Description	Type	Reset Off
		0x1C: –9 dB		
		0x1D: –8 dB		
		0x1E: –7 dB		
		0x1F: –6 dB		

Table 13-26. VSTPGA Register

Address Offset	0x15		
Physical Address	0x0000 0015	**Instance**	AUDIO_VOICE
Description	Voice sidetone gain control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED		VSTPGA_GAIN					

Bits	Field Name	Description	Type	Reset Off
7:6	Reserved	Reserved	RW	0x0
5:0	VSTPGA_GAIN	Voice sidetone: Digital gain control	RW	0x00

0x0:	Mute	0x20:	–19 dB
0x1:	–50 dB	0x21:	–18 dB
0x2:	–49 dB	0x22:	–17 dB
0x3:	–48 dB	0x23:	–16 dB
0x4:	–47 dB	0x24:	–15 dB
0x5:	–46 dB	0x25:	–14 dB
0x6:	–45 dB	0x26:	–13 dB
0x7:	–44 dB	0x27:	–12 dB
0x8:	–43 dB	0x28:	–11 dB
0x9:	–42 dB	0x29:	–10 dB
0xA:	–41 dB		
0xB:	–40 dB		
0xC:	–39 dB		
0xD:	–38 dB		
0xE:	–37 dB		
0xF:	–36 dB		
0x10:	–35 dB		
0x11:	–34 dB		
0x12:	–33 dB		
0x13:	–32 dB		
0x14:	–31 dB		
0x15:	–30 dB		
0x16:	–29 dB		
0x17:	–28 dB		
0x18:	–27 dB		
0x19:	–26 dB		
0x1A:	–25 dB		
0x1B:	–24 dB		
0x1C:	–23 dB		
0x1D:	–22 dB		
0x1E:	–21 dB		

Bits	Field Name	Description	Type	Reset Off
		0x1F: –20 dB		

Table 13-27. VRX2ARXPGA Register

Address Offset	0x16		
Physical Address	0x0000 0016	**Instance**	AUDIO_VOICE
Description	Voice RX to audio RX PGA gain control. Controls the gain of the mixing of voice RX with audio RX (see Table 13-14).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED			VRX2ARXPGA_GAIN				

Bits	Field Name	Description	Type	Reset Off
7:5	Reserved	Reserved	RW	0x0
4:0	VRX2ARXPGA_GAIN	Voice RX to audio RX PGA gain	RW	0x00
		0x0: Mute		
		0x1: –24 dB		
		0x2: –23 dB		
		0x3: –22 dB		
		0x4: –21 dB		
		0x5: –20 dB		
		0x6: –19 dB		
		0x7: –18 dB		
		0x8: –17 dB		
		0x9: –16 dB		
		0xA: –15 dB		
		0xB: –14 dB		
		0xC: –13 dB		
		0xD: –12 dB		
		0xE: –11 dB		
		0xF: –10 dB		
		0x10: –9 dB		
		0x11: –8 dB		
		0x12: –7 dB		
		0x13: –6 dB		
		0x14: –5 dB		
		0x15: –4 dB		
		0x16: –3 dB		
		0x17: –2 dB		
		0x18: –1 dB		
		0x19: 0 dB		

Table 13-28. AVDAC_CTL Register

Address Offset	0x17		
Physical Address	0x0000 0017	**Instance**	AUDIO_VOICE
Description	Power control register for audio DAC and voice DAC If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ is powered off, the digital filter, analog section, and Bluetooth/voice/ audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED			VDAC_EN	ADACL2_EN	ADACR2_EN	ADACL1_EN	ADACR1_EN

Bits	Field Name	Description	Type	Reset Off
7:5	Reserved	Reserved	RW	0x0
4	VDAC_EN	Voice DAC power control 0x0: Disabled 0x1: Enabled	RW	0
3	ADACL2_EN	Audio DACL2 power control 0x0: Disabled 0x1: Enabled	RW	0
2	ADACR2_EN	Audio DACR2 power control 0x0: Disabled 0x1: Enabled	RW	0
1	ADACL1_EN	Audio DACL1 power control 0x0: Disabled 0x1: Enabled	RW	0
0	ADACR1_EN	Audio DACR1 power control 0x0: Disabled 0x1: Enabled	RW	0

Table 13-29. ARX2VTXPGA Register

Address Offset	0x18		
Physical Address	0x0000 0018	**Instance**	AUDIO_VOICE
Description	Audio RX to voice TX PGA gain control. Controls the gain of the mixing of audio RX with voice TX (see Table 13-14).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED		ARX2VTXPGA_GAIN					

Bits	Field Name	Description	Type	Reset Off
7:6	Reserved	Reserved	RW	0x0
5:0	ARX2VTXPGA_GAIN	Digital gain control 0x0: Mute 0x1: –62 dB 0x2: –61 dB 0x3: –60 dB 0x4: –59 dB 0x20: –31 dB 0x21: –30 dB 0x22: –29 dB 0x23: –28 dB 0x24: –27 dB	RW	0x00

Bits	Field Name	Description				Type	Reset Off
		0x5:	–58 dB	0x25:	–26 dB		
		0x6:	–57 dB	0x26:	–25 dB		
		0x7:	–56 dB	0x27:	–24 dB		
		0x8:	–55 dB	0x28:	–23 dB		
		0x9:	–54 dB	0x29:	–22 dB		
		0xA:	–53 dB	0x2A:	–21 dB		
		0xB:	–52 dB	0x2B:	–20 dB		
		0xC:	–51 dB	0x2C:	–19 dB		
		0xD:	–50 dB	0x2D:	–18 dB		
		0xE:	–49 dB	0x2E:	–17 dB		
		0xF:	–48 dB	0x2F:	–16 dB		
		0x10:	–47 dB	0x30:	–15 dB		
		0x11:	–46 dB	0x31:	–14 dB		
		0x12:	–45 dB	0x32:	–13 dB		
		0x13:	–44 dB	0x33:	–12 dB		
		0x14:	–43 dB	0x34:	–11 dB		
		0x15:	–42 dB	0x35:	–10 dB		
		0x16:	–41 dB	0x36:	–9 dB		
		0x17:	–40 dB	0x37:	–8 dB		
		0x18:	–39 dB	0x38:	–7 dB		
		0x19:	–38 dB	0x39:	–6 dB		
		0x1A:	–37 dB	0x3A:	–5 dB		
		0x1B:	–36 dB	0x3B:	–4 dB		
		0x1C:	–35 dB	0x3C:	–3 dB		
		0x1D:	–34 dB	0x3D:	–2 dB		
		0x1E:	–33 dB	0x3E:	–1 dB		
		0x1F:	–32 dB	0x3F:	0 dB		

Table 13-30. ARXL1_APGA_CTL Register

Address Offset	0x19		
Physical Address	0x0000 0019	**Instance**	AUDIO_VOICE
Description	Audio RXL1 analog PGA control register If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ is powered off, the digital filter, analog section, and Bluetooth/voice/ audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ARXL1_GAIN_SET					ARXL1_FM_EN	ARXL1_DA_EN	ARXL1_PDZ

Bits	Field Name	Description		Type	Reset Off
7:3	ARXL1_GAIN_SET	Analog programmable gain control Mute mode can be performed by disabling all input channels.		RW	0x06
		0x0:	12 dB		
		0x1:	10 dB		
		0x2:	8 dB		
		0x3:	6 dB		
		0x4:	4 dB		
		0x5:	2 dB		

Bits	Field Name	Description	Type	Reset Off
		0x6: 0 dB		
		0x7: –2 dB		
		0x8: –4 dB		
		0x9: –6 dB		
		0xA: –8 dB		
		0xB: –10 dB		
		0xC: –12 dB		
		0xD: –14 dB		
		0xE: –16 dB		
		0xF: –18 dB		
2	ARXL1_FM_EN	FM loop path enable control bit	RW	0
		0x0: Disabled		
		0x1: Enabled		
1	ARXL1_DA_EN	Digital-to-analog path enable control bit	RW	1
		0x0: Disabled		
		0x1: Enabled		
0	ARXL1_PDZ	Analog PGA power control bit	RW	0
		0x0: Power-down mode		
		0x1: Application mode		

Table 13-31. ARXR1_APGA_CTL Register

Address Offset	0x1A		
Physical Address	0x0000 001A	**Instance**	AUDIO_VOICE
Description	Audio RXR1 analog PGA control register. If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ is powered off, the digital filter, analog section, and Bluetooth/voice/ audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ARXR1_GAIN_SET					ARXR1_FM_EN	ARXR1_DA_EN	ARXR1_PDZ

Bits	Field Name	Description	Type	Reset Off
7:3	ARXR1_GAIN_SET	Analog programmable gain control Mute mode can be performed by disabling all input channels.	RW	0x06
		0x0: 12 dB		
		0x1: 10 dB		
		0x2: 8 dB		
		0x3: 6 dB		
		0x4: 4 dB		
		0x5: 2 dB		
		0x6: 0 dB		
		0x7: –2 dB		
		0x8: –4 dB		
		0x9: –6 dB		

Bits	Field Name	Description	Type	Reset Off
		0xA: –8 dB		
		0xB: –10 dB		
		0xC: –12 dB		
		0xD: –14 dB		
		0xE: –16 dB		
		0xF: –18 dB		
		0x10: –20 dB		
		0x11: –22 dB		
		0x12: –24 dB		
2	ARXR1_FM_EN	FM loop path enable control bit	RW	0
		0x0: Disabled		
		0x1: Enabled		
1	ARXR1_DA_EN	Digital-to-analog path enable control bit	RW	1
		0x0: Disabled		
		0x1: Enabled		
0	ARXR1_PDZ	Analog PGA power control bit	RW	0
		0x0: Power-down mode		
		0x1: Application mode		

Table 13-32. ARXL2_APGA_CTL Register

Address Offset	0x1B		
Physical Address	0x0000 001B	**Instance**	AUDIO_VOICE
Description	Audio RXL2 analog PGA control register If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ is powered off, the digital filter, analog section, and Bluetooth/voice/ audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ARXL2_GAIN_SET					ARXL2_FM_EN	ARXL2_DA_EN	ARXL2_PDZ

Bits	Field Name	Description	Type	Reset Off
7:3	ARXL2_GAIN_SET	Analog programmable gain control Mute mode can be performed by disabling all input channels.	RW	0x06
		0x0: 12 dB		
		0x1: 10 dB		
		0x2: 8 dB		
		0x3: 6 dB		
		0x4: 4 dB		
		0x5: 2 dB		
		0x6: 0 dB		
		0x7: –2 dB		
		0x8: –4 dB		
		0x9: –6 dB		
		0xA: –8 dB		
		0xB: –10 dB		
		0xC: –12 dB		
		0xD: –14 dB		
		0xE: –16 dB		

Bits	Field Name	Description	Type	Reset Off
		0xF: –18 dB 0x10 –20 dB : 0x11 –22 dB : 0x12 –24 dB :		
2	ARXL2_FM_EN	FM loop path enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1	ARXL2_DA_EN	Digital-to-analog path enable control bit 0x0: Disabled 0x1: Enabled	RW	1
0	ARXL2_PDZ	Analog PGA power control bit 0x0: Power-down mode 0x1: Application mode	RW	0

Table 13-33. ARXR2_APGA_CTL Register

Address Offset	0x1C		
Physical Address	0x0000 001C	**Instance**	AUDIO_VOICE
Description	Audio RXR2 analog PGA control register If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ is powered off, the digital filter, analog section, and Bluetooth/voice/ audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
ARXR2_GAIN_SET					ARXR2_FM_EN	ARXR2_DA_EN	ARXR2_PDZ

Bits	Field Name	Description	Type	Reset Off
7:3	ARXR2_GAIN_SET	Analog programmable gain control Mute mode can be performed by disabling all input channels. 0x0: 12 dB 0x1: 10 dB 0x2: 8 dB 0x3: 6 dB 0x4: 4 dB 0x5: 2 dB 0x6: 0 dB 0x7: –2 dB 0x8: –4 dB 0x9: –6 dB 0xA: –8 dB 0xB: –10 dB 0xC: –12 dB 0xD: –14 dB	RW	0x06

Bits	Field Name	Description	Type	Reset Off
		0xE: –16 dB 0xF: –18 dB 0x10 : –20 dB 0x11 : –22 dB 0x12 : –24 dB		
2	ARXR2_FM_EN	FM loop path enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1	ARXR2_DA_EN	Digital-to-analog path enable control bit 0x0: Disabled 0x1: Enabled	RW	1
0	ARXR2_PDZ	Analog PGA power control bit 0x0: Power-down mode 0x1: Application mode	RW	0

Table 13-34. ATX2ARXPGA Register

Address Offset	0x1D		
Physical Address	0x0000 001D	**Instance**	AUDIO_SCAUDIO_VOICE
Description	Audio TX to audio RX PGA digital gain control		
Write Latency			
Type	RW		

7	6	5	4	3	2	1	0
RESERVED		ATX2ARXL_PGA			ATX2ARXR_PGA		

Bits	Field Name	Description	Type	Reset Off
7:6	Reserved	Reserved	RW	0x0
5:3	ATX2ARXL_PGA	Loop TX to RX digital gain control (left) 0x0: Mute 0x1: –24 dB 0x2: –24 dB 0x3: –24 dB 0x4: –18 dB 0x5: –12 dB 0x6: –6 dB 0x7: 0 dB	RW	0x0
2:0	ATX2ARXR_PGA	Loop TX to RX digital gain control (right) 0x0: Mute 0x1: –24 dB 0x2: –24 dB 0x3: –24 dB 0x4: –18 dB 0x5: –12 dB 0x6: –6 dB 0x7: 0 dB	RW	0x0

Table 13-35. BT_IF Register

Address Offset	0x1E		
Physical Address	0x0000 001E	**Instance**	AUDIO_VOICE
Description	Control mode for Bluetooth interface **Note:** The data format of the Bluetooth interface is defined by voice interface (VOICE_IF register at address 0x0F, VIF_FORMAT bit, see Table 13-20). If the codec powers control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SPARE	BT_DIN_EN	BT_DOUT_EN	BT_SWAP	RESERVED	BT_TRI_EN	RESERVED	BT_EN

Bits	Field Name	Description	Type	Reset Off
7	SPARE	Spare bit	RW	0
6	BT_DIN_EN	Enable Bluetooth input. 0x0: Off mode BTDIN = L 0x1: Application mode	RW	0
5	BT_DOUT_EN	Enable Bluetooth output. 0x0: Off mode BT_PCM_VDX = L 0x1: Application mode	RW	0
4	BT_SWAP	Control to swap bt_pcm_vdr/bt_pcm_vdx 0x0: I/O not swapped 0x1: I/O swapped	RW	0
3	Reserved		RW	0
2	BT_TRI_EN	Put the Bluetooth interface output pins (BT_PCM_VDR and BT_PCM_VDX) in high impedance. PCM_VCK and PCM_VFS in high impedance if BT_TRI_EN = 1 and VIF_TRI_EN = 1 (VIF_TRI_EN bit defined in VOICE_IF register, see Table 13-20). 0x0: Application mode 0x1: High impedance	RW	0
1	Reserved		RW	0
0	BT_EN	Bluetooth and voice interface power control PCM_VCK and PCM_VFS in low state (L) if VIF_EN = 0 and BT_EN = 0 (VIF_EN bit defined in VOICE_IF register, see Table 13-20). 0x0: Mode BTDIN/BTDOUT = L 0x1: Application mode	RW	0

Table 13-36. BTPGA Register

Address Offset	0x1F		
Physical Address	0x0000 001F	**Instance**	AUDIO_VOICE
Description	Bluetooth path digital gain control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
BTTXPGA_GAI				BTRXPGA_GAIN			

Bits	Field Name	Description	Type	Reset Off
7:4	BTTXPGA_GAIN	Bluetooth TX path: Digital gain control	RW	0x5
		0x0: –15 dB		
		0x1: –12 dB		
		0x2: –9 dB		
		0x3: –6 dB		
		0x4: –3 dB		
		0x5: 0 dB		
		0x6: 3 dB		
		0x7: 6 dB		
		0x8: 9 dB		
		0x9: 12 dB		
		0xA: 15 dB		
		0xB: 18 dB		
		0xC: 21 dB		
		0xD: 24 dB		
		0xE: 27 dB		
		0xF: 30 dB		
3:0	BTRXPGA_GAIN	Bluetooth RX path: Digital gain control	RW	0x5
		0x0: –30 dB		
		0x1: –27 dB		
		0x2: –24 dB		
		0x3: –21 dB		
		0x4: –18 dB		
		0x5: –15 dB		
		0x6: –12 dB		
		0x7: –9 dB		
		0x8: –6 dB		
		0x9: –3 dB		
		0xA: 0 dB		
		0xB: 3 dB		
		0xC: 6 dB		
		0xD: 9 dB		
		0xE: 12 dB		
		0xF: 15 dB		

Table 13-37. BTSTPGA Register

Address Offset	0x20		
Physical Address	0x0000 0020	**Instance**	AUDIO_VOICE
Description	Bluetooth sidetone gain control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED		BTXTPGA_GAIN					

Bits	Field Name	Description				Type	Reset Off
7:6	Reserved	Reserved				RW	0x0
5:0	BTSTPGA_GAIN	Bluetooth sidetone: Digital gain control				RW	0x00
		0x0:	Mute	0x19:	–26 dB		
		0x1:	–50 dB	0x1A:	–25 dB		
		0x2:	–49 dB	0x1B:	–24 dB		
		0x3:	–48 dB	0x1C:	–23 dB		
		0x4:	–47 dB	0x1D:	–22 dB		
		0x5:	–46 dB	0x1E:	–21 dB		
		0x6:	–45 dB	0x1F:	–20 dB		
		0x7:	–44 dB	0x20:	–19 dB		
		0x8:	–43 dB	0x21:	–18 dB		
		0x9:	–42 dB	0x22:	–17 dB		
		0xA:	–41 dB	0x23:	–16 dB		
		0xB:	–40 dB	0x24:	–15 dB		
		0xC:	–39 dB	0x25:	–14 dB		
		0xD:	–38 dB	0x26:	–13 dB		
		0xE:	–37 dB	0x27:	–12 dB		
		0xF:	–36 dB	0x28:	–11 dB		
		0x10:	–35 dB	0x29:	–10 dB		
		0x11:	–34 dB				
		0x12:	–33 dB				
		0x13:	–32 dB				
		0x14:	–31 dB				
		0x15:	–30 dB				
		0x16:	–29 dB				
		0x17:	–28 dB				
		0x18:	–27 dB				

Table 13-38. EAR_CTL Register

Address Offset	0x21		
Physical Address	0x0000 0021	**Instance**	AUDIO_VOICE
Description	Earphone amplifier control register Voice A →IN1, Audio L1 → IN2, Audio L2 → IN3, Audio R1 → IN4 If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting. Earphone output (EAR): Voice, audio L1, audio L2, or audio R1 can be routed to the output separately (only one enable bit at 1); or voice can be mixed with audio R1, audio L1, or audio L2 and routed to the output (EAR_VOICE_EN = 1, EAR_AR1_EN = 1, EAR_AL1_EN = 1, or EAR_AL2_EN = 1).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
EAR_OUTLOW_EN	SPARE	EAR_GAIN		EAR_AR1_EN	EAR_AL2_EN	EAR_AL1_EN	EAR_VOICE_EN

Bits	Field Name	Description	Type	Reset Off
7	EAR_OUTLOW_EN	Output low-level control bit 0x0: Disabled 0x1: Enabled (Output = L)	RW	0
6	SPARE	Spare bit	RW	0
5:4	EAR_GAIN	Amplifier gain control 0x0: Power-down mode 0x1: 12 dB 0x2: 6 dB 0x3: 0 dB	RW	0x0
3	EAR_AR1_EN	Audio R1 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
2	EAR_AL2_EN	Audio L2 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1	EAR_AL1_EN	Audio L1 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
0	EAR_VOICE_EN	Voice enable control bit 0x0: Disabled 0x1: Enabled	RW	0

Table 13-39. HS_SEL Register

Address Offset	0x22		
Physical Address	0x0000 0022	**Instance**	AUDIO_VOICE
Description	Headset left and right amplifier control register Voice A → IN1, Audio L/R1 → IN2, Audio L/R2 → IN3 If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/voice/audio interfaces are switched off, regardless of this register setting. Headset output right (HSOR): Voice, audio R1, or audio R2 can be routed to the output separately (only one enable bit at 1); or voice can be mixed with audio R1 or audio R2 and routed to the output (HSOR_VOICE_EN = 1, HSOR_AR1_EN = 1, or HSOR_AR2_EN = 1). Headset output left (HSOL): Voice, audio L1, or audio L2 can be routed to the output separately (only one enable bit at 1); or voice can be mixed with audio L1 or audio L2 and routed to the output (HSOL_VOICE_EN = 1, HSOL_AL1_EN = 1, or HSOL_AL2_EN = 1).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
HSR_INV_EN	HS_OUTLOW_EN	HSOR_AR2_EN	HSOR_AR1_EN	HSOR_VOICE_EN	HSOL_AL2_EN	HSOL_AL1_EN	HSOL_VOICE_EN

Bits	Field Name	Description	Type	Reset Off
7	HSR_INV_EN	Invert HSOR signals 0x0: Disabled 0x1: Enabled	RW	0
6	HS_OUTLOW_EN	Outputs low-level control bit 0x0: Disabled 0x1: Amplifier output is in low state	RW	0
5	HSOR_AR2_EN	HSOR: Audio R2 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
4	HSOR_AR1_EN	HSOR: Audio R1 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
3	HSOR_VOICE_EN	HSOR: Voice enable control bit 0x0: Disabled 0x1: Enabled	RW	0
2	HSOL_AL2_EN	HSOL: Audio L2 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1	HSOL_AL1_EN	HSOL: Audio L1 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
0	HSOL_VOICE_EN	HSOL: Voice enable control bit 0x0: Disabled 0x1: Enabled	RW	0

Table 13-40. HS_GAIN_SET Register

Address Offset	0x23		
Physical Address	0x0000 0023	**Instance**	AUDIO_VOICE
Description	Headset left/right amplifier gain setting register If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED	SPARE	RESERVED		HSR_GAIN		HSL_GAIN	

Bits	Field Name	Description	Type	Reset Off
7	Reserved		RW	0
6	SPARE	Spare bit	RW	0
5:4	Reserved		RW	0x0
3:2	HSR_GAIN	Amplifier right gain control. Mute can be performed by disabling all input channels (see Table 13-39). 0x0: Power-down mode 0x1: 6 dB 0x2: 0 dB 0x3: –6 dB	RW	0x0
1:0	HSL_GAIN	Amplifier left gain control. Mute can be performed by disabling all input channels (see Table 13-39). 0x0: Power-down mode 0x1: 6 dB 0x2: 0 dB 0x3: –6 dB	RW	0x0

Table 13-41. HS_POPN_SET Register

Address Offset	0x24		
Physical Address	0x0000 0024	**Instance**	AUDIO_VOICE
Description	Headset left/right amplifier pop-noise attenuation setting register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED	VMID_EN	EXTMUTE	RAMP_DELAY			RAMP_EN	RESERVED

Bits	Field Name	Description	Type	Reset Off
7	Reserved		RW	0
6	VMID_EN	VMID buffer enable control 0x0: Disabled 0x1: Enabled	RW	0
5	EXTMUTE	Mute control (external FET) 0x0: Mute off 0x1: Mute on	RW	0
4:2	RAMP_DELAY	Ramp time control word 0x0: 2^19/f(MCLK)	RW	0x0

Bits	Field Name	Description	Type	Reset Off
		* f(MCLK) = 19.2 MHz → delay = 27 ms * f(MCLK) = 26 MHz → delay = 20 ms * f(MCLK) = 38.4 MHz → delay = 14 ms 0x1: 2^20/f(MCLK) * f(MCLK) = 19.2 MHz → delay = 55 ms * f(MCLK) = 26 MHz → delay = 40 ms * f(MCLK) = 38.4 MHz → delay = 27 ms 0x2: 2^21/f(MCLK) * f(MCLK) = 19.2 MHz → delay = 109 ms * f(MCLK) = 26 MHz → delay = 81 ms * f(MCLK) = 38.4 MHz → delay = 55 ms 0x3: 2^22/f(MCLK) * f(MCLK) = 19.2 MHz → delay = 218 ms * f(MCLK) = 26 MHz → delay = 161 ms * f(MCLK) = 38.4 MHz → delay = 109 ms 0x4: 2^23/f(MCLK) * f(MCLK) = 19.2 MHz → delay = 437 ms * f(MCLK) = 26 MHz → delay = 323 ms * f(MCLK) = 38.4 MHz → delay = 218 ms 0x5: 2^24/f(MCLK) * f(MCLK) = 19.2 MHz → delay = 874 ms * f(MCLK) = 26 MHz → delay = 645 ms * f(MCLK) = 38.4 MHz → delay = 437 ms 0x6: 2^25/f(MCLK) * f(MCLK) = 19.2 MHz → delay = 1748 ms * f(MCLK) = 26 MHz → delay = 1291 ms * f(MCLK) = 38.4 MHz => delay = 874 ms 0x7: 2^26/f(MCLK) * f(MCLK) = 19.2 MHz → delay = 3495 ms * f(MCLK) = 26 MHz → delay = 2581 ms * f(MCLK) = 38.4 MHz → delay = 1748 ms		
1	RAMP_EN	Ramp generator control bit for pop-noise attenuation. The ramp time is defined by word RAMP_DELAY. 0x0: Ramp down (from hso_vmid value to 0) 0x1: Ramp up (from zero to hso_vmid)	RW	0
0	Reserved		RW	0

Table 13-42. PREDL_CTL Register

Address Offset	0x25		
Physical Address	0x0000 0025	**Instance**	AUDIO_VOICE
Description	Predriver class D left amplifier control register Voice A −> IN1, Audio L1 −> IN2, Audio L2 −> IN3, Audio R2 −> IN4 If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting. Predriver class D output left (PREDL): Voice, audio L1, audio L2, or audio R2 can be routed to the output separately (only one enable bit at 1); or voice can be mixed with audio L1, audio L2, or audio R2 and routed to the output (PREDL_VOICE_EN = 1, PREDL_AL1_EN = 1, PREDL_AL2_EN = 1, or PREDL_AR2_EN = 1, respectively).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
PREDL_OUTLOW_EN	RESERVED	PREDL_GAIN		PREDL_AR2_EN	PREDL_AL2_EN	PREDL_AL1_EN	PREDL_VOICE_EN

Bits	Field Name	Description	Type	Reset Off
7	PREDL_OUTLOW_EN	Output low-level control bit 0x0: Disabled 0x1: Enabled (Output = L)	RW	0
6	Reserved		RW	0
5:4	PREDL_GAIN	Amplifier gain control. Mute can be performed by disabling all input channels. 0x0: Power-down mode 0x1: 6 dB 0x2: 0 dB 0x3: –6 dB	RW	0x0
3	PREDL_AR2_EN	Audio R2 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
2	PREDL_AL2_EN	Audio L2 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1	PREDL_AL1_EN	Audio L1 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
0	PREDL_VOICE_EN	Voice enable control bit 0x0: Disabled 0x1: Enabled	RW	0

Table 13-43. PREDR_CTL Register

Address Offset	0x26		
Physical Address	0x0000 0026	**Instance**	AUDIO_VOICE
Description	Predriver class D left amplifier control register Voice A −> IN1, Audio R1 −> IN2, Audio R2 −> IN3, Audio L2 −> IN4 If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/voice/audio interfaces are switched off, regardless of this register setting. Predriver class D output right (PREDR): Voice, audio R1, audio R2, or audio L2 can be routed to the output separately (only one enable bit at 1); or voice can be mixed with audio R1, audio R2, or audio L2 and routed to the output (PREDR_VOICE_EN = 1, PREDR_AR1_EN = 1, PREDR_AR2_EN = 1, or PREDR_AL2_EN = 1).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
PREDR_OUTLOW_EN	RESERVED	PREDR_GAINPREDR_GAIN		PREDR_AL2_EN	PREDR_AR2_EN	PREDR_AR1_EN	PREDR_VOICE_EN

Bits	Field Name	Description	Type	Reset Off
7	PREDR_OUTLOW_EN	Output low-level control bit 0x0: Disabled 0x1: Enabled (Output = L)	RW	0
6	Reserved		RW	0
5:4	PREDR_GAIN	Amplifier gain control. Mute can be performed by disabling all input channels. 0x0: Power-down mode 0x1: 6 dB 0x2: 0 dB 0x3: –6 dB	RW	0x0
3	PREDR_AL2_EN	Audio L2 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
2	PREDR_AR2_EN	Audio R2 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1	PREDR_AR1_EN	Audio R1 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
0	PREDR_VOICE_EN	Voice enable control bit 0x0: Disabled 0x1: Enabled	RW	0

Table 13-44. PRECKL_CTL Register

Address Offset	0x27		
Physical Address	0x0000 0027	**Instance**	AUDIO_VOICE
Description	Preamplifier carkit left control register Voice A −> IN1, Audio L1 −> IN2, Audio L2 −> IN3 If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/voice/audio interfaces are switched off, regardless of this register setting. Predriver carkit output left (PRECKL): Voice, audio L1, or audio L2 can be routed to the output separately (only one enable bit at 1); or voice can be mixed with audio L1 or audio L2 and routed to the output (PRECKL_VOICE_EN = 1, PRECKL_AL1_EN = 1, or PRECKL_AL2_EN = 1).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED	PRECKL_EN	PRECKL_GAIN		RESERVED	PRECKL_AL2_EN	PRECKL_AL1_EN	PRECKL_VOICE_EN

Bits	Field Name	Description	Type	Reset Off
7	Reserved		RW	0
6	PRECKL_EN	Preamplifier left carkit enable control bit 0x0: Disabled 0x1: Enabled	RW	0
5:4	PRECKL_GAIN	Gain control. Mute can be performed by disabling all input channels. 0x0: Power-down mode 0x1: 6 dB 0x2: 0 dB 0x3: –6 dB	RW	0x0
3	Reserved		RW	0
2	PRECKL_AL2_EN	Audio L2 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1	PRECKL_AL1_EN	Audio L1 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
0	PRECKL_VOICE_EN	Voice enable control bit 0x0: Disabled 0x1: Enabled	RW	0

Table 13-45. PRECKR_CTL Register

Address Offset	0x28		
Physical Address	0x0000 0028	**Instance**	AUDIO_VOICE
Description	Preamplifier carkit right control register Voice A −> IN1, Audio R1 −> IN2, Audio R2 −> IN3. If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting. Predriver carkit output right (PRECKR): Voice, audio R1, or audio R2 can be routed to the output separately (only one enable bit at 1); or voice can be mixed with audio R1 or audio R2 and routed to the output (PRECKR_VOICE_EN = 1, PRECKR_AR1_EN = 1, or PRECKR_AR2_EN = 1).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED	PRECKR_EN	PRECKR_GAIN		RESERVED	PRECKR_AR2_EN	PRECKR_AR1_EN	PRECKR_VOICE_EN

Bits	Field Name	Description	Type	Reset Off
7	Reserved		RW	0
6	PRECKR_EN	Preamplifier right carkit enable control bit 0x0: Disabled 0x1: Enabled	RW	0
5:4	PRECKR_GAIN	Gain control. Mute can be performed by disabling all input channels. 0x0: Power-down mode 0x1: 6 dB 0x2: 0 dB 0x3: –6 dB	RW	0x0
3	Reserved		RW	0
2	PRECKR_AR2_EN	Audio R2 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1	PRECKR_AR1_EN	Audio R1 enable control bit 0x0: Disabled 0x1: Enabled	RW	0
0	PRECKR_VOICE_EN	Voice enable control bit 0x0: Disabled 0x1: Enabled	RW	0

Table 13-46. HFL_CTL Register

Address Offset	0x29		
Physical Address	0x0000 0029	**Instance**	AUDIO_VOICE
Description	Hands-free left class D amplifier control register If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting. The class D amplifier is in application mode if all EN bits are in high state.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED		HFL_REF_EN	HFL_RAMP_EN	HFL_LOOP_EN	HFL_HB_EN	HFL_INPUT_SEL	

Bits	Field Name	Description	Type	Reset Off
7:6	Reserved		RW	0x0
5	HFL_REF_EN	Ref enable control bit 0x0: Disabled 0x1: Enabled	RW	0
4	HFL_RAMP_EN	Ramp enable control bit 0x0: Disabled 0x1: Enabled	RW	0
3	HFL_LOOP_EN	Loop enable control bit 0x0: Disabled 0x1: Enabled	RW	0
2	HFL_HB_EN	H-bridge enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1:0	HFL_INPUT_SEL	Input select for hands-free amplifier control word 0x0: Voice input 0x1: Audio left channel 1 input 0x2: Audio left channel 2input 0x3: Audio right channel 2 input	RW	0x0

Table 13-47. HFR_CTL Register

Address Offset	0x2A		
Physical Address	0x0000 002A	**Instance**	AUDIO_VOICE
Description	Hands-free right class D amplifier control register. If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ setting is powered off, the digital filter, analog section, and Bluetooth/ voice/audio interfaces are switched off, regardless of this register setting. The class D amplifier is in application mode if all EN bits are in high state.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED		HFR_REF_EN	HFR_RAMP_EN	HFR_LOOP_EN	HFR_HB_EN	HFR_INPUT_SEL	

Bits	Field Name	Description	Type	Reset Off
7:6	Reserved		RW	0x0
5		Ref enable control bit 0x0: Disabled 0x1: Enabled	RW	0
4	HFR_RAMP_EN	Ramp enable control bit 0x0: Disabled 0x1: Enabled	RW	0x0
3	HFR_LOOP_EN	Loop enable control bit 0x0: Disabled 0x1: Enabled	RW	0
2	HFR_HB_EN	H-bridge enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1:0	HFR_INPUT_SEL	Input select for hands-free amplifier control word 0x0: Voice input 0x1: Audio right channel 1 input 0x2: Audio right channel 2input 0x3: Audio left channel 2 input	RW	0x0

Table 13-48. ALC_CTL Register

Address Offset	0x2B		
Physical Address	0x0000 002B	**Instance**	AUDIO_VOICE
Description	ALC control If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ is powered off, the digital filter, analog section, and Bluetooth/voice/ audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SPARE2	SPARE1	ALC_MODE	SUBMIC_ALC_EN	MAINMIC_ALC_EN	ALC_WAIT		

Bits	Field Name	Description	Type	Reset Off
7	SPARE2	Spare bit 2	RW	0
6	SPARE1	Spare bit 1	RW	0
5	ALC_MODE	ALC mode control 0x0: Normal 0x1: Interlock	RW	0
4	SUBMIC_ALC_EN	SUBMIC ALC power control 0x0: Off 0x1: On	RW	0
3	MAINMIC_ALC_EN	Main microphone ALC control	RW	0
2:0	ALC_WAIT	Wait time control 0x0: 1 * WaitToRelease 0x1: 2 * WaitToRelease 0x2: 4 * WaitToRelease 0x3: 8 * WaitToRelease 0x4: 16 * WaitToRelease 0x5: 32 * WaitToRelease 0x6: 64 * WaitToRelease 0x7: 128 * WaitToRelease	RW	0x5

Table 13-49. ALC_SET1 Register

Address Offset	0x2C		
Physical Address	0x0000 002C	**Instance**	AUDIO_VOICE
Description	ALC high and low threshold controls Some restrictions on the combinations of setting: • ALC_MAX_LIMIT − ALC_MIN_LIMIT must be more than 2*ALC_STEP. • ALC_MAX_LIMIT > ALC_MIN_LIMIT		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED		ALC_MAX_LIMIT			ALC_MIN_LIMIT		

Bits	Field Name	Description	Type	Reset Off
7:6	Reserved	Reserved	RW	0x0
5:3	ALC_MAX_LIMIT	ALC high threshold control 0x0: –9 dB 0x1: –12 dB 0x2: –15 dB 0x3: –18 dB 0x4: –21 dB 0x5: –24 dB 0x6: –27 dB 0x7: –27 dB	RW	0x0
2:0	ALC_MIN_LIMIT	ALC low threshold control 0x0: –12 dB 0x1: –15 dB 0x2: –18 dB 0x3: –21 dB 0x4: –24 dB 0x5: –27 dB 0x6: –30 dB 0x7: –30 dB	RW	0x0

Table 13-50. ALC_SET2 Register

Address Offset	0x2D		
Physical Address	0x0000 002D	**Instance**	AUDIO_VOICE
Description	ALC release/attack time control		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED	ALC_STEP	ALC_ATTACK			ALC_RELEASE		

Bits	Field Name	Description	Type	Reset Off
7	Reserved		RW	0
6	ALC_STEP		RW	0
		0x0: 1 dB		
		0x1: 2 dB		

Bits	Field Name	Description	Type	Reset Off
5:3	ALC_ATTACK	ALC attack time control. ALC attack time defines the minimum time between two steps of decreasing gain. 0x0: 1 * 6.25 µs 0x1: 2 * 6.25 = 12.5 µs 0x2: 4 * 6.25 25 µs 0x3: 8 * 6.25 - 50 µs 0x4: 100 µs 0x5: 200 µs 0x6: 400 µs 0x7: 800 µs	RW	0x0
2:0	ALC_RELEASE	ALC release time control. ALC release time defines the minimum time between two steps of increasing gain. 0x0: 1.6 ms 0x1: 3.2 ms 0x2: 6.4 ms 0x3: 12.8 ms 0x4: 25.6 ms 0x5: 51.2 ms 0x6: 1.6 ms 0x7: 1.6 ms	RW	0x0

Table 13-51. BOOST_CTL Register

Address Offset	0x2E		
Physical Address	0x0000 002E	**Instance**	AUDIO_VOICE
Description	Control equalizer function		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED						EFFECT	

Bits	Field Name	Description	Type	Reset Off
7:2	Reserved	Reserved	RW	0x00
1:0	EFFECT	Boost effect adds emphasis to low frequencies to compensate the high-pass filter created by the RC filter of the headset in the AC coupling configuration. Four modes define the equalization profile. Three modes have slightly different frequency responses; the fourth mode disables the boost effect. 0x0: No effect 0x1: Boost 1 mode 0x2: Boost 2 mode 0x3: Boost 3 mode **Note:** The difference between the three boost modes is the frequency response, which is defined by the frequency response versus the input frequency and Fs frequency (see Section 6.1.10, *Boost Stage*, in the Triton2 Data Manual).	RW	0x0

Table 13-52. SOFTVOL_CTL Register

Address Offset	0x2F		
Physical Address	0x0000 002F	**Instance**	AUDIO_VOICE
Description	Soft volume control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SOFTVOL_SET			RESERVED				SOFTVOL_EN

Bits	Field Name	Description	Type	Reset Off
7:5	SOFTVOL_SET	Soft volume sweep time control 0x0: 1024 * 0.8/Fs 0x1: 512 * 0.8/Fs 0x2: 256 * 0.8/Fs 0x3: 128 * 0.8/Fs 0x4; 64 * 0.8/Fs 0x5: 16 * 0.8/Fs 0x6: 4 * 0.8/Fs 0x7: 1 * 0.8/Fs	RW	0x0
4:1	Reserved	Reserved	RW	0x0
0	SOFTVOL_EN	Bypass soft volume control 0x0: Bypass mode 0x1: Application mode	RW	0

Table 13-53. DTMF_FREQSEL Register

Address Offset	0x30		
Physical Address	0x0000 0030	**Instance**	AUDIO_VOICE
Description	Tone frequency control • Controls the frequency of Tone 1 and Tone 2 • When selecting extended tone, frequency selected by extended tone frequency registers (see Table 13-54, Table 13-55, Table 13-56, and Table 13-57).		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SPARE2	SPARE1	RESERVED	FREQSEL				

Bits	Field Name	Description	Type	Reset Off
7	SPARE2	Spare bit 2	RW	0
6	SPARE1	Spare bit 1	RW	0
5	Reserved	Reserved	RW	0
4:0	FREQSEL	Tone frequency control 0x0: 1: Tone 1 = 1209 Hz, Tone 2 = 697 Hz 0x1: 2: Tone 1 = 1336 Hz, Tone 2 = 697 Hz 0x2: 3: Tone 1 = 1477 Hz, Tone 2 = 697 Hz 0x3: A: Tone 1 = 1633 Hz, Tone 2 = 697 Hz 0x4; 4: Tone 1 = 1209 Hz, Tone 2 = 770 Hz 0x5: 5: Tone 1 = 1336 Hz, Tone 2 = 770 Hz 0x6: 6: Tone 1 = 1477 Hz, Tone 2 = 770 Hz	RW	0x13

Bits	Field Name	Description	Type	Reset Off
		0x7: B: Tone 1 = 1633 Hz, Tone 2 = 770 Hz 0x8: 7: Tone 1 = 1209 Hz, Tone 2 = 852 Hz 0x9: 8: Tone 1 = 1336 Hz, Tone 2 = 852 Hz 0xA: 9: Tone 1 = 1477 Hz, Tone 2 = 852 Hz 0xB: C: Tone 1 = 1633 Hz, Tone 2 = 852 Hz 0xC: *: Tone 1 = 1209 Hz, Tone 2 = 941 Hz 0xD: 0: Tone 1 = 1336 Hz, Tone 2 = 941 Hz 0xE: #: Tone 1 = 1477 Hz, Tone 2 = 941 Hz 0xF: D: Tone 1 = 1633 Hz, Tone 2 = 941 Hz 0x10 Single Tone 1 = 400 Hz : 0x11 Single Tone 1 = 425 Hz : 0x12 Single Tone 1 = 2 kHz : 0x13 Single Tone 1 = 2.67 kHz : 0x14 Tone 1: extended, Tone 2: extended :		

Table 13-54. DTMF_TONEXT1H Register

Address Offset	0x31		
Physical Address	0x0000 0031	**Instance**	AUDIO_VOICE
Description	Setting Tone 1 high frequency • Frequency setting range is 2000 to 3992.1875 Hz • Register value = frequency(Hz)/7.8125 – 256		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
EXT_TONE1H							

Bits	Field Name	Description	Type	Reset Off
7:0	EXT_TONE1H	Frequency setting range 2000 to 3992.1875 Hz	RW	0x00

Table 13-55. DTMF_TONEXT1L Register

Address Offset	0x32		
Physical Address	0x0000 0032	**Instance**	AUDIO_VOICE
Description	Setting Tone 1 low frequency • Frequency setting range is 0 to 1992.1875 Hz • Register value = frequency(Hz)/7.8125		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
EXT_TONE1L							

Bits	Field Name	Description	Type	Reset Off
7:0	EXT_TONE1L	Frequency setting range is 0 to 1992.1875 Hz	RW	0x00

Table 13-56. DTMF_TONEXT2H Register

Address Offset	0x33		
Physical Address	0x0000 0033	**Instance**	AUDIO_VOICE
Description	Setting Tone 2 high frequency • Frequency setting range is 2000 to 3992.1875 Hz. • Register value = frequency(Hz)/7.8125 – 256		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
EXT_TONE2H							

Bits	Field Name	Description	Type	Reset Off
7:0	EXT_TONE2H	Frequency setting range is 2000 to 3992.1875 Hz	RW	0x00

Table 13-57. DTMF_TONEXT2L Register

Address Offset	0x34		
Physical Address	0x0000 0034	**Instance**	AUDIO_VOICE
Description	Setting Tone 2 low frequency • Frequency setting range is from 0 Hz to 1992.1875 Hz • Register value = frequency(Hz)/7.8125		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
EXT_TONE2I							

Bits	Field Name	Description	Type	Reset Off
7:0	EXT_TONE2L	Frequency setting range is 0 to 1992.1875 Hz	RW	0x00

Table 13-58. DTMF_TONOFF Register

Address Offset	0x35		
Physical Address	0x0000 0035	**Instance**	AUDIO_VOICE
Description	Setting time for tone on/off • During tone off, there is no tone. • During tone on, sound is operating.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
TONE_OFF_TIME				TONE_ON_TIME			

Bits	Field Name	Description	Type	Reset Off
7:4	TONE_OFF_TIME		RW	0x7
		0x0: 0 ms		
		0x1: 50 ms		
		0x2: 100 ms		
		0x3: 200 ms		

Bits	Field Name	Description	Type	Reset Off
		0x4: 250 ms		
		0x5: 300 ms		
		0x6: 400 ms		
		0x7: 500 ms		
		0x8: 750 ms		
		0x9: 1000 ms		
		0xA: 1500 ms		
		0xB: 2000 ms		
		0xC: 2500 ms		
		0xD: 3000 ms		
		0xE: 3500 ms		
		0xF: Reserved		
3:0	TONE_ON_TIME		RW	0x9
		0x0: 0 ms		
		0x1: 50 ms		
		0x2: 100 ms		
		0x3: 150 ms		
		0x4: 200 ms		
		0x5: 250 ms		
		0x6: 300 ms		
		0x7: 400 ms		
		0x8: 450 ms		
		0x9: 500 ms		
		0xA: 750 ms		
		0xB: 1000 ms		
		0xC: 1250 ms		
		0xD: 1500 ms		
		0xE: 1750 ms		
		0xF: 2000 ms		

Table 13-59. DMTF_WANONOFF Register

Address Offset	0x36		
Physical Address	0x0000 0036	**Instance**	AUDIO_VOICE
Description	Wobble on/off control • During wobble on, the frequency is that of Tone 1. • During wobble off, the frequency is that of Tone 2.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
WAMBLE_OFF_TIME				WAMBLE_ON_TIME			

Bits	Field Name	Description	Type	Reset Off
7:4	WAMBLE_OFF_TIME	Wobble off control	RW	0x1
		0x0: 0 ms		
		0x1: 31.25 ms		
		0x2: 50 ms		
		0x3: 100 ms		
		0x4: 150 ms		

Bits	Field Name	Description	Type	Reset Off
		0x5: 200 ms		
		0x6: 250 ms		
		0x7: 300 ms		
		0x8: 350 ms		
		0x9: 400 ms		
		0xA: 450 ms		
		0xB: 500 ms		
3:0	WAMBLE_ON_TIME		RW	0x1
		0x0: 0 ms		
		0x1: 31.25 ms		
		0x2: 50 ms		
		0x3: 100 ms		
		0x4: 150 ms		
		0x5: 200 ms		
		0x6: 250 ms		
		0x7: 300 ms		
		0x8: 350 ms		
		0x9: 400 ms		
		0xA: 450 ms		
		0xB: 500 ms		

Table 13-60. CODEC_RX_SCRAMBLE_H Register

Address Offset	0x37		
Physical Address	0x0000 0037	**Instance**	AUDIO_VOICE
Description	Audio DAC scramble upper 8 bits		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
CODEC_RX_SCRAMBLE_H							

Bits	Field Name	Description	Type	Reset Off
7:0	CODEC_RX_SCRAMBLE_H	Audio RX scramble upper 8 bits	RW	0x00

Table 13-61. CODEC_RX_SCRAMBLE_M Register

Address Offset	0x38		
Physical Address	0x0000 0038	**Instance**	AUDIO_VOICE
Description	Audio DAC scramble medium 8 bits		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
CODEC_RX_SCRAMBLE_M							

Bits	Field Name	Description	Type	Reset Off
7:0	CODEC_RX_SCRAMBLE_M	Audio RX scramble medium 8 bits	RW	0x00

Table 13-62. CODEC_RX_SCRAMBLE_L Register

Address Offset	0x39		
Physical Address	0x0000 0039	**Instance**	AUDIO_VOICE
Description	Audio DAC scramble lower 8 bits		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
CODEC_RX_SCRAMBLE_L							

Bits	Field Name	Description	Type	Reset Off
7:0	CODEC_RX_SCRAMBLE_L	Audio RX scramble lower 8 bits	RW	0x00

Table 13-63. APLL_CTL Register

Address Offset	0x3A		
Physical Address	0x0000 003A	**Instance**	AUDIO_VOICE
Description	Audio PLL control register If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ is powered off, the digital filter, analog section, and Bluetooth/voice/ audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED			APLL_EN	APLL_INFREQ			

Bits	Field Name	Description	Type	Reset Off
7:5	Reserved		RW	0x0
4	APLL_EN	PLL power control 0x0: Disabled 0x1: Enabled	RW	0
3:0	APLL_INFREQ	Input frequency selecting 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Reserved 0x5: 19.2 MHz 0x6: 26 MHz 0x7: Reserved 0xF: 38.4 MHz	RW	0x6

Table 13-64. DTMF_CTL Register

Address Offset	0x3B		
Physical Address	0x0000 003B	**Instance**	AUDIO_VOICE
Description	DTMF generator control		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED				TONE_MODE	TONE_PATTERN	DUAL_TONE_EN	TONE_EN

Bits	Field Name	Description	Type	Reset Off
7:4	Reserved		RW	0x0
3	TONE_MODE	Tone mode control 0x0: Single tone 0x1: Dual tone	RW	0
2	TONE_PATTERN	Tone pattern control 0x0: Continuous 0x1: Wobble	RW	0
1	DUAL_TONE_EN	 0x0: Off (single tone) 0x1: On (dual mode)	RW	0
0	TONE_EN	Tone generator start/stop 0x0: Disabled 0x1: Enabled	RW	0

Table 13-65. DTMF_PGA_CTL2 Register

Address Offset	0x3C		
Physical Address	0x0000 003C	**Instance**	AUDIO_VOICE
Description	DTMF gain control register 2		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
TONE_18DB_ATT	TONE4_GAIN			RESERVED	TONE3_GAIN		

Bits	Field Name	Description	Type	Reset Off
7	TONE_18DB_ATT	Tone attenuator gain control (TNATT) 0x0 Tone attenuator disabled: 0 dB : 0x1 Tone attenuator enabled: −18 dB :	RW	0

Bits	Field Name	Description	Type	Reset Off
6:4	TONE4_GAIN	Tone gain 4 control (TNG4) 0x0 –42 dB : 0x1 –36 dB : 0x2 –30 dB : 0x3 –24 dB : 0x4 –18 dB : 0x5 –12 dB : 0x6 –6 dB : 0x7 0 dB :	RW	0x4
3	Reserved		RW	0
2:0	TONE3_GAIN	Tone gain 3 control (TNG3) 0x0 –42 dB : 0x1 –36 dB : 0x2 –30 dB : 0x3 –24 dB : 0x4 –18 dB : 0x5 –12 dB : 0x6 –6 dB : 0x7 0 dB :	RW	0x4

Table 13-66. DTMF_PGA_CTL1 Register

Address Offset	0x3D		
Physical Address	0x0000 003D	**Instance**	AUDIO_VOICE
Description	Tone gain control register 1		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
Tone 2_GAIN				Tone 1_GAIN			

Bits	Field Name	Description	Type	Reset Off
7:4	Tone 2_GAIN	Tone gain 2 control (TNG2)` 0x0: –15 dB 0x1: –14 dB 0x2: –13 dB 0x3: –12 dB 0x4: –11 dB 0x5: –10 dB	RW	0x6

Bits	Field Name	Description	Type	Reset Off
		0x6: –9 dB		
		0x7: –8 dB		
		0x8: –7 dB		
		0x9: –6 dB		
		0xA: –5 dB		
		0xB: –4 dB		
		0xC: –3 dB		
		0xD: –2 dB		
		0xE: –1 dB		
		0xF: 0 dB		
3:0	Tone 1_GAIN	Tone gain 1 control (TNG1)	RW	0x9
		0x0: –15 dB		
		0x1: –14 dB		
		0x2: –13 dB		
		0x3: –12 dB		
		0x4: –11 dB		
		0x5: –10 dB		
		0x6: –9 dB		
		0x7: –8 dB		
		0x8: –7 dB		
		0x9: –6 dB		
		0xA: –5 dB		
		0xB: –4 dB		
		0xC: –3 dB		
		0xD: –2 dB		
		0xE: –1 dB		
		0xF: 0 dB		

Table 13-67. MISC_SET_1 Register

Address Offset	0x3E		
Physical Address	0x0000 003E	**Instance**	AUDIO_VOICE
Description	Miscellaneous 1		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
CLK64EN	SCRAMBLE_EN	FMLOOP_EN	RESERVED		SPARE2	SMOOTH_ANAVOL_EN	DIGMIC_LR_SWAP_EN

Bits	Field Name	Description	Type	Reset Off
7	CLK64_EN	64-kHz clock enable	RW	0
		0x0: Disabled		
		0x1: Enabled		

Bits	Field Name	Description	Type	Reset Off
6	SCRAMBLE_EN	Scramble function enable 0x0: Disabled 0x1: Enabled	RW	0
5	FMLOOP_EN	Analog FM radio loop enable 0x0: Disabled 0x1: Enabled	RW	0
4:3	Reserved		RW	0x0
2	SPARE2	Spare bit 2	RW	0
1	SMOOTH_ANAVOL_EN	Enable a smooth transition when analog volume control changes. 0x0: Bypass mode. Gain change is effective immediately (if signal, pop noise can be generated). 0x1: Pop noise reduced when analog gain change. The gain change is done when the signal crosses zero or after a 25-ms time-out.	RW	0
0	DIGMIC_LR_SWAP_EN	Digital mixing left and right swapping enable 0x0: Left and right not swapped 0x1: Left and right swapped	RW	0

Table 13-68. PCMBTMUX Register

Address Offset	0x3F		
Physical Address	0x0000 003F	**Instance**	AUDIO_VOICE
Description	PCM/BT mux and tone adder control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
MUXTX_PCM	MUXRX_PCM	MUXRX_BT	RESERVED	TNTXACT_PCM	TNRXACT_PCM	TNTXACT_BT	TNRXACT_BT

Bits	Field Name	Description	Type	Reset Off
7	MUXTX_PCM	Voice data out (VDX main) mux select 0x0: VTx data 0x1: BT data	RW	0
6	MUXRX_PCM	Voice RX input mux select 0x0: VTx data 0x1: BT data	RW	0
5	MUXRX_BT	Bluetooth data out mux select 0x0: VTx data 0x1: BT data	RW	0
4	Reserved		RW	0
3	TNTXACT_PCM	TONE on/off for PCM TX signal 0x0: Tone off 0x1: Tone on	RW	0
2	TNRXACT_PCM	TONE on/off for PCM RX signal 0x0: Tone off 0x1: Tone on	RW	0

Bits	Field Name	Description	Type	Reset Off
1	TNTXACT_BT	TONE on/off for BT TX signal 0x0: Tone off 0x1: Tone on	RW	0
0	TNRXACT_BT	TONE on/off for BT RX signal 0x0: Tone off 0x1: Tone on	RW	0

Table 13-69. RX_PATH_SEL Register

Address Offset	0x43		
Physical Address	0x0000 0043	**Instance**	AUDIO_VOICE
Description	RX path select control register		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED		RXL2_SEL	RXR2_SEL	RXL1_SEL		RXR1_SEL	

Bits	Field Name	Description	Type	Reset Off
7:6	Reserved	Reserved	RW	0x0
5	RXL2_SEL	Input RXL2 PGA select control 0x0: SDRL2 to RXL2 PGA 0x1: SDRM2 (mix SDRL2 and SDRR2) to RXL2 PGA	RW	0
4	RXR2_SEL	Input RXR2 PGA select control 0x0: SDRR2 to RXR2 PGA 0x1: SDRM2 (mix SDRL2 and SDRR2) to RXR2 PGA	RW	0
3:2	RXL1_SEL	Input RXL1 PGA select control 0x0: SDRL1 to RXL1 PGA (only in option 1) 0x1: SDRM1 (mix SDRL1 and SDRR1) to RXL1 PGA (only in option 1) 0x2: SDRL2 to RXL1 PGA 0x3: SDRM2 (mix SDRL2 and SDRR2) to RXL1 PGA	RW	0x0
1:0	RXR1_SEL	Input RXR1 PGA select control 0x0: SDRR1 to RXR1 PGA (only in option 1) 0x1: SDRM1 (mix SDRL1 and SDRR1) to RXR1 PGA (only in option 1) 0x2: SDRR2 to RXR1 PGA 0x3: SDRM2 (mix SDRL2 and SDRR2) to RXR1 PGA	RW	0x0

Table 13-70. VDL_APGA_CTL Register

Address Offset	0x44		
Physical Address	0x0000 0044	**Instance**	AUDIO_VOICE
Description	Voice downlink analog PGA control register If the codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If the CODECPDZ is powered off, the digital filter, analog section, and Bluetooth/voice/ audio interfaces are switched off, regardless of this register setting.		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
VDL_GAIN_SET					VDL_FM_EN	VDL_DA_EN	VDL_PDZ

Bits	Field Name	Description	Type	Reset Off
7:3	VDL_GAIN_SET	Analog programmable gain control 0x0: 12 dB 0x1: 10 dB 0x2: 8 dB 0x3: 6 dB 0x4: 4 dB 0x5: 2 dB 0x6: 0 dB 0x7: –2 dB 0x8: –4 dB 0x9: –6 dB 0xA: –8 dB 0xB: –10 dB 0xC: –12 dB 0xD: –14 dB 0xE: –16 dB 0xF: –18 dB 0x10: –20 dB 0x11: –22 dB 0x12: –24 dB	RW	0x6
2	VDL_FM_EN	FM loop path enable control bit 0x0: Disabled 0x1: Enabled	RW	0
1	VDL_DA_EN	Digital-to-analog path enable control bit 0x0: Disabled 0x1: Enabled	RW	1
0	VDL_PDZ	Analog PGA power control bit 0x0: Power-down mode 0x1: Application mode	RW	0

Table 13-71. VIBRA_CTL

Address Offset	0x45		
Physical Address	0x0000 0045	**Instance**	AUDIO_SCAUDIO_VOICE
Description	Vibrator H-bridge control register If codec power control register bit (CODECPDZ) setting is powered on, this register setting is assumed valid. If CODECPDZ is off, the codec is powered down and this register setting has no effect.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SPARE	VIBRA_DIR_SEL	VIBRA_SEL	VIBRA_AUDIO_SEL		VIBRA_DIR	VIBRA_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	SPARE	Spare bit	RW	0
5	VIBRA_DIR_SEL	Vibrator H-bridge direction selection bit (available only if audio data drive the vibrator H-bridge) 0x0: Direction is given by the VIBRA_DIR bit. 0x1: Direction is given by the audio data MSB.	RW	0
4	VIBRA_SEL	Vibrator H-bridge driver selection 0x0: Local vibrator driver (controlled by OCP register, average value control word in VIBRA_SET register) 0x1: Audio data as vibrator driver (the audio channel controlled by AUDIOCH word control)	RW	0
3:2	VIBRA_AUDIO_ SEL	Audio channel selection control 0x0: LEFT1 input selection 0x1: RIGHT1 input selection 0x2: LEFT2 input selection 0x3: RIGHT2 input selection	RW	0x0
1	VIBRA_DIR	H-bridge direction control bit 0x0: Positive polarity 0x1: Negative polarity	RW	0
0	VIBRA_EN	H-bridge power control 0x0: Vibrator H-bridge is OFF 0x1: Vibrator H-bridge is ON	RW	0

Table 13-72. VIBRA_SET

Address Offset	0x46		
Physical Address	0x0000 0046	**Instance**	AUDIO_SCAUDIO_VOICE
Description	Vibrator H-bridge PWM generator turnoff control register		
Type	RW		

7	6	5	4	3	2	1	0
VIBRA_AVG_VAL							

Bits	Field Name	Description	Type	Reset
7:0	VIBRA_AVG_VAL	Sets the vibrator H-bridge PWM generator turnon value. The average value is the inverse of the VIBRA_AVG_VAL value. The minimal value is 0x01 and the value 0x00 is forbidden.	RW	0x00

Table 13-73. ANAMIC_GAIN Register

Address Offset	0x48		
Physical Address	0x0000 0048	**Instance**	AUDIO_VOICE
Description	Gain control of the microphone amplifier		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
RESERVED		MICAMPR_GAIN			MICAMPL_GAIN		

Bits	Field Name	Description	Type	Reset Off
7:6	Reserved	Reserved	RW	0x0
5:3	MICAMPR_GAIN	Two interpretations: If ALC is disabled: Gain setting of the right microphone amplifier. If ALC is enabled for sub-mic: Maximum gain setting of the right microphone amplifier. 0x0: 0 dB 0x1: 6 dB 0x2: 12 dB 0x3: 18 dB 0x4: 24 dB 0x5:1 30 dB	RW	0x0
2:0	MICAMPL_GAIN	Two interpretations: If ALC is disabled: Gain setting of the left microphone amplifier. If ALC is enabled for main microphone: Maximum gain setting of the left microphone amplifier. 0x0: 0 dB 0x1: 6 dB 0x2: 12 dB 0x3: 18 dB 0x4: 24 dB 0x5: 30 dB	RW	0x0

Table 13-74. MISC_SET_2 Register

Address Offset	0x49		
Physical Address	0x0000 0049	**Instance**	AUDIO_VOICE
Description	Miscellaneous 2		
Type	RW		
Write Latency			

7	6	5	4	3	2	1	0
SPARE2	VTX_3RD_HPF_BYP	ATX_HPF_BYP	VRX_3RD_HPF_BYP	ARX_HPF_BYP	VTX_HPF_BYP	VRX_HPF_BYP	SPARE1

Bits	Field Name	Description	Type	Reset Off
7	SPARE2	Spare bit 1	RW	0
6	VTX_3RD_HPF_ BYP	Voice TX third-order high-pass filter bypass mode control 0x0: High-pass filter in application mode 0x1: High-pass filter bypassed	RW	0
5	ATX_HPF_BYP	Audio TX high-pass filter bypass mode control 0x0: High-pass filter in application mode 0x1: High-pass filter bypassed	RW	0
4	VRX_3RD_HPF_ BYP	Voice RX third-order high-pass filter bypass mode control 0x0: High-pass filter in application mode 0x1: High-pass filter bypassed	RW	0
3	ARX_HPF_BYP	Audio RX high-pass filter bypass mode control 0x0: High-pass filter in application mode 0x1: High-pass filter bypassed	RW	0
2	VTX_HPF_BYP	Voice TX high-pass filter bypass mode control 0x0: High-pass filter in application mode 0x1: High-pass filter bypassed	RW	0
1	VRX_HPF_BYP	Voice RX high-pass filter bypass mode control 0x0: High-pass filter in application mode 0x1: High-pass filter bypassed	RW	0
0	SPARE1	Spare bit 2	RW	0

Universal Serial Bus

This chapter describes the universal serial bus (USB) function in the device integrated power-management/audio coder/decoder (codec) device.

Topic **Page**

14.1 USB PHY Overview

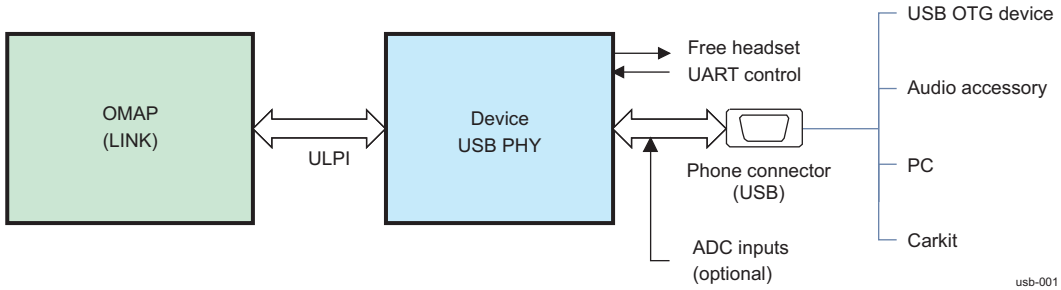
The primary function of the universal serial bus (USB) physical layer (PHY) is to transmit and receive USB data at high speed (HS) (480 Mbps), full speed (FS) (12 Mbps), and low speed (LS) (1.5 Mbps). It also provides a pin-optimized standard USB transceiver macrocell interface (UTMI)+ low pin interface (ULPI) to a main USB link layer device (LINK) controller.

The USB PHY can also interface to a CEA-936-A-compliant device (charger, smart or basic carkit, or phone-powered accessory) using 4-wire or 5-wire protocol.

NOTE: References to audio apply only to the TPS65930.

Figure 14-1 shows the USB PHY.

Figure 14-1. USB PHY



The device has a USB On-The-Go (OTG) carkit transceiver that allows system implementation that complies with the following specifications:

- *Universal Serial Bus 2.0 Specification*
- *On-The-Go Supplement to the USB 2.0 Specification*
- *CEA-2011: OTG Transceiver Interface Specification*
- *CEA-936A: Mini-USB Analog Carkit Specification*
- *UTMI+ Low Pin Interface Specification*

The features of the individual specifications are:

- *Universal Serial Bus 2.0 Specification* (hereafter referred to as the USB 2.0 specification):
  - 5-V-tolerant data line at HS/FS, FS-only, and LS-only transmission rates
  - 7-V-tolerant video bus (VBUS) line
  - Integrated data line serial termination resistors (factory-trimmed)
  - Integrated data line pullup and pulldown resistors
  - On-chip 480-MHz phase-locked loop (PLL) from the internal system clock (19.2, 26, and 38.4 MHz)
  - Synchronization (SYNC)/end-of-period (EOP) generation and checking
  - Data and clock recovery from the USB stream
  - Bit-stuffing/unstuffing and error detection
  - Resume signaling, wakeup, and suspend detection
  - USB 2.0 test modes
- *On-The-Go Supplement to the USB 2.0 Specification* (hereafter referred to as the OTG supplement to the USB 2.0 specification):
  - 3-pin LS/FS serial mode (DAT_SE0)
  - 4-pin LS/FS serial mode (VP_VM)
- *CEA-2011: OTG Transceiver Interface Specification*:
  - 3-pin LS/FS serial mode (DAT_SE0)
  - 4-pin LS/FS serial mode (VP_VM)
- *CEA-936-A: Mini-USB Analog Carkit Interface Specification* (hereafter referred to as the CEA-936-A specification):

- 5-pin Consumer Electronics Association (CEA) mini-USB analog carkit interface
- UART signaling
- Audio (mono/stereo) signaling
- UART transactions during audio signaling
- Basic and smart 4-wire/5-wire carkit, chargers, and accessories
- ID CEA resistor comparators

• *UTMI + Low Pin Interface Specification* (hereafter referred to as the ULPI specification):

- 12-pin ULPI with 8-pin parallel data for USB signaling and register access
- 60-MHz clock generation
- Register mapping

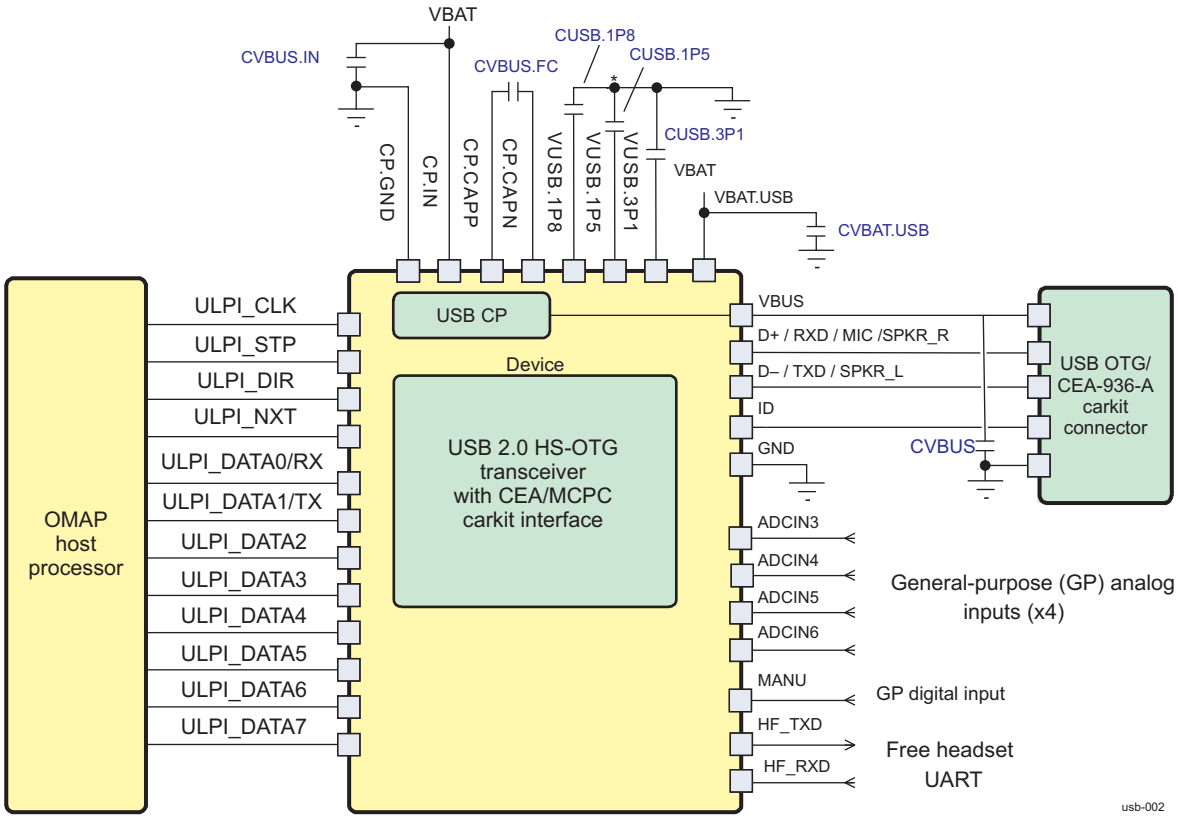
14.2 USB PHY Environment

This section describes the USB PHY environment.

Figure 14-2 shows a typical way to use the USB module in an application.

Figure 14-2 shows USB module connectivity in a typical USB-OTG application or in a USB + CEA-936-A carkit application.

Figure 14-2. USB/CEA-936-A Carkit Application Example



NOTE: IEC electrostatic sensitive device (ESD) protection is not shown.

14.2.1 ULPI Functional Interface

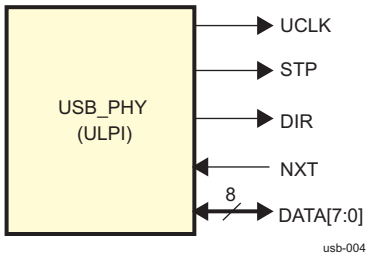
The ULPI specification defines a generic bus to interface a USB 2.0 HS PHY with the USB LINK controller. The ULPI defines a clock, three control signals, a bidirectional data bus, and bus arbitration.

This bus routes UART signals through the PHY for carkit applications. It can also be used to interface with a USB FS LINK controller with a 3-pin or a 4-pin bidirectional serial interface.

14.2.1.1 ULPI Pins for the USB PHY

Figure 14-3 shows the ULPI signals.

Figure 14-3. ULPI Signals



14.2.1.2 ULPI Interface Description

Table 14-1 lists the ULPI inputs and outputs.

Table 14-1. ULPI Inputs/Outputs

Signal Name	I/O (1)	Description		Reset Value
UCLK	O	60-MHz UTMI clock output. By default, control and data signals are synchronous with UCLK.		0
DIR	O	Data direction control. By default, DIR is low and the PHY listens for nonzero data from the LINK. The PHY asserts DIR to get control of the data bus.		0
STP	I	Stop signal. The LINK drives STP high to signal the end of its data stream. The LINK can also drive STP high to request data bus access from the PHY.		HiZ + pullup
NXT	O	Next signal. The PHY drives NXT high to throttle the data bus.		0
DATA[0]	I/O	ULPI:	Bidirectional data signal (data timed on the rising edge of the clock)	ULPI mode − HiZ
	I	UART:	TXI data input that is routed to the D– pin	
	I	FS USB PHY:	Transmit enable (TXEN in ULPI mode)	
	I/O	3-pin FS USB PHY:	Bidirectional transmit/receive single-ended 0 (SE0 in CEA-2011 mode)	
	I/O	4-pin FS USB PHY:	Bidirectional single-ended receive/transmit (VM in CEA-2011 mode)	
DATA[1]	I/O	ULPI:	Bidirectional data signal (data timed on the rising edge of the clock)	ULPI mode − HiZ
	O	UART:	RXO data output routed from D+ pin	
	I/O	3-pin FS USB PHY:	Bidirectional transmit/receive differential data (DAT)	
	I/O	4-pin FS USB PHY:	Bidirectional single-ended receive/transmit (VP)	
DATA[2]	I/O	ULPI:	Bidirectional data signal (data timed on the rising edge of the clock)	ULPI mode − HiZ
	I	UART:	Request to send data input (RTSI)	
	I/O	3-pin FS USB PHY:	Bidirectional transmit/receive SE0 (SE0 in ULPI mode)	
	I/O	4-pin FS USB PHY:	Bidirectional single-ended receive/transmit (VM in ULPI mode)	
	I/O	FS USB PHY:	Active low output enable input and active low interrupt output (OE/INT_ in CEA-2011 mode)	
DATA[3]	I/O	ULPI:	Bidirectional data signal (data timed on the rising edge of the clock)	ULPI mode − HiZ
	O	UART:	Clear to send data output (CTSO)	
	O	4-pin FS USB PHY:	Differential receiver output (RCV)	
	O	Active high interrupt output (INT)		
DATA[4]	I/O	ULPI:	Bidirectional data signal (data timed on the rising edge of the clock)	ULPI mode − HiZ
DATA[5]	I/O	ULPI:	Bidirectional data signal (data timed on the rising edge of the clock)	ULPI mode − HiZ

(1) I = Input, O = Output

Table 14-1. ULPI Inputs/Outputs (continued)

Signal Name	I/O (1)	Description		Reset Value
DATA[6]	I/O	ULPI:	Bidirectional data signal (data timed on the rising edge of the clock)	ULPI mode − HiZ
	O	4-pin FS USB PHY:	Differential receiver output (RCV)	
DATA[7]	I/O	ULPI:	Bidirectional data signal (data timed on the rising edge of the clock)	ULPI mode − HiZ

14.2.1.3 ULPI Protocol and Data Format Overview

The USB PHY of the device supports the 8-bit data bus in the internal clock mode of the ULPI specification.

The PHY is the master of the ULPI interface; the direction of the LINK data bus is determined by the DIR signal from the PHY.

A turnaround cycle is inserted on the data bus when the DIR signal changes. During this cycle, the data bus is not driven by the LINK or the PHY; the PHY holds its ULPI bus in high-impedance state during this turnaround cycle.

During idle, the LINK owns the data bus and continuously drives the bus to 00h.

The LINK initiates a transmission by driving a nonzero value on the data bus, and then signals the end of the transmission by asserting a stop (STP) signal.

During transmit, the NXT signal acts as an acknowledgment line to signal that the PHY has captured the data sent by the LINK. The PHY can abort a transmission from the LINK by asserting the DIR signal.

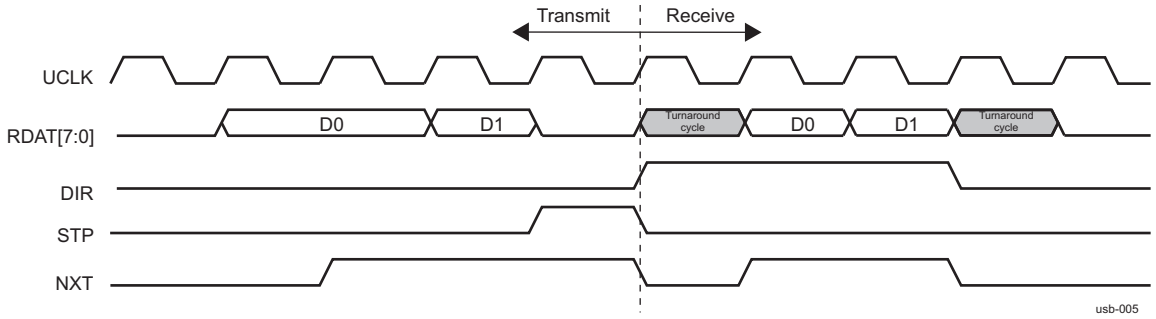
When the PHY sends data to the LINK, it asserts DIR and keeps it high until the last data is sent.

During receive, NXT acts as a validation line to signal that the PHY outputs valid data.

The LINK can abort a reception by asserting STP for one clock cycle.

Figure 14-4 shows the transmit-and-receive protocol. For more information about the ULPI protocol, see the ULPI specification.

Figure 14-4. ULPI Transmit-and-Receive Protocol Overview



14.2.1.4 3-Pin and 4-Pin Bidirectional Protocol and Data Format Overview

The USB PHY supports the 3-pin DAT-SE0 and 4-pin VP-VM modes of the CEA-2011 specification.

In DAT-SE0 mode, the DAT pin sends single-ended data to the transceiver (when OE_ = low) or to receive single-ended data from the transceiver (when OE_ = high). The SE0 pin forces the D+/D– outputs of the transceiver to the SE0 state (when OE_ = low) or indicates that the D+/D– lines are logic low (when OE_ = high). The RCV pin is not used in this mode.

In VP_VM mode, the VP pin is used to drive the level of the D+ pin (when OE_ = low) or to indicate the logic level on the D+ pin (OE_ = high). The _VM pin is used to drive the level of the D– pin (when OE_ = low) or to indicate the logic level on the D– pin (when OE_ = high). The RCV pin is always an output, and comes from a differential receiver.

The OE_INT pin can also be an active low interrupt output when the transceiver is in suspend mode.

The ULPI specification also defines similar serial modes but requires opposite polarity for the transmit enable signal (TXEN = not OE_) and for the interrupt pin (INT is active high for ULPI; INT_ is active low for CEA-2011). The USB PHY of the device also supports the ULPI definition.

For more information about this protocol, see the CEA-2011 specification.

14.2.1.5 UART Protocol and Data Format Overview

The USB PHY allows the routing of UART signals through the PHY. In UART mode, the USB PHY only passes data through and usually only provides DC level-shifting adaptation, except in CEA-936-A data during audio (DDA) mode.

In basic UART mode, the TXI pin (DATA0) drives the level of the D– pin or the HF_TXD pin. The RXO pin (DATA1) indicates the logic level of the D+ pin or the HF_RXD pin.

For UART mode with hardware handshake, the RTSI pin (DATA2) drives the level on the RTSO pin, and the CSTO pin (DATA3) indicates the logic level on the CTSI pin.

In CEA-936-A DDA mode, each signal transition that occurs on the TXI pin (DATA0) is output as a calibrated pulse on the D– pin, and the level on the RXO pin (DATA1) toggles for each detected pulse received on the D+ pin.

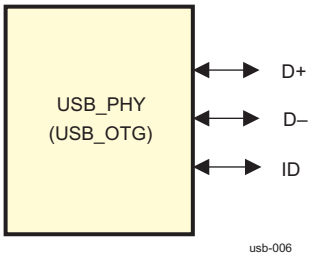
14.2.2 USB OTG Functional Interfaces

14.2.2.1 USB OTG Pins for USB PHY

USB OTG pins interface directly with the USB connector without requiring external components, except for low-capacitance external International Electro-technical Commission (IEC) electrostatic discharge (ESD) protection (recommended). The serial terminations and data line pullup/pulldown resistors are integrated in the USB PHY. The 45-Ω nominal serial data line termination is trimmed at the factory and does not require an external calibration resistor. The pullup and pulldown values of the data lines comply with the *USB ECN: Pull-Up/Pull-Down Resistors* specification (hereafter referred to as the USB ECN 2.0 specification) in USB mode, or with the MCPC ME-UART specification in MCPC UART mode.

Figure 14-5 shows the USB OTG signals.

Figure 14-5. USB OTG Signals



14.2.2.2 USB OTG Interface Description

Table 14-2 lists the USB OTG inputs and outputs.

Table 14-2. USB OTG Inputs/Outputs

Signal Name	I/O (1) (2)	Description	Reset Value
USB_DP	AI/O	3 V I/O (5.25-V tolerant). Connects to the D+ pin of the USB cable (without external serial resistor)	USB mode, HiZ with USB pulldown
		USB mode: Bidirectional D+	
		UART mode: RXD input signal	

(1) I = Input, O = Output, A = Analog
(2) These I/Os are in the VUSB3V1 power domain.

Table 14-2. USB OTG Inputs/Outputs (continued)

Signal Name	I/O (1) (2)	Description		Reset Value
		Analog audio mode:	Microphone input, right stereo speaker output (CEA)	
USB_DM	AI/O	3 V I/O (5.25-V tolerant). Connects to the D− pin of the USB cable (without external serial resistor)		USB mode, HiZ with USB pulldown
		USB mode:	Bidirectional D−	
		UART mode:	TXD output signal programmable for push-pull or open-drain operation	
		CEA audio mode:	Speaker mono or stereo left output (CEA)	
USB_ID	AI/O	3 V I/O (5.25-V tolerant). Connects to the ID pin of the USB cable		
		Detects the following:		Analog input
			USB OTG A or B default (ground [GND] or open)	
			CEA accessory (100K)	
			CEA charger type (200K, 400K)	
		Generates the following:		Analog output
			Interrupt (pulled to GND) during 5-wire carkit protocol	

14.2.2.3 USB OTG Protocol and Data Format

The USB PHY supports the USB OTG definition of the USB. The USB is a cable bus that supports data exchange between a host and a peripheral. The OTG supplement defines limited requirements to enable portable USB applications. A description of the USB or OTG protocol is outside the scope of this document. For more information about the USB protocol, see the USB 2.0 specification or the OTG supplement to the USB specification.

14.2.2.4 CEA-936-A Protocol and Data Format

The USB PHY allows operation of the USB data lines as defined in the CEA-936-A specification.

In CEA-936-A UART mode, the D− pin indicates the logic level on the ULPI DATA0 pin (TXI); the D+ pin drives the level of the ULPI DATA1 pin (RXO) when not in audio mode.

In CEA-936-A audio mode, the D− pin carries the analog audio output speaker left channel signal that comes from the device audio function; the D+ pin carries the analog audio microphone signal as an input or the analog audio speaker right channel as an output in stereo mode.

In CEA-936-A DDA mode, UART commands are transported as pulses and carried over the audio signals operating in mono mode.

For more information about the CEA-936-A carkit protocol, see the CEA-936-A specification.

14.2.3 Power Supply Pin Interface

Table 14-3 lists the inputs and outputs of the USB power supplies.

Table 14-3. USB Power Supply I/O

Signal Name	I/O (1)	Description	Reset Value
VUSB3V1	PWR-OUT	Regulated 3.1-V power supply for USB PHY; requires external decoupling; not usable to power another IC	
VUSB1V8	PWR-OUT	Regulated 1.8-V power supply for USB PHY; requires external decoupling; not usable to power another IC	
VUSB1V5	PWR-OUT	Regulated 1.5-V power supply for USB PHY; requires external decoupling; not usable to power another IC	
CP.IN	PWR-IN	Battery voltage input to the 5-V charge pump	
CP.GND	PWR-IN	Power ground	

(1) A = Analog

Table 14-3. USB Power Supply I/O (continued)

Signal Name	I/O (1)	Description	Reset Value
VBUS	PWR-IN/OUT	Used by the VBUS comparators and optionally to power the VUSB3V1 low dropout (LDO). It is also the charge pump output.	
CP.CAPP	A	Flying capacitor pin for the 5-V charge pump	
CP.CAPM	A	Flying capacitor pin for the 5-V charge pump	

14.2.4 USB External Components

The USB can support an external ESD protection device and a DP/DM common-mode filter device.

14.2.4.1 ESD Device

To improve ESD robustness on DP/DM, the USB can support an external ESD protection circuit designed for a HS data rate and having capacitance of less than 1 pF on DP/DM.

TI recommends the RClamp052B from SEMTECH.

Contact TI Field Applications Engineering for assistance.

14.2.4.2 DP/DM Common-Mode Filter

If improved electromagnetic interference (EMI) immunity is required, the USB interface works with a common-mode filter on the DP and DM lines if the filter's DC series resistance is less than 1 ohm.

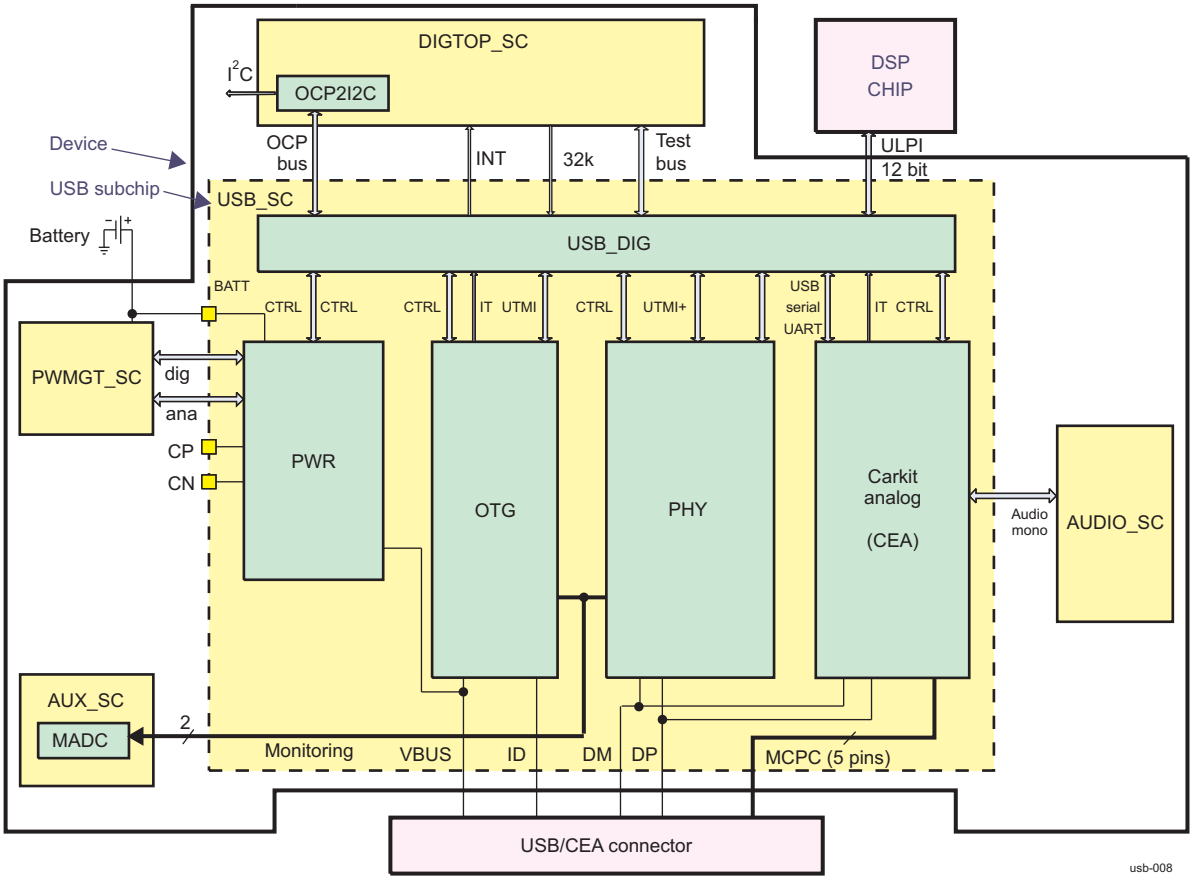
14.3 USB Integration

The USB module interfaces with the following functions in the device:

- Power, reset, and clock management (PRCM) module
- Battery charger interface (BCI)
- MADC module
- Audio module
- Open-core protocol (OCP) digital interconnect for inter-integrated circuit (I^2C™) register access and interrupt support

Figure 14-6 shows integration of the USB module in the device.

Figure 14-6. USB Module Integration in the Device

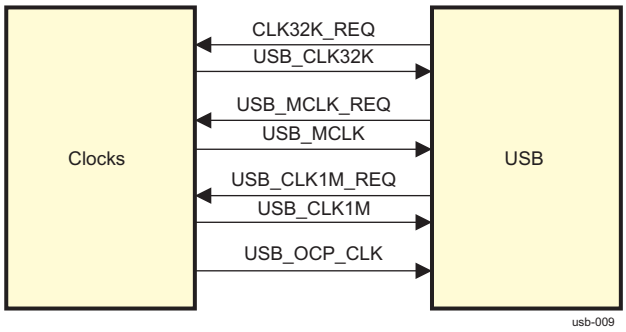


14.3.1 Clocking, Reset, and Power-Management Scheme

14.3.1.1 Clocks

Figure 14-7 shows the interface with the clock module.

Figure 14-7. Interface With the Clock Module



The USB receives four clocks from the clocks module (USB_CLK32K, USB_CLK1M, USB_MCLK, and USB_OCP_CLK) and generates one UTMI_CLK.

USB_CLK32K is the 32.768-kHz clock. It is used by the debounce timers on the VBUS and ID signals, by the phone state-machine (PSM) timers for CEA-936-A operations, and by the VBAT monitoring function timer that generates a periodic conversion request to the MADC for the BCI. This clock is always available when the system is running, but it can be disabled by clearing the PHY_CLK_CTRL CLK32K_EN bit.

USB_CLK1M is a 1-MHz clock used by the VBUS charge pump. The charge pump must be enabled to request this clock. The associated request signal USB_CLK1M_REQ is directly controlled by DRVVBUS in the OTG_CTRL register.

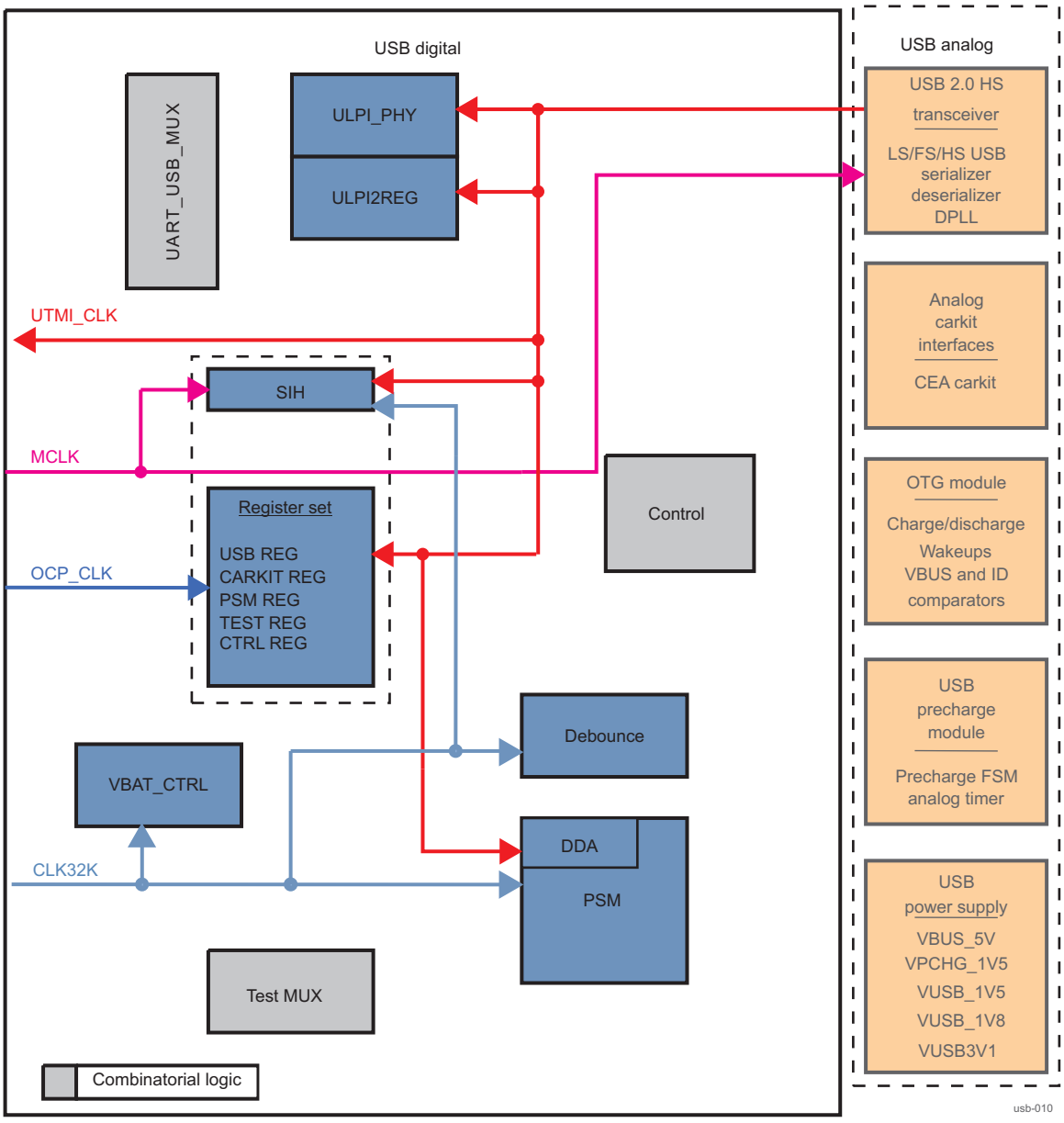
USB_MCLK is the main system clock (19.2, 26, or 38.4 MHz). This clock is used by the 480-MHz digital phase-locked loop (DPLL) in the USB 2.0 PHY to generate the 60-MHz UTMI clock frequency. The DPLL uses the MCLK_FREQ setting to select the correct DPLL ratio. The associated request signal USB_MCLK_REQ is directly controlled by the PHY_PWR_CTRL[0] PHYPWD bit. By default, this clock is always requested.

USB_OCP_CLK is used to access registers in the USB through I^2C accesses. This clock is half the frequency of USB_MCLK.

UTMI_CLK is a 60-MHz clock used by the USB 2.0 PHY ULPI controller function to access registers in the USB through ULPI or I^2C accesses. It generates the ULPI CLK signal in synchronous mode.

Figure 14-8 shows USB clock distribution.

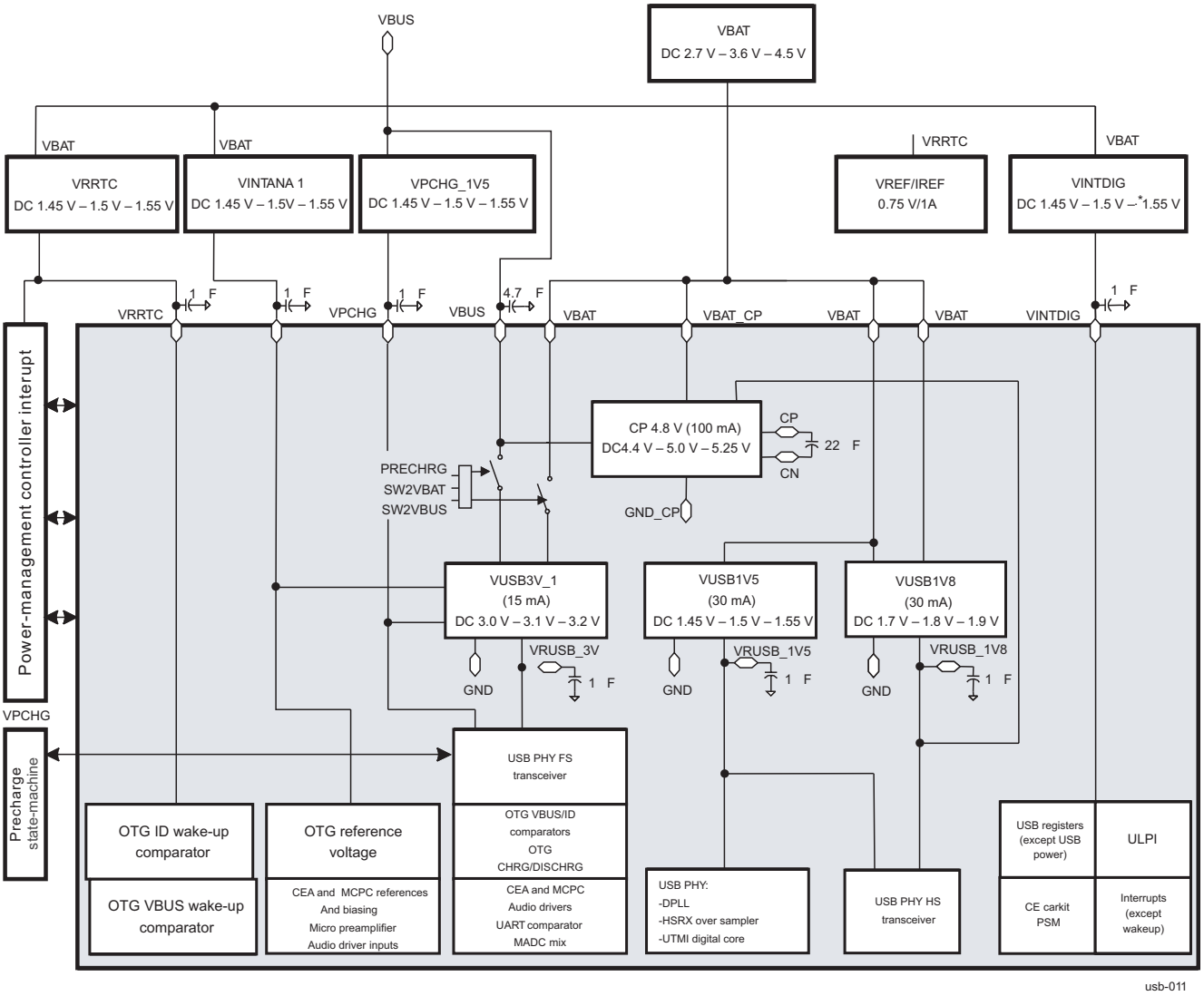
Figure 14-8. USB Clock Distribution Scheme



14.3.1.2 Power Management

The USB uses battery voltage (VBAT) to power the USB 2.0 transceiver by producing three regulated voltage supplies (VUSB3.1V, VUSB1.8V, and VUSB1.5V). The VBUS pin from the USB connector can also be considered an external power supply source, because it can be used to power the VUSB3.1V LDO in place of VBAT or for battery charging. It also uses three shared 1.5-V nominal power supply sources (VRRTC, VINTANA1, and VINTDIG) and a bandgap 0.75-V reference voltage (VREF) from the device POWERMGT module. It receives a power source (VPCHG) and a bandgap reference voltage from the BCI to handle battery precharge cases. Figure 14-9 shows the USB power domains.

Figure 14-9. USB Power Domains



14.3.1.2.1 VUSB3V1

The USB PHY uses an internal 3.1-V LDO (VUSB3V1) whose input can be supplied from VBAT (default) or VBUS. The choice between VBAT or VBUS is controlled by the SW2VBAT and SW2VBUS register bits in the device PWR_MGT module (see Chapter 6, *Power Resources*, Section 6.4.2.6, *VUSB3V1 LDO*). A sleep mode decreases power consumption.

If the device is in precharge mode, VRRTC is off and no digital control is available. When receiving VBUSPRECH high (VBUS_STS in BCI), the VUSB_3P1 is automatically switched to VBUS.

In normal mode (battery voltage OK), the switch is controlled by internal software.

An unconfigured B-device must not consume more than 150 μA on VBUS. Therefore, it is recommended that the default mode for the switch is for VUSB3V1 to be supplied by VBAT. Once configured, the host processor can switch the input for VUSB3V1 to VBUS, although current consumption exceeds 8 mA.

The device enters active mode when VBAT > = 3.2 V. Therefore, the host processor must manually monitor VBAT and check for VBAT > 3.3 V before allowing USB activity.

VBUS can be generated from the USB charge pump (when it is an A-device) or from an external device (when it is a B-device).

VUSB3V1 is also used to bias analog multiplexers on the four MCPC pins between the carkit and the MADC (supplied by VINTANA2). Therefore, VUSB3V1 must be powered up before VINTANA2 to avoid unwanted leakages. This application does not require a large current-driving capability from the 3.1-V LDO; it can be configured in sleep mode.

By default, the device power-up sequence powers up the VUSB3V1 in sleep mode before it powers up VINTANA2.

14.3.1.2.2 VUSB_1V5 and VUSB_1V8

The USB PHY uses two other LDOs (VUSB_1V5 and VUSB_1V8), which are directly supplied by VBAT. To avoid simultaneous large inrush current, it is recommended to delay the power on of VUSB_1V5 from VUSB_1V8 by 10~20 μs. The estimated inrush current is 450 mA for each LDO, which corresponds to a combined power dissipation of 450 mA*2*4.5 V = 4.05 W for a peak duration of 2 μs at power on (total power-on time is ~ 20 μs), if they are powered on simultaneously.

14.3.1.3 Resets

14.3.1.3.1 Hardware Reset

The USB receives USB_RESET_NA from the device power subchip. This is the master reset from the device power-management state-machine, which resets the logic and the registers in the USB.

14.3.1.3.2 Software Reset

There are two main possibilities of software reset at the USB module level:

- UTMI core reset with setting RESET = 1 in the FUNC_CTRL register
- PSM software reset with setting CARKIT_PSM_RESET in the CARKIT_ SM_CTRL register

There are other small individual sources of self-reset for registers with autoclear functions.

14.3.1.4 Power Domain

For more information about the power domain, see Figure 14-9 and Section 14.3.1.2, *Power Management.*

14.3.2 Hardware Requests

14.3.2.1 Interrupt Requests

The USB_SC module can signal interrupts internally through the INT1 line or externally through its ULPI interface. For a detailed description of the interrupts, see Section 14.4.6, *Interrupts*.

14.3.2.2 Wake-Up Requests

Two wake-up requests (VBUS_PRES and ID_PRES) are signaled by the USB to the PWRMGT module when a voltage presence on the VBUS pin or a resistor-to-ground on the ID pin is detected. For more information about VBUS_PRES and ID_PRES wake-up requests, see Section 14.4.8.1, *VBUS and ID Wake-Up Interrupt*.

VBUS and ID detection is supplied by VRRTC and allows waking of the device from wait-on mode (only the VRRTC regulator is on; no USB regulated voltage is available).

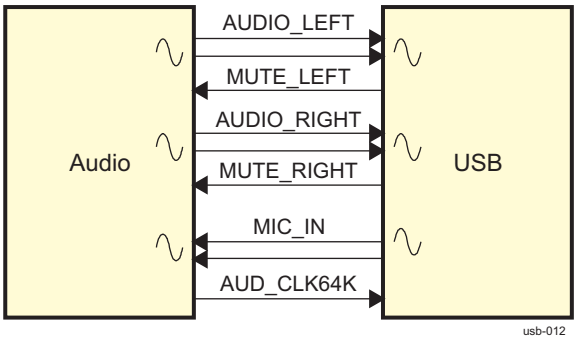
14.3.3 MADC and USB Interface

The USB subchip can power on the MADC through an internal signal. The USB subchip can then request the MADC for measurement of VBAT to determine whether to use the VBAT or VRUSB supply in slave mode. First, the USB subchip sends an internal signal to power on MADC. This is followed by MADC conversion requests based on a timer in the USB subchip. The USB conversion request is similar to a general-purpose (GP) conversion, because it can generate interrupts on the primary interrupt handler (PIH) at the end of the conversion; the results of the conversion are stored in registers accessible by the host processor through the I^2C interface.

14.3.4 Audio and USB Interface

Figure 14-10 shows the USB interface with the audio module.

Figure 14-10. Interface With the Audio Module



14.4 Functional Description

14.4.1 Functional Modes and Datapath Control

14.4.1.1 USB Synchronous Mode

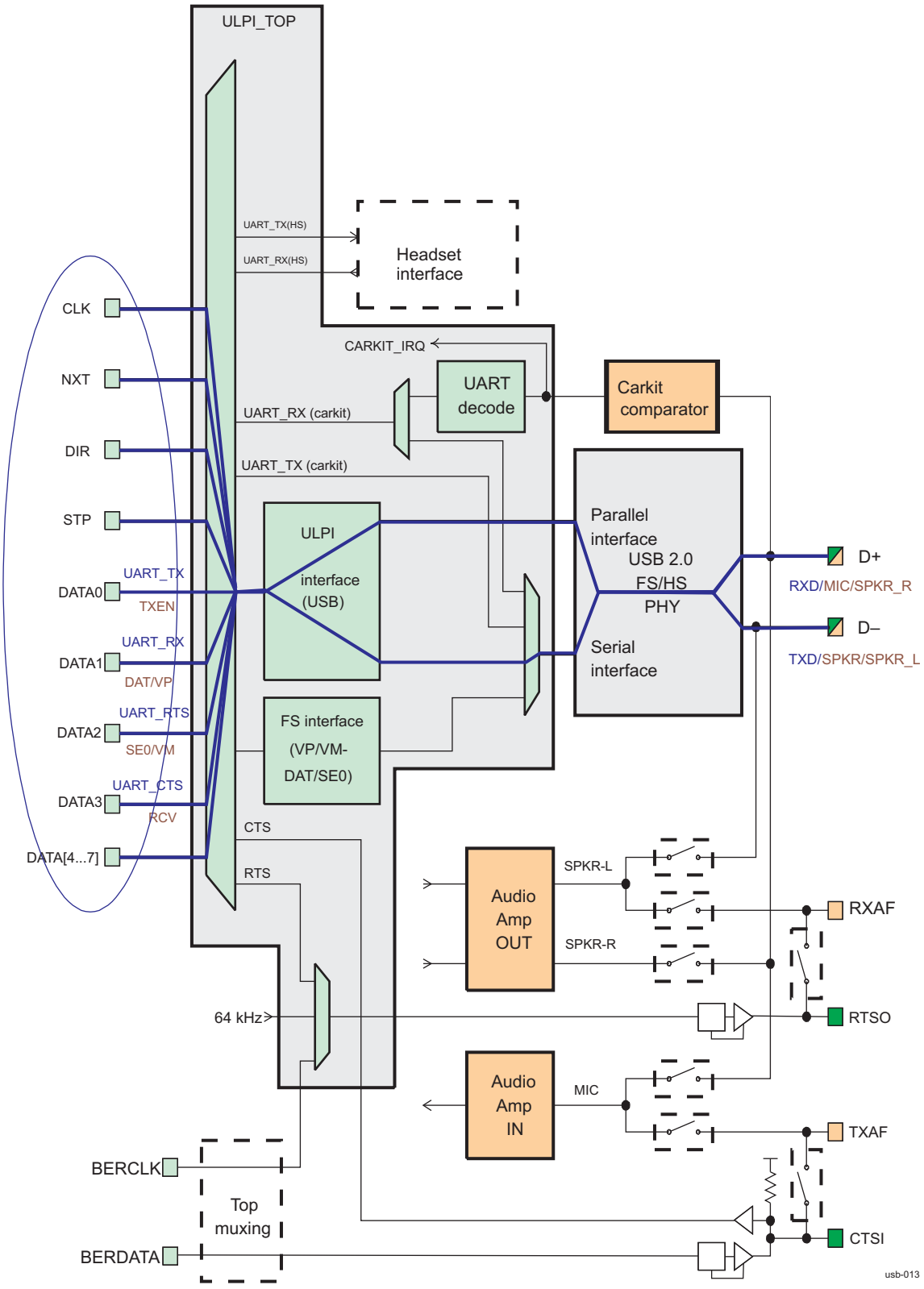
USB synchronous mode is the normal and default mode of operation.

This mode supports USB HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps) transfers.

In this mode, the ULPI 8-bit data bus carries USB commands and data that are exchanged with the USB PHY through the ULPI parallel interface, as defined in the ULPI specification.

Figure 14-11 shows USB synchronous mode.

Figure 14-11. USB Synchronous Mode



14.4.1.2 USB ULPI 3-Pin Serial Mode

In USB ULPI 3-pin serial mode, the ULPI data bus is redefined as a 3-pin serial interface using DAT/SE0 encoding, as defined in the ULPI specification. DAT/SE0 encoding is used to exchange data through a direct access to the FS/LS analog transmitter and receiver.

Serial mode supports only USB FS and LS transfers.

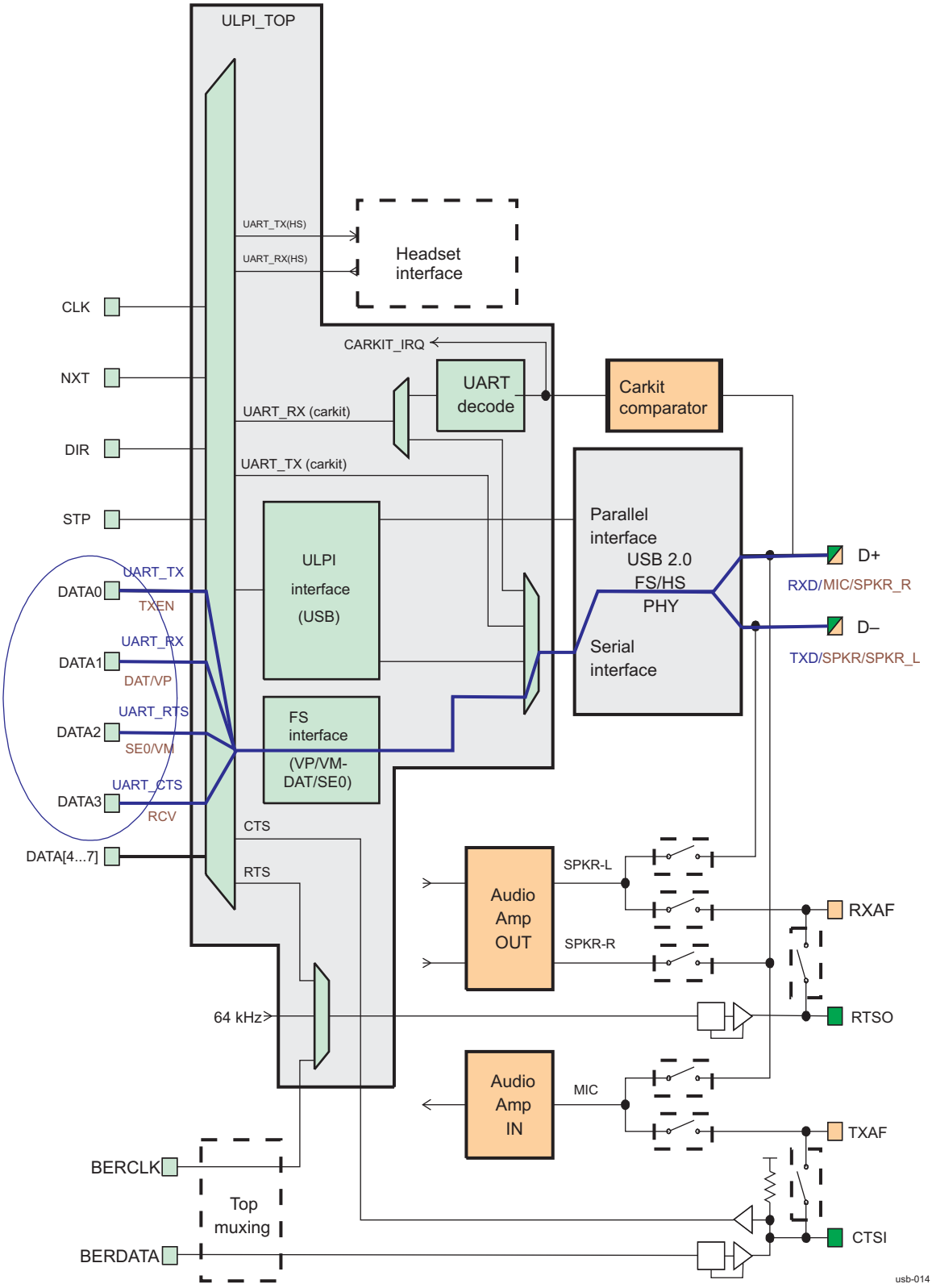
Table 14-4 lists the 3-pin serial mode mapping for USB ULPI. Figure 14-12 shows the 3-pin and 4-pin serial modes for USB ULPI and CEA-2011.

Table 14-4. USB ULPI 3-Pin Serial Mode Pin Mapping

ULPI Data Bit	Direction (1)	Description
DATA[0]	I	Active high transmit enable (TXEN)
DATA[1]	I/O	Transmit/receive differential data to/from D+/D− (DAT)
DATA[2]	I/O	Transmit/receive SE0 to/from D+/D−
DATA[3]	O	Active high interrupt (INT)

(1) I = Input, O = Output

Figure 14-12. USB ULPI and CEA-2011 3-Pin and 4-Pin Serial Modes



14.4.1.3 USB ULPI 4-Pin Serial Mode

In USB ULPI 4-pin serial mode, the ULPI data bus is redefined as a 4-pin serial interface using VP/VM encoding, as defined in the ULPI specification. VP/VM encoding is used to exchange data through a direct access to the FS/LS analog transmitter and receiver (see Figure 14-12). In this mode, the RCV signal is mapped behind DATA[3].

Table 14-5 lists the USB ULPI 4-pin serial mode pin mapping.

This mode supports only USB FS and LS transfers.

Table 14-5. USB ULPI 4-Pin Serial Mode Pin Mapping

ULPI Data Bit	Direction (1)	Description
DATA[0]	I	Active high transmit enable (TXEN)
DATA[1]	I/O	Transmit/receive single-ended data to/from D+ (VP)
DATA[2]	I/O	Transmit/receive single-ended data to/from D− (VM)
DATA[3]	O	Receive differential data from D+/D− (RCV)

(1) I = Input, O = Output

14.4.1.4 USB ULPI 4-Pin Serial Mode Compliant With OMAP2430C ULPI Port Mapping

USB ULPI 4-pin serial mode compliant with OMAP2430C ULPI port mapping is essentially the same mode as defined in Section 14.4.1.3, *USB ULPI 4-Pin Serial Mode*. In this mode, the RCV signal is mapped behind DATA[6] by setting the OTHER_IFC_CTRL2[2] ULPI_4PIN_2430 bit to 1.

Because the OMAP2430C uses an active low transmit enable signal, the OTHER_IFC_CTRL2[3] ULPI_TXEN_POL bit is set to 1.

Table 14-6 lists the USB ULPI 4-pin serial mode for OMAP2430C pin mapping.

Table 14-6. USB ULPI 4-Pin Serial Mode for OMAP2430C Pin Mapping

ULPI Data Bit	Direction (1)	Description
DATA[0]	I	Active low transmit enable (TXEN_) assuming ULPI_TXEN_POL = 1
DATA[1]	I/O	Transmit/receive single-ended data to/from D+ (VP)
DATA[2]	I/O	Transmit/receive single-ended data to/from D− (VM)
DATA[6]	O	Receive differential data from D+/D− (RCV)

(1) I = Input, O = Output

14.4.1.5 USB CEA-2011 3-Pin Serial Mode

USB CEA-2011 3-pin serial mode supports only USB FS and LS transfers.

In this mode, the ULPI data bus is redefined as a 3-pin serial interface using DAT/SE0 encoding, which is used to exchange data through a direct access to the FS/LS analog transmitter and receiver.

The functionality of the ULPI data pins complies with the CEA-2011 serial mode defined in the CEA-2011 specification (also see Figure 14-12).

In this mode, it is possible to use the DATA[2] pin as interrupt output. For more information, see Section 14.4.6, *Interrupts*.

Table 14-7 lists the 3-pin serial mode pin mapping for the USB CEA-2011.

Table 14-7. USB CEA-2011 3-Pin Serial Mode Pin Mapping

ULPI Data Bit	Direction (1)	Description
DATA[0]	I/O	Transmit/receive SE0 to/from D+/D−
DATA[1]	I/O	Transmit/receive differential data to/from D+/D− (DAT)
DATA[2]	I/O	Active low transmit enable input/active low interrupt output (OE_/INT_)

(1) I = Input, O = Output

14.4.1.6 USB CEA-2011 4-Pin Serial Mode

USB CEA-2011 4-pin serial mode supports only USB FS and LS transfers.

In this mode, the ULPI data bus is redefined as a 4-pin serial interface using VP/VM encoding compliant with the CEA-2011 serial mode defined in the CEA-2011 specification, which is used to exchange data through a direct access to the FS/LS analog transmitter and receiver (see Figure 14-12).

In this mode, it is possible to use the DATA[2] pin as interrupt output. For more information, see Section 14.4.6, *Interrupts*.

Table 14-8 lists the 4-pin serial mode pin mapping for the USB CEA-2011.

Table 14-8. USB CEA-2011 4-Pin Serial Mode Pin Mapping

ULPI Data Bit	Direction (1)	Description
DATA[0]	I/O	Transmit/receive single-ended data to/from D− (VM)
DATA[1]	I/O	Transmit/receive single-ended data to/from D+ (VP)
DATA[2]	I/O	Active low transmit enable input/active low interrupt output (OE_/INT_)
DATA[3]	O	Receive differential data from D+/D− (RCV)

(1) I = Input, O = Output

14.4.1.7 CEA-936-A Carkit UART and Audio Mode

CEA-936-A carkit UART and audio mode lets the LINK communicate through the USB PHY with a remote carkit, as defined in the CEA-936-A specification.

In this mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter and receiver.

UART data are sent/received on the USB D+/D− pads. D+/D− are also used in this mode to carry audio in/out signals. The audio/UART selection is controlled by the PSM.

Several audio configurations are possible:

- Audio mono out and microphone in
- Audio mono out and microphone in and DDA
- Audio stereo out

The audio module must be enabled and configured before enabling this mode.

For a detailed description of the PSM, see Section 14.4.9, *CEA-936-A PSM*.

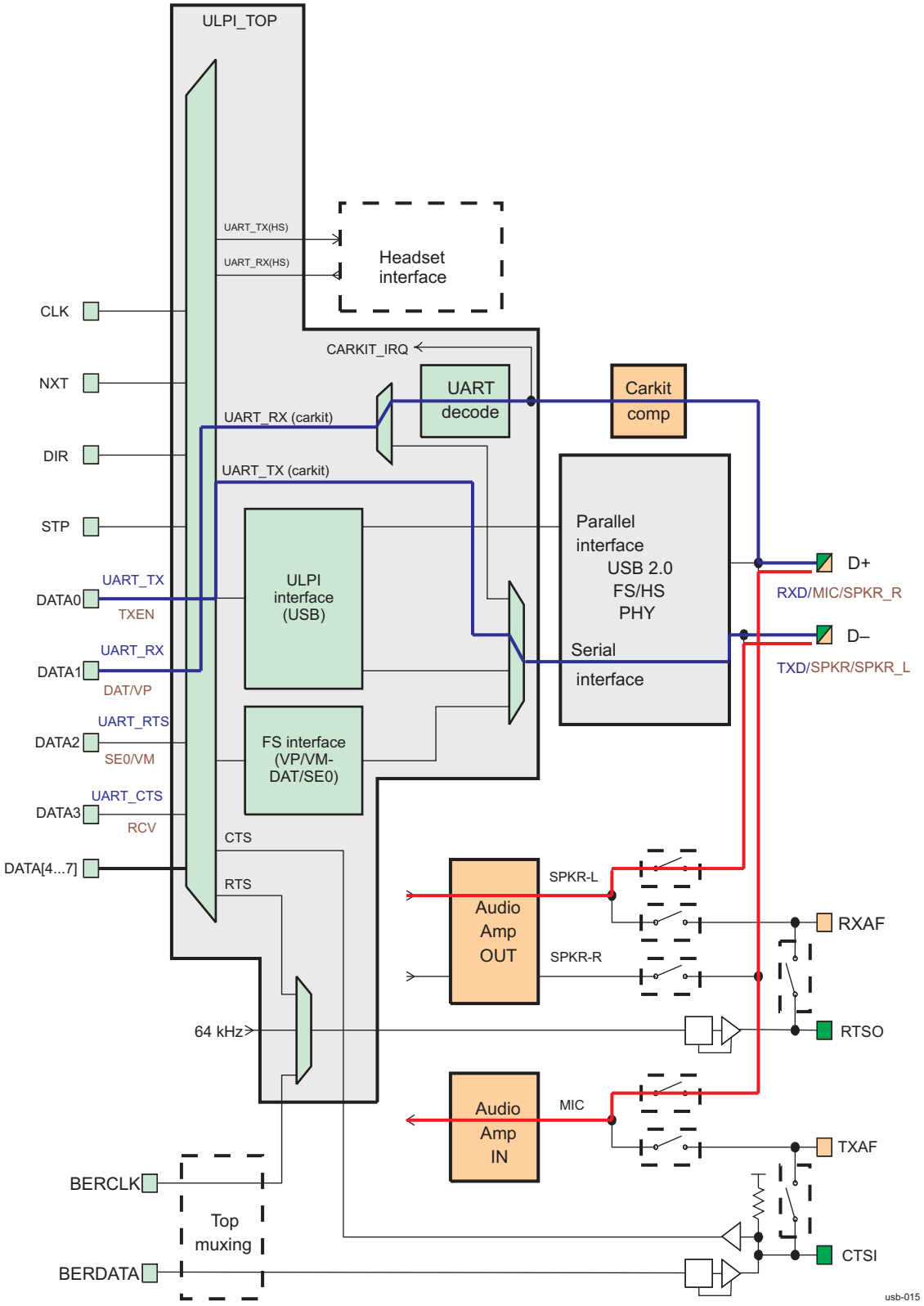
Table 14-9 lists the pin mapping for the CEA-936-A carkit UART and audio mode. Figure 14-13 shows the CEA-936-A carkit UART and audio mode.

Table 14-9. CEA-936-A Carkit UART and Audio Mode Pin Mapping

ULPI Data Bit	Direction (1)	Description
DATA[0]	I	Transmit UART data on D−
DATA[1]	I/O	Receive UART data from D+

(1) I = Input, O = Output

Figure 14-13. CEA-936-A Carkit UART and Audio Mode



14.4.1.8 Free Headset UART

In free headset UART mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through direct access to two 3.1-V-capable I/O pads (UART1.TXD/UART1.RXD).

For correct routing of the UART signals, set the MCPC_CTRL[0] HS_UART bit to 1.

The transmit data output on UART1.TXD is open-drain that requires an external pullup to between 1.8 V and 3.3 V.

The receive data on UART1.RXD is provided from an external open-drain buffer; therefore, an internal maximum 10-kΩ pullup resistor is provided in the device.

To configure these two pins, write 0x00 to the INTBR_PMBR2 register and write 0x02 to the GPIOPUPDCTR3 register (see Chapter 11, *General-Purpose Inputs/Outputs*). For both pads, the maximum specified operating frequency is 3 MHz.

Table 14-10 lists the free headset UART pin mapping.

Figure 14-14 shows the free headset UART mode in general, and Figure 14-15 shows it in detail.

Table 14-10. Free Headset UART Pin Mapping

ULPI Data Bit	Direction [1]	Description
DATA[0]	I	Transmit UART data on UART1.TXD.
DATA[1]	O	Receive UART data from UART1.RXD.

[1] I = Input, O = Output

Figure 14-14. Free Headset UART Mode (General)

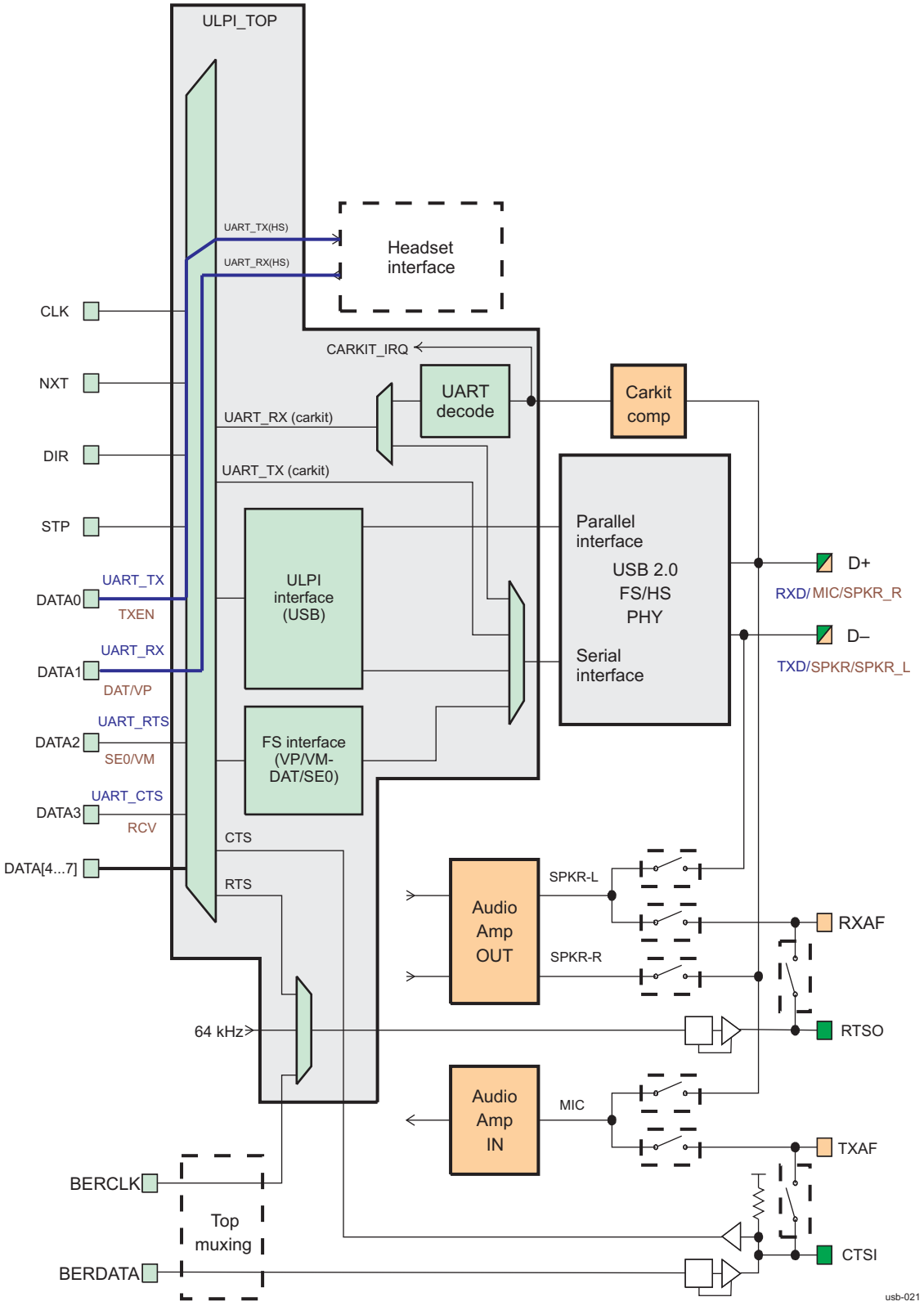
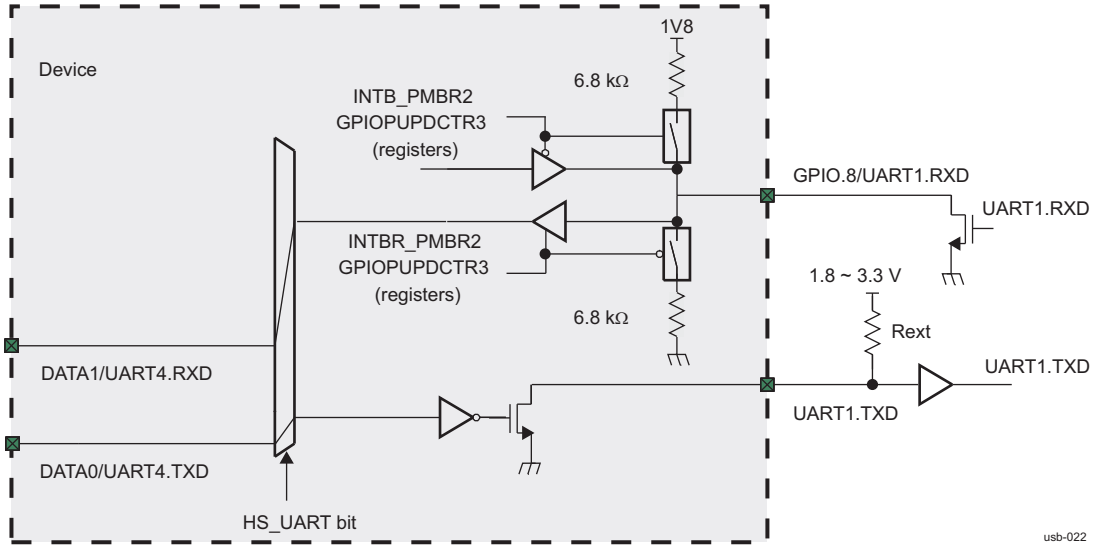


Figure 14-15. Free Headset UART Mode (Detailed)



14.4.1.9 BER and UART

In BER + UART mode, the ULPI data bus is redefined as a 2-pin UART interface. UART data are sent/received on the USB D+/D− pads. Simultaneously, the paths from the BERCLK/BERDATA pads to the RTS/CTS open-drain pads are enabled.

The CTSI pullup is automatically disconnected when BER mode is entered, regardless of the state of the CTS_NPU register.

BERDATA and BERCLK are input to the device through multiplexing of the JTAG.TDI and JTAG.TCK pins, respectively, on 1.8-V VIO supply; they are output from the device through multiplexing of the CTSI and RTSO pins, respectively, on an external supply of from 1.8 to ~3.1 V using open-drain nMOS buffers.

BERCLK is routed from the JTAG.TCK pin to the RTSO pin when EXTSWR = 1. BERDATA is routed from the JTAG.TDI pin to the CTSI pin when EXTSWC = 1 in the MCPC_CTRL register.

In summary, the only function the device provides for BER is level-shifting BERCLK and BERDATA from VDD_IO to an external supply from 1.8 to ~3.1 V.

Figure 14-16 shows BER and UART mode in general. Figure 14-17 shows the BERCLK data path in detail. Figure 14-18 shows the BERDATA data path in detail.

Table 14-11 lists the BER and UART pin mapping.

Table 14-11. BER and UART Pin Mapping

ULPI Data Bit	Direction (1)	Description
DATA[0]	I	Transmit UART data on D−.
DATA[1]	O	Receive UART data from D+.

(1) I = Input, O = Output

Figure 14-16. BER and UART (General)

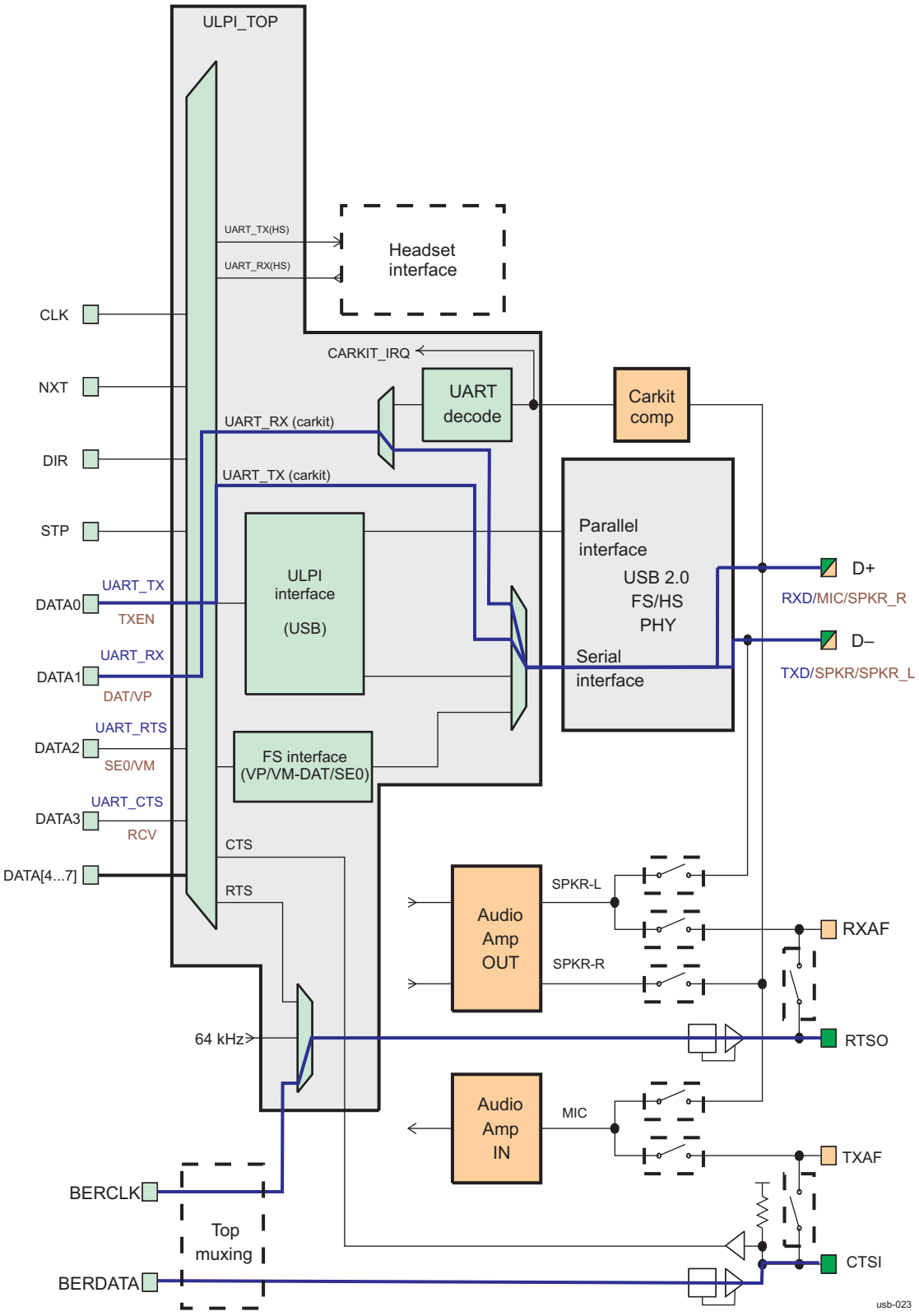


Figure 14-17. BERCLK Data Path

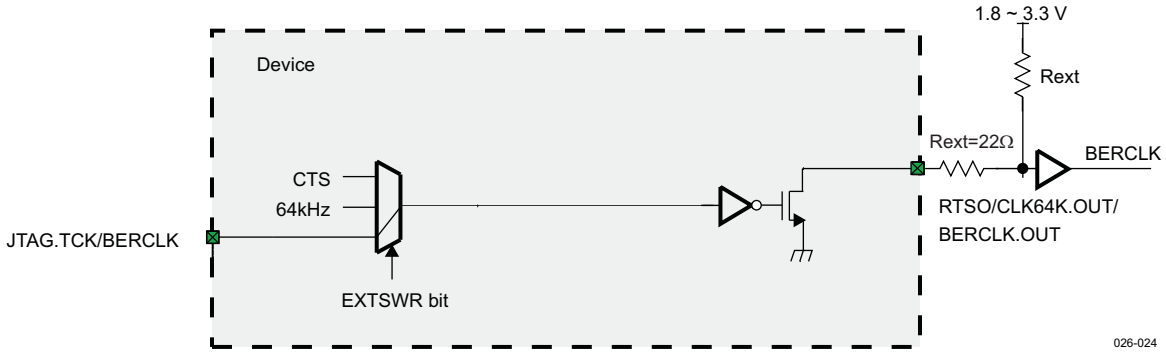
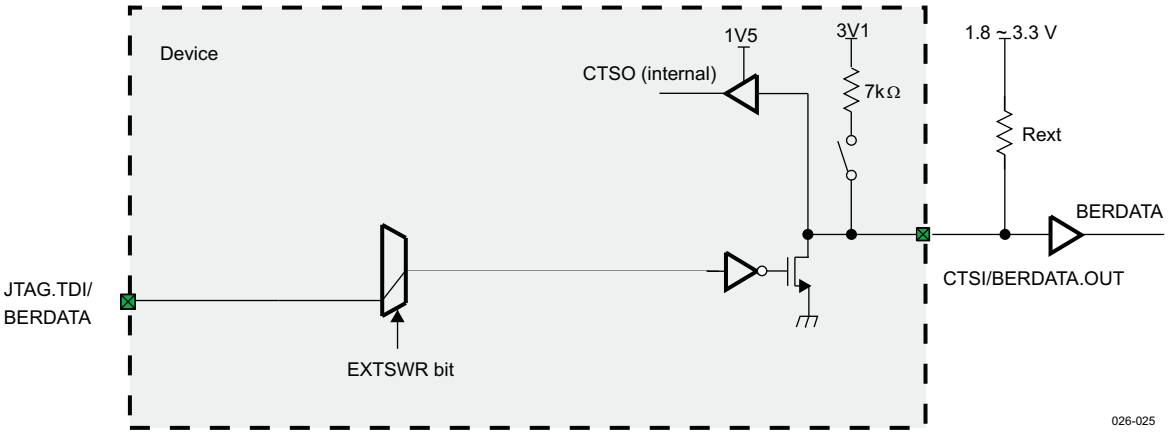


Figure 14-18. BERDATA Data Path



NOTE: The maximum operating frequency for the CTSI and RTSO output buffers is 3 MHz.

14.4.1.10 HiZ ULPI

In HiZ ULPI mode, the complete ULPI interface (data and control pins) is set in high-impedance state. This mode can be used to multiplex a separate interface on the ULPI pads (for example, a GPIO interface) outside the USB subchip.

To tristate all pins, set the OTHER_IFC_CTRL HIZ_ULPI bit to 1.

If it is necessary to shut down the DPLL, the STP signal is internally tied low by setting the OTHER_IFC_CTRL2 ULPI_STP_LOW bit to 1 before requesting the DPLL to idle. This is done to prevent the creation of a wake-up condition of the DPLL.

14.4.1.11 HiZ ULPI with 60-MHz Clock OUT

HiZ ULPI with 60-MHz clock OUT mode is similar to HiZ ULPI mode, except that the UCLK pin is not tristated and outputs the 60-MHz clock (DPLL is on).

To tristate all pins except UCLK, set the OTHER_ IFC_CTRL HIZ_ULPI_60MHZ bit to 1.

14.4.1.12 USB Low-Power Mode

The USB PHY can be put in low-power mode when the FUNC_CTRL[6] SUSPENDM bit is set to 0. In this case, all blocks (except the FS receiver, the OTG comparators, and the ULPI interface pins) are powered down.

In low-power mode, the DPLL clock is not available, which means that register access is not possible.

14.4.2 Mode Multiplexing Control

Functional modes are handled by the UART_USB_MUX block, which redefines the ULPI data bus and routes the signals to the selected connector (USB/CARKIT). These modes are entered by configuring the REGISTER_SET block through the OCP or ULPI interface.

Figure 14-19 shows USB/UART mode multiplexing. Table 14-12 lists USB mode settings, and Table 14-13 lists other mode settings.

Figure 14-19. USB/UART Mode Multiplexing

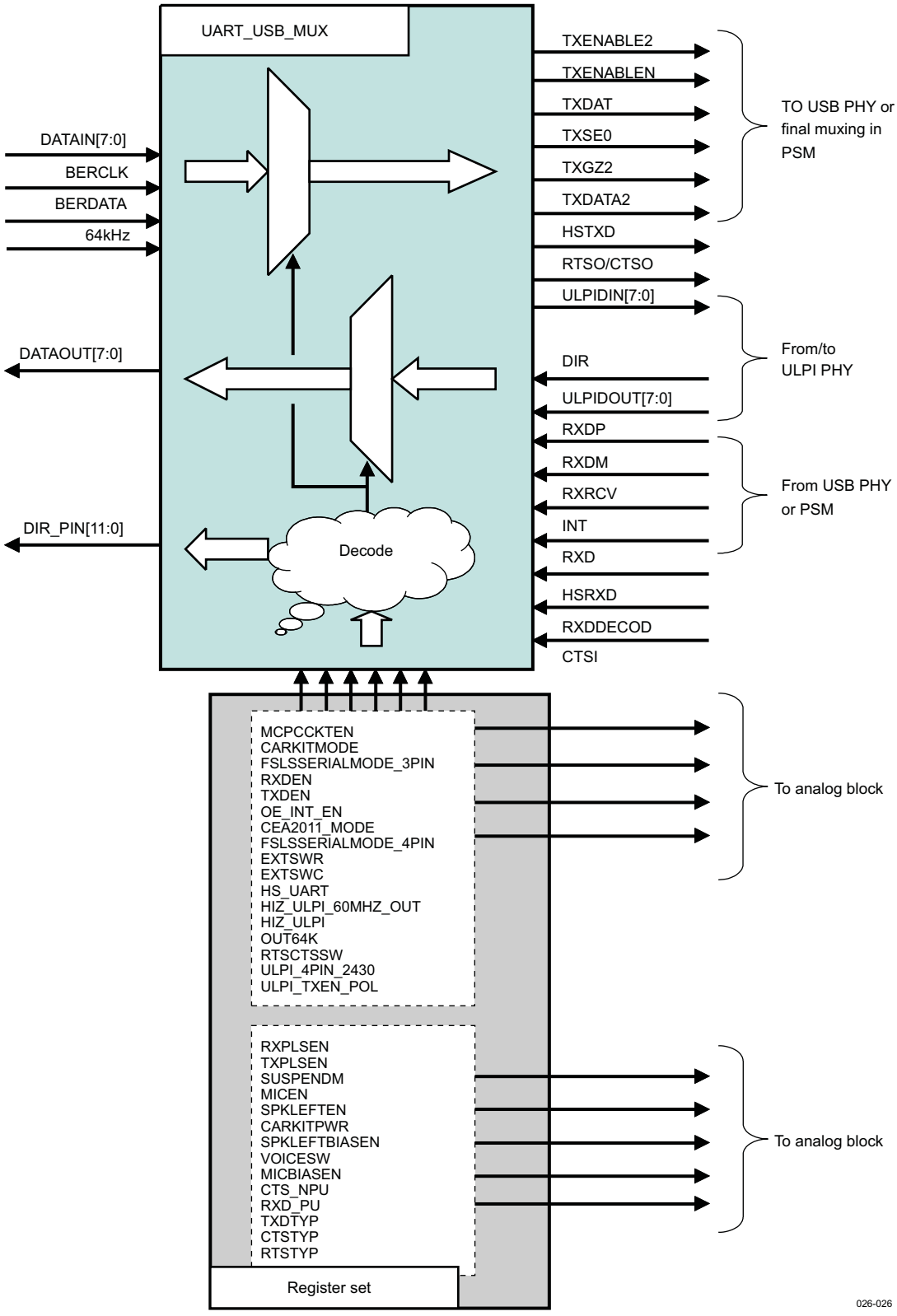


Table 14-12. USB Mode Settings

Address	Register	Bit Name	Bit	USB ULPI	USB ULPI 3 Pins	USB ULPI 4 Pins	USB CEA-2011 4 Pins for OMAP 2430C	USB CEA-2011 3 Pins	USB CEA-2011 4 Pins
0x07	IFC_CTRL	CARKITMODE	2	0	0	0	0	0	0
0x07	IFC_CTRL	FSLSSERIALMODE_3PIN	1	0	1	1	1	1	1
0x19	CARKIT_CTRL	MICEN	6	0	0	0	0	0	0
0x19	CARKIT_CTRL	SPKLEFTEN	4	0	0	0	0	0	0
0x19	CARKIT_CTRL	RXDEN	3	0	0	0	0	0	0
0x19	CARKIT_CTRL	TXDEN	2	0	0	0	0	0	0
0x19	CARKIT_CTRL	CARKITPWR	0	0	0	0	0	0	0
0x22	CARKIT_PLS_CTRL	SPKRLEFTBIASEN	2	0	0	0	0	0	0
0x22	CARKIT_PLS_ CTRL	RXPLSEN	1	0	0	0	0	0	0
0x22	CARKIT_PLS_ CTRL	TXPLSEN	0	0	0	0	0	0	0
0x83	OTHER_IFC_CTRL	OE_INT_EN	6	0	0	0	0	OE_INT_EN	OE_INT_EN
0x83	OTHER_IFC_CTRL	CEA2011_mode	5	0	0	0	0	1	1
0x83	OTHER_IFC_CTRL	FSLSSERIALMODE_4PIN	4	0	0	1	0	0	1
0x83	OTHER_IFC_CTRL	HIZ_ULPI_60MHZ_OUT	3	0	0	0	0	0	0
0x83	OTHER_IFC_CTRL	HIZ_ULPI	2	0	0	0	0	0	0
0xAF	OTHER_IFC_CTRL2	ULPI_4PIN_2430		0	0	0	1	0	0
0xAF	OTHER_IFC_CTRL2	ULPI_TXEN_POL		0	0	0	1	0	0

Table 14-13. Other Mode Settings

Address	Register	Bit Name	Bit	CEA Carkit UART + Audio	Free Headset UART	BER + UART	HiZ ULPI	60-MHz Clock + HiZ ULPI
0x07	IFC_CTRL	CARKITMODE	2	1	0	0	0	0
0x07	IFC_CTRL	FSLSSERIALMODE_3PIN	1	0	0	0	0	0
0x19	CARKIT_CTRL	MICEN	6	1	0	0	0	0
0x19	CARKIT_CTRL	SPKLEFTEN	4	1	0	0	0	0
0x19	CARKIT_CTRL	RXDEN	3	1	0	0	0	0
0x19	CARKIT_CTRL	TXDEN	2	1	0	0	0	0
0x19	CARKIT_CTRL	CARKITPWR	0	1	0	0	0	0
0x22	CARKIT_PLS_CTRL	SPKRLEFTBIASEN	2	1	0	0	0	0
0x22	CARKIT_PLS_ CTRL	RXPLSEN	1	1	0	0	0	0
0x22	CARKIT_PLS_ CTRL	TXPLSEN	0	1	0	0	0	0
0x83	OTHER_IFC_CTRL	OE_INT_EN	6	0	0	0	0	0

Table 14-13. Other Mode Settings (continued)

Address	Register	Bit Name	Bit	CEA Carkit UART + Audio	Free Headset UART	BER + UART	HiZ ULPI	60-MHz Clock + HiZ ULPI
0x83	OTHER_IFC_CTRL	CEA2011_mode	5	0	0	0	0	0
0x83	OTHER_IFC_CTRL	FSLSSERIALMODE_4PIN	4	0	0	0	0	0
0x83	OTHER_IFC_CTRL	HIZ_ULPI_60MHZ_OUT	3	0	0	0	0	1
0x83	OTHER_IFC_CTRL	HIZ_ULPI	2	0	0	0	1	0
0xAF	OTHER_IFC_CTRL2	ULPI_4PIN_2430	3	0	0	0	0	0
0xAF	OTHER_IFC_CTRL2	ULPI_TXEN_POL	2	0	0	0	0	0

14.4.3 Register Access and Arbitration Scheme

The USB registers can be accessed two ways:

- Through the ULPI bus using a TX CMD as a RegWrite or a RegRead command
- Through the OCP interface using an I^2C access

All USB registers can be accessed by the OCP or the ULPI interfaces, except for a few OCP-only registers (PHY_PWR_CTRL, PHY_CLK_CTRL, and PHY_CLK_CTRL_STS) that control the register dual-access mechanism or the USB power-saving features.

All common registers are in the 60-MHz UTMI clock domain and require the USB PHY DPLL to be waked up before any ULPI or I^2C access is attempted. Therefore, the PHY LDOs must also be powered up.

In low-power mode (the FUNC_CTRL[6] SUSPENDM bit is low), the DPLL clock is not available, so register access is not possible.

Also, the clock-suspend function is enabled (the IFC_CTRL[3] CLOCKSUSPENDM bit is low) and the DPLL clock is not powered when the device enters serial or carkit mode, so register access is not possible in these modes.

By default, the register set is allocated to the OCP interface, but when a ULPI access is detected, the register is automatically reallocated to the ULPI until the end of the access.

CAUTION

Concurrent accesses from the ULPI and the OCP are not supported; they produce nonrecoverable errors.

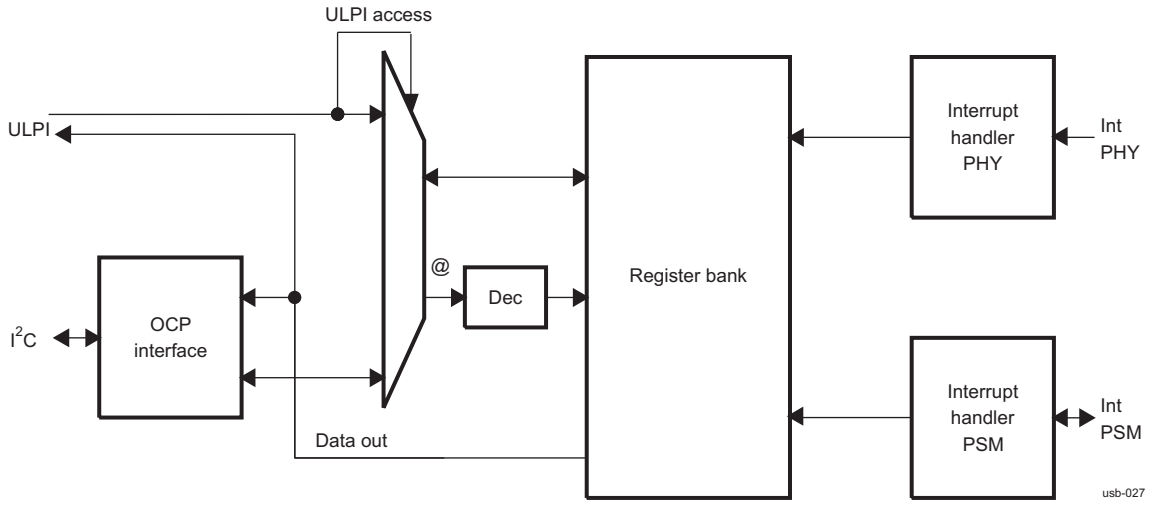
Register addresses do not have to be the same to create a register address conflict. Such an error is reported as a ULPI_12C_CONFLICT_ERROR interrupt, if enabled, and the register content must be considered corrupt.

To avoid conflict, the host software implements a semaphore handshake between the I^2C and ULPI accesses, as follows:

- Wait for an I^2C acknowledgement (ACK) for the current I^2C access before going to a ULPI access.
- Conversely, wait for a ULPI ACK for the current ULPI access before proceeding with an I^2C access.

Figure 14-20 shows the register arbitration.

Figure 14-20. Register Arbitration Overview



Some USB features require specific sequences to configure registers:

- Put the FUNC_CTRL register last in a programming sequence if the FUNC_CTRL[3] SUSPENDM bit is to be set to 0 (PHY to low power).

Reason: When the PHY is set to low power, the ULPI clock is stopped, making register access impossible.

- Put the IFC_CTRL register last in a programming sequence if the following conditions exist:
  - The I^2C bus is in use.
  - The IFC_CTRL[2] CARKITMODE bit or the IFC_CTRL[1] FSLSSERIALMODE_3PIN bit is set to 1 (active).
  - The IFC_CTRL[3] CLOCKSUSPENDM bit is being set to 0 (inactive).

  Reason: Turning on the CARKIT_MODE bit or the FSLSSERIALMODE_3PIN bit and then setting the CLOCKSUSPENDM bit to 0 turns off the clock, making register access impossible.
- Put the IFC_CTRL register last in a programming sequence if the following conditions exist:
  - ULPI is in use.
  - The IFC_CTRL[2] CARKITMODE bit or the IFC_CTRL[1] FSLSSERIALMODE_3PIN bit is set to 1 (active).

  Reason: After turning on the CARKIT_MODE bit or the FSLSSERIALMODE_3PIN bit, the ULPI is not available for register access.
- Put the OTHER_IFC_CTRL2 register first in a programming sequence if entering USB serial or UART mode.

  Reason: The OTHER_IFC_CTRL2[4] ULPI_STP_LOW bit must be set first.

14.4.4 ULPI Access

The ULPI access procedure follows:

1. Request the PHY DPLL clock by asserting the ULPI STOP signal high (if the PHY DPLL clock is already running, go to Step 3).
2. Wait for the clock to wake up.
3. Begin the register accesses.
4. When the register accesses are complete, and if this clock is no longer needed, request to idle the PHY DPLL clock with the appropriate ULPI command.

14.4.5 OCP Access

The OCP access procedure follows:

1. Request the PHY DPLL clock by setting the PHY_CLK_CTRL[0] REQ_PHY_DPLL_CLK bit.
2. Wait for the clock wakeup signaled by a value of 1 in the PHY_CLK_CTRL_STS[0] PHY_DPLL_LOCK bit.
3. Begin the register accesses.
4. When the register accesses are complete, request to idle the PHY DPLL clock by clearing the REQ_PHY_DPLL_CLK bit.

Clearing the REQ_PHY_DPLL_CLK bit does not disable the PHY DPLL if it is used by the ULPI interface. This bit indicates only that the PHY DPLL clock is needed for OCP accesses.

If set, the PHY_CLK_CTRL[2] CLOCKGATING_EN bit provides an additional power-saving feature by autogating the 60-MHz clock to the registers when they are not accessed.

14.4.6 Interrupts

The USB subsystem supports 24 edge-triggered interrupts.

The subsystem embeds a customized secondary interrupt handler (SIH) that receives incoming nonmasked events and updates the corresponding LATCH and STATUS registers.

For each interrupt source, a set of interrupt-enable registers is defined. They can be any of the following:

- Enable falling-edge event detection
- Enable rising-edge event detection
- Enable edge event detection

14.4.6.1 Interrupt Register Definition

This section describes the interrupt registers.

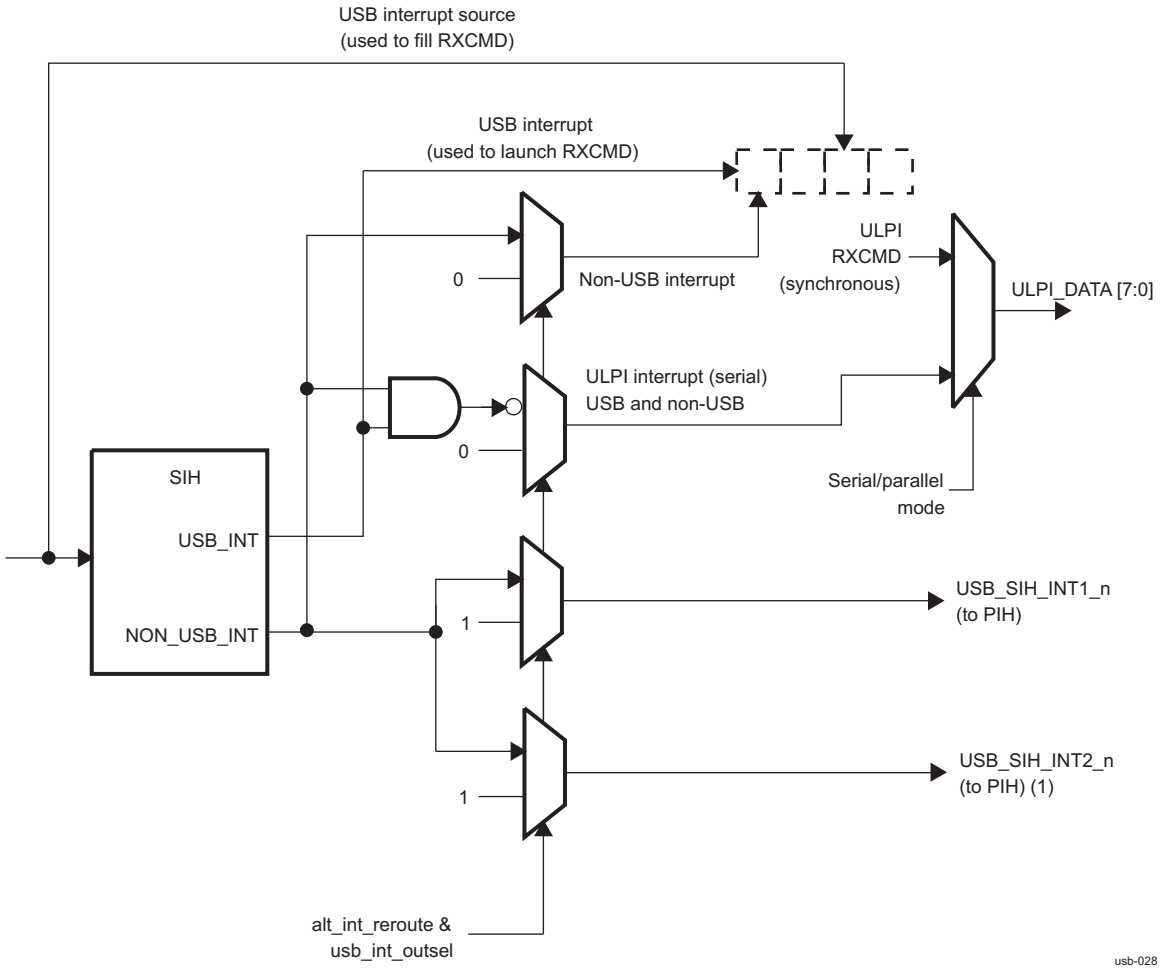
- Interrupt enable rising register: Enables the notification of an event when the corresponding signal goes from low to high (acts as a mask rising event when set low).
- Interrupt enable falling register: Enables the notification of an event when the corresponding signal goes from high to low (acts as a mask falling event when set low).
- Interrupt enable register: Enables the notification of an event when the corresponding signal changes (acts as a mask event when set low).
- Interrupt status register: Indicates the current value of the interrupt source signal (never masked). This register is read-only.
- Interrupt latch register: Set when a nonmasked event occurs on the corresponding signal. This register is read-only and is cleared automatically on a read access.

If at least one nonmasked interrupt occurs, the SIH asserts the subsystem IRQ line. This line is outgoing to one of the following ports:

- PIH/int1_n signal
- ULPI port:
  - As an active high DAT2 or DAT3 pin, in USB serial mode or in carkit mode
  - As an RX command in USB synchronous mode: ULPI/DATA(7:0) port in USB synchronous mode (the interrupt is sent as an RX command)

Figure 14-21 is an overview of USB interrupt routing.

Figure 14-21. USB Interrupt Routing Overview



(1) INT2 is not available.

When an interrupt event occurs, if int1_n is selected, the corresponding PISRx register in the PIH is updated, and the PIH asserts low the po_intx_n interrupt line to the host.

If the ULPI port is selected, the ULPI DATA bus is a direct interrupt line to the host.

All interrupts are acknowledged by a read access on the corresponding LATCH register; the entire content of this register is then reset. An interrupt can be acknowledged by reading through the ULPI interface or the OCP interface.

The routing of the interrupt line is controlled by the following bits:

- FUNC_CTRL[6] SUSPENDM
- OTHER_IFC_CTRL[0] ALT_INT_REROUTE, OTHER_IFC_CTRL[6] OE_INT_EN, and OTHER_IFC_CTRL[5] CEA_2011_MODE
- OTHER_IFC_CTRL2[1:0] USB_INT_OUTSEL

Table 14-14 lists the decoding of the interrupt routing control registers.

Table 14-14. Interrupt Routing Control

Mode	ALT_INT_ REROUTE	USB_INT_ OUTSEL (1)	CEA2011_ MODE (1)	OE_INT_EN (1)	SUSPENDM (1)	Interrupts Signaled On:	Comments
Synchronous	0	XX	X	X	X	RX CMD	ULPI RX command only. Non-USB interrupts signaled with ALT_INT bit set in the RX CMD.
	1	00	X	X	X	RX CMD + INT1 signal	ULPI RX command only for USB interrupts (ALT_IN bit never set). Non-USB interrupts signaled on INT1 signal.
	1	01	X	X	X	RX CMD + INT2 signal	ULPI RX command only for USB interrupts. Non-USB interrupts signaled on INT2 signal.
Serial	0	XX	0	X	X	DAT3 pin	All interrupts signaled on ULPI DAT3 pin (INT) pin: Active high interrupt ULPI STD-compatible
	0	XX	1	1	0	DAT2 pin	All interrupts signaled on ULPI DAT2 pin. DAT2 = INT/output − active low interrupt CEA-2011 STD-compatible
	0	XX	1	1	1	-	No interrupts. DAT2 = OE_ input CEA-2011 STD-compatible
	1	00	X	X	X	INT1 signal	All interrupts signaled to the device interrupt module on INT1 signal.

(1) X = don't care.

Table 14-15 lists the existing interrupts and the associated control in the USB. A more detailed description is in Section 14.5.1, *USB Register Mapping Summary*.

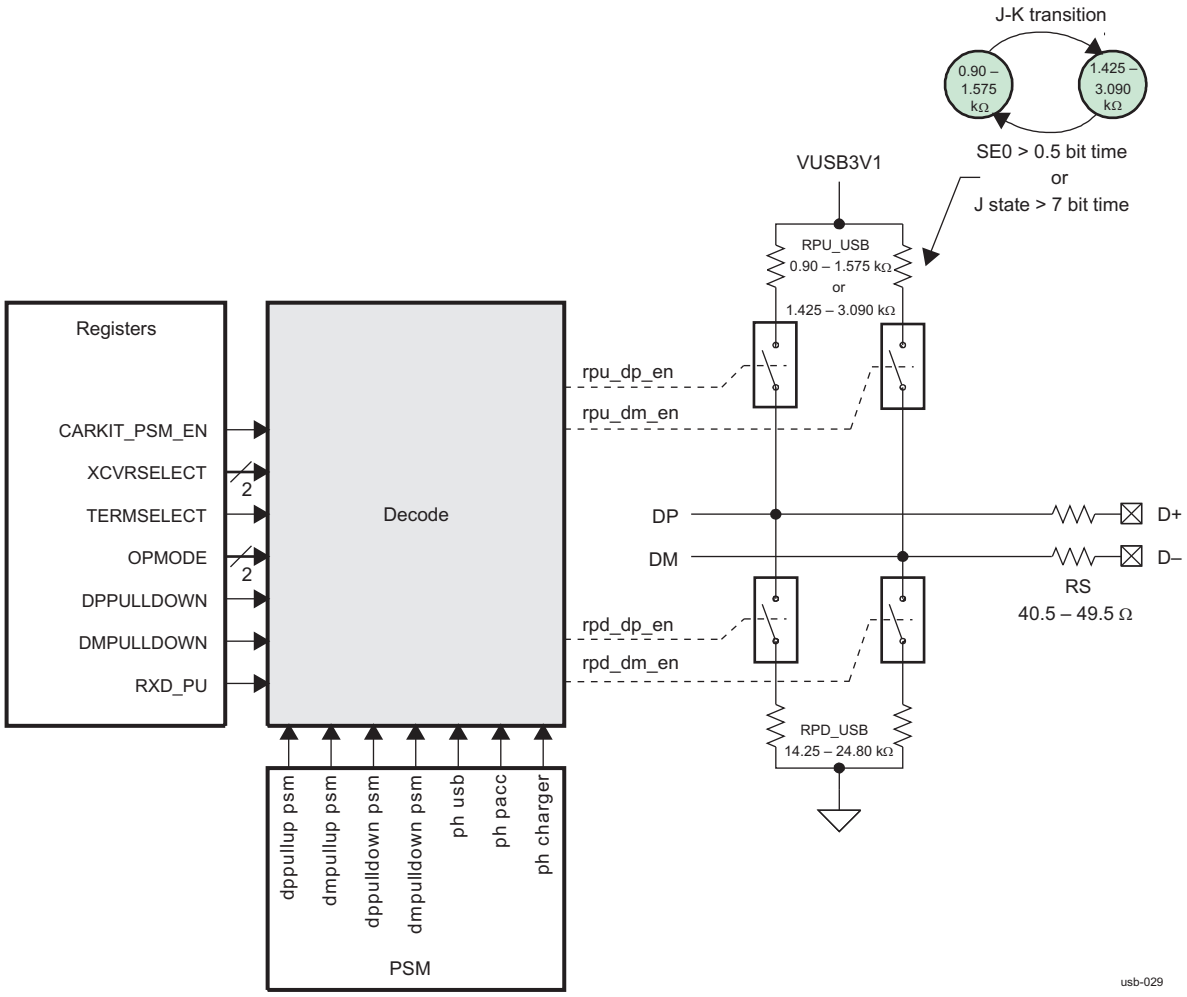
Table 14-15. USB Register Interrupt Summary

Register Group	Interrupt Event Sources	Register INT Enables	@	Register INT Status	@	Register INT Latch	@
1	HOST DISCONNECT VBUSVALID SESSVALID SESSEND IDGND	USB_INT_EN_RISE	0x0D (RW) 0x0E (RS) 0x0F (RC)	USB_INT_STS	0x13	USB_INT_LATCH	0x14
		USB_INT_EN_FALL	0x10 (RW) 0x11 (RS) 0x12 (RC)				
2	IDFLOAT CARINTDET CARDP	CARKIT_INT_EN	0x1D (RW) 0x1E (RS) 0x1F (RC)	CARKIT_INT_STS	0x20	CARKIT_INT_LATCH	0x21
3	ABNORMAL_ STRESS BDIS ACON VB_SESS_VLD	OTHER_INT_EN_RISE	0x86 (RW) 0x87 (RS) 0x88 (RC)	OTHER_INT_STS	0x94	OTHER_INT_LATCH	0x95
		OTHER_INT_EN_FALL	0x89 (RW) 0x8A (RS) 0x8B (RC)				
4	DISCONNECTED CARKIT USB_OTG_B USB_HOST CHARGER PH_ACC PSM_ERROR	CARKIT_SM_1_INT_EN	0x97 (RW) 0x98 (RS) 0x99 (RC)	CARKIT_SM_1_INT_ STS	0x9A	CARKIT_SM_1_INT_ LATCH	0x9B
5	PH_NO_ACK PHONE_UART STEREO_TO_ MONO STOP_PLS_MISS	CARKIT_SM_2_INT_EN	0x9C (RW) 0x9D(RS) 0x9E (RC)	CARKIT_SM_2_INT_ STS	0x9F	CARKIT_SM_2_INT_ LATCH	0xA0
6	ULPI_I2C_ CONFLICT_ ERROR	REG_CTRL_EN	0xB2 (RW) 0xB3 (RS) 0xB4 (RC)	–	–	REG_CTRL_ERROR	0xB5

14.4.7 D+/D– Termination Resistor Control

The USB fully integrates the termination resistors required for USB UART operation. The integrated USB pullup and pulldown resistors comply with the USB ECN 2.0 specification. The integrated 45-Ω HS termination resistors comply with the USB 2.0 specification.

Figure 14-22. D+/D− Termination Resistors



14.4.7.1 USB Mode Without CEA Carkit Support

In USB mode without CEA carkit support, the USB termination resistors are set to the desired signaling mode by the XCVRSELECT, TERMSELECT, and OPMODE bits in the FUNC_CTRL register, and by the DPPULLDOWN and DMPULLDOWN bits in the OTG_CTRL register.

The MCPC_IO_CTRL[3] RXD_PU bit and the CARKIT_SM_CTRL[0] CARKIT_PSM_EN bit must be cleared to 0.

Table 14-16 describes how USB termination resistors are set according to the register bit settings.

14.4.7.2 CEA-936-A Carkit Mode

In CEA carkit mode, when the CARKIT_SM_ CTRL[0] CARKIT_PSM_EN bit = 1, the PSM directly controls the USB pullup and pulldown resistors, except when the PSMs are in the ph_usb, ph_pacc, or ph_charger states.

14.4.7.2.1 All States Except ph_usb or ph_pacc

The PSM takes precedence over the control registers for the carkit and FS transceiver control:

- DPPULLDOWN = dppulldown_psm signal from PSM
- DMPULLDOWN = dmpulldown_psm signal from PSM
- The XCVRSELECT and TERMSELECT values are decoded according to Table 14-16.

Table 14-16. XCVRSELECT and TERMSELECT in States Other Than ph_usb or ph_acc

dmpullup_psm (from PSM)	dppullup_psm (from PSM)	XCVRSELECT	TERMSELECT	XCVRSELECT (PHY Input)	TERMSELECT (PHY Input)
0	0	XCVRSELECT	TERMSELECT	XCVRSELECT	TERMSELECT
0	1	x	xx	01	1
1	0	x	xx	10	1

14.4.7.2.2 ph_usb, ph_pacc, and ph_pacc States

In these states, the control registers take precedence over the PSM signal for the carkit and FS transceiver control:

- DPPULLDOWN = DPPULLDOWN field of the OTG_CTRL register (bit 1)
- DMPULLDOWN = DMPULLDOWN field of the OTG_CTRL register (bit 2)
- XCVRSELECT = XCVRSELECT field of the FUNC_CTRL register (bits 1:0)
- TERMSELECT = TERMSELECT field of the FUNC_CTRL register (bit 2)

14.4.7.3 USB Signaling Mode Register Settings

Table 14-17 lists the valid register settings versus the signaling modes supported by the USB.

Table 14-17. D+/D− Termination Settings Versus Signaling Mode

Signaling Mode	Register Settings or PSM Signals						Resistor Settings				
	Xcvr Select	Term Select	Op Mode	DpPulldown	DmPulldown	RXD_ PU	rpu_ dp_en	rpu_ dm_en	rpd_ dp_en	rpd_ dm_en	hsterm_ en
USB General Settings											
Tristate drivers	xx	x	01	x	x	0	0	0	0	0	0
Power up or VBUS < VSESSEND	01	0	00	1	1	0	0	0	1	1	0
USB Host Settings											
Host chirp	00	0	10	1	1	0	0	0	1	1	1
Host HS	00	0	00	1	1	0	0	0	1	1	1
Host FS	x1	1	00	1	1	0	0	0	1	1	0
Host HS/FS suspend	01	1	00	1	1	0	0	0	1	1	0
Host HS/FS resume	01	1	10	1	1	0	0	0	1	1	0
Host LS	10	1	00	1	1	0	0	0	1	1	0
Host LS suspend	10	1	00	1	1	0	0	0	1	1	0
Host LS resume	10	1	10	1	1	0	0	0	1	1	0
Host Test_J/Test_K	00	0	10	1	1	0	0	0	1	1	1
USB Peripheral Settings											
Peripheral chirp	00	1	10	0	0	0	1	0	0	0	0
Peripheral HS	00	0	00	0	0	0	0	0	0	0	1
Peripheral FA	01	1	00	0	0	0	1	0	0	0	0
Peripheral HS/FS suspend	01	1	00	0	0	0	1	0	0	0	0
Peripheral HS/FS resume	01	1	10	0	0	0	1	0	0	0	0
Peripheral LS	10	1	00	0	0	0	0	1	0	0	0
Peripheral LS suspend	10	1	00	0	0	0	0	1	0	0	0
Peripheral LS resume	10	1	10	0	0	0	0	1	0	0	0
Peripheral Test_J/Test_K	00	0	10	0	0	0	0	0	0	0	1
OTG device, peripheral chirp	00	1	10	0	1	0	1	0	0	1	0
OTG device, peripheral HS	00	0	00	0	1	0	0	0	0	1	1
OTG device, peripheral FS	01	1	00	0	1	0	1	0	0	1	0

Table 14-17. D+/D− Termination Settings Versus Signaling Mode (continued)

Signaling Mode	Register Settings or PSM Signals						Resistor Settings				
	Xcvr Select	Term Select	Op Mode	DpPulldown	DmPulldown	RXD_ PU	rpu_ dp_en	rpu_ dm_en	rpd_ dp_en	rpd_ dm_en	hsterm_ en
USB General Settings											
OTG device, peripheral HS/FS suspend	01	1	00	0	1	0	1	0	0	1	0
OTG device, peripheral HS/FS resume	01	1	10	0	1	0	1	0	0	1	0
OTG device, peripheral Test_J/Test_K	00	0	10	0	1	0	0	0	0	1	1

14.4.8 OTG Support: VBUS and ID Pin Comparators

The OTG block integrates three functions:

- USB plug detection on VBUS and ID
- ID resistor detection
- VBUS level detection

14.4.8.1 VBUS and ID Wake-Up Interrupt

When the device is in wait-on mode, the USB regulators and analog device shared regulators are disabled. Only VRRTC is present to control the main power-management event/power-up sequence. However, the device must wake up when a USB plug event (VBUS plug or ID plug) occurs. For this reason, the OTG block integrates a VBUS wake-up comparator under VRRTC that toggles when VBUS > 0.55 V, and an ID wake-up comparator under VRRTC that toggles when the external resistor connected to the device ID pin is less than 445 kΩ. When one of the two comparators toggles, the power module switches to active mode and a USB presence interrupt is generated in the digital block (USB_PRES = VBUS_PRES or ID_PRES). The plug type (VBUS or ID) is stored in a status register that can be read by the external host processor.

This function is disabled while the device is in backup battery mode.

In case of ID plug detection and no VBUS plug detection, when the device wakes up, the OTG block is turned on and the ID level is detected in the following situations:

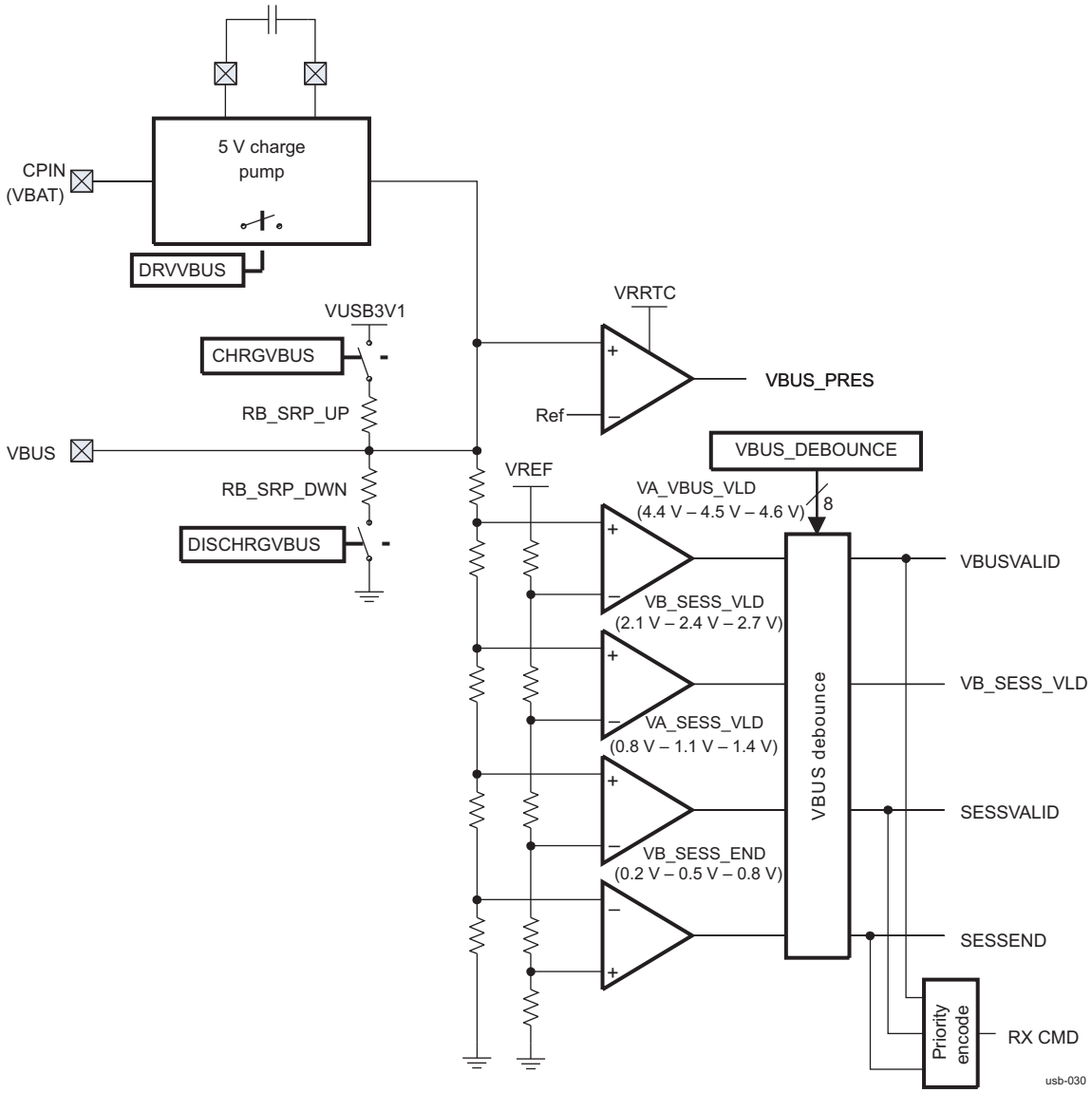
- If ID-to-ground is detected: The device USB is an A-device and the charge pump can be turned on.
- If ID-to-100k is detected: This is an attached CEA-936-A phone-powered accessory that can be powered by the USB charge pump or by switching the BCI external FET from VBAT.
- If ID floating is detected: The device is in a B-device state and the charge pump is not turned on.

In case of VBUS plug detection, when the device wakes up, the OTG block is turned on. The device is recognized as a B-device connected to an A-device or to a CEA-936-A carkit or charger as a function of the ID resistor value.

14.4.8.2 VBUS Pin Monitoring and Control

Figure 14-23 shows VBUS control and detection.

Figure 14-23. VBUS Control and Detection



The charge pump is used to generate the 4.8-V (nominal) VBUS supply from VBAT. For battery voltage higher than 3 V, the charge pump maximum load is specified as 100 mA (at the charge pump output). For battery voltage between 2.7 V and 3 V, the maximum load is limited to 50 mA to ensure the output voltage performance of the charge pump.

The charge pump is controlled by the OTG_CTRL[5] DRVVBUS bit and is turned on when the device USB is required to act as an A-device.

The charge pump relies on a 1-MHz clock from the device clock module; the DRVVBUS bit is used as a request signal for this clock.

The VBUS block also integrates four comparators that generate four interrupts, depending on the VBUS level:

- VB_SESS_END: 0.2 V, 0.5 V, 0.8 V
- VA_SESS_VLD: 0.8 V, 1.1 V, 1.4 V
- VB_SESS_VLD: 2.1 V, 2.4 V, 2.7 V
- VA_VBUS_VLD: 4.4 V, 4.5 V, 4.6 V

The SESSEND_LATCH interrupt corresponds to a VB_SESS_END event. The SESSVALID_LATCH interrupt corresponds to a VA_SESS_VLD event. The VBUSVALID_LATCH interrupt corresponds to a VA_VBUS_VLD event. These three interrupts are in the USB_INT_LATCH register.

The VB_SESS_VLD_LATCH interrupt corresponds to a VB_SESS_VLD event in the OTHER_INT_LATCH register.

In USB synchronous mode, a VBUS voltage state change after debounce triggers a ULPI RX CMD.

The VBUS state field of the ULPI RX CMD is encoded according to Table 14-18.

Table 14-18. Encoded VBUS Voltage State

VBUS State	VBUS Voltage	SESSEND	SESSVALID	VBUSVALID
00	VBUS < VSESSEND	1	0	0
01	VSESSEND ≤ VBUS < VSESSVALID	0	0	0
10	VSESSVALID ≤ VBUS < VvBUSVALID	X	1	0
11	VvBUSVALID ≤ VBUS	X	X	1

The VBUS line is referenced to GND_REF (GND_REF must be connected to the USB cable SHIELD pin).

The VBUS block also integrates the following:

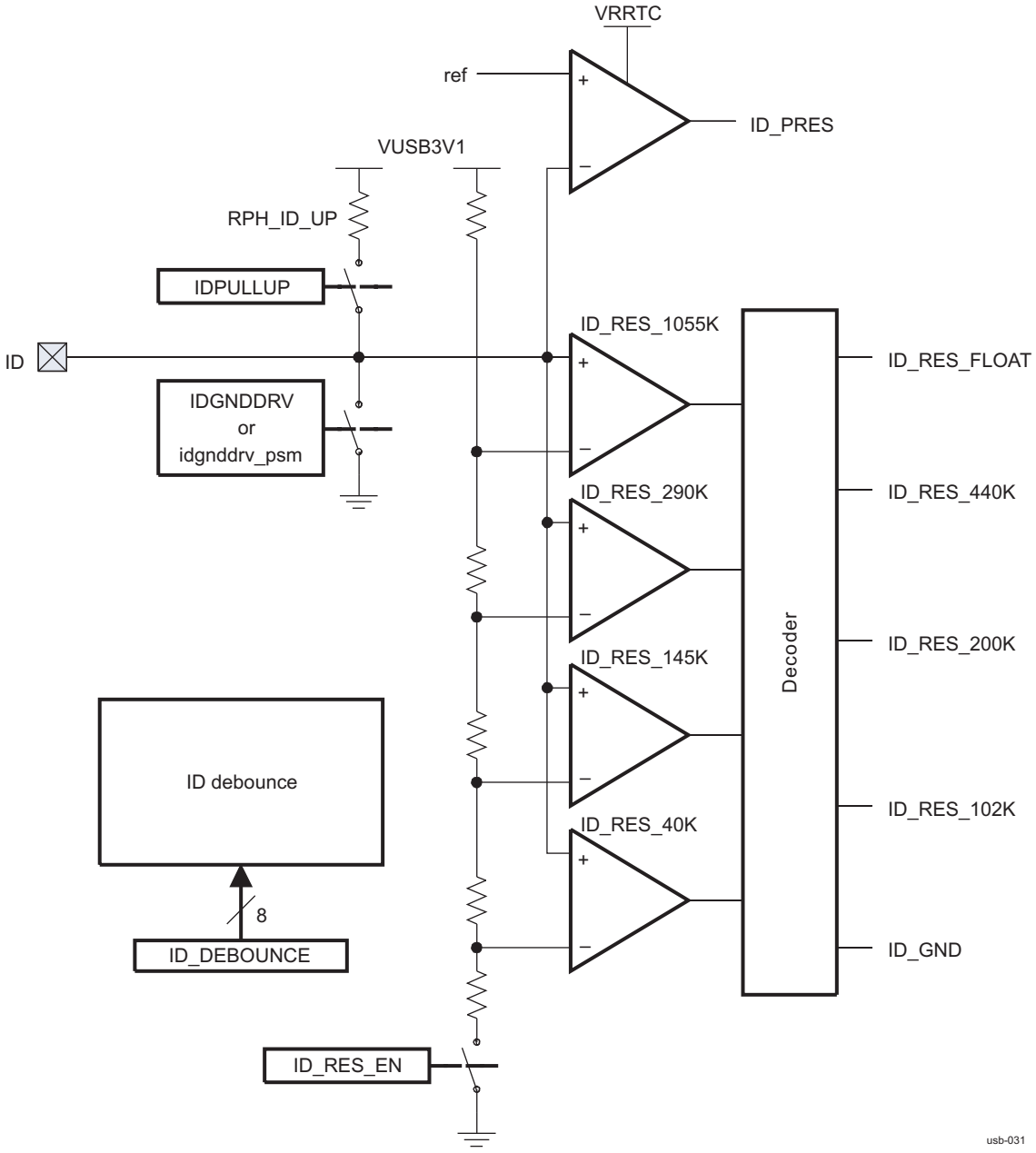
- One switchable pulldown resistor (RA_BUS_IN). When an A-device is powered and not providing VBUS, the A-device must present an input impedance on VBUS of not more than 100kΩ (RA_BUS_IN maximum) to the ground. Here, the A-device responds to the VBUS pulsing method of SR; therefore, the input impedance is not lower than 40 kΩ (RA_BUS_IN minimum) to the ground.
- One switchable pulldown resistor (RB_SRP_DWN) controlled by the OTG_CTRL[3] DISCHRGVBUS bit. Before initiating SRP, an OTG B-device is allowed to discharge VBUS for not more than 100 ms, at a current of not more than 8 mA (IB_DSCHG_IN maximum). This is done by connecting RB_SRP_DWN to the ground.
- One switchable pullup resistor (RB_SRP_UP) controlled by the OTG_CTRL[4] CHRGVBUS bit. SRP starts by pulling up VBUS through RB_SRP_UP to the 3.1-V USB regulator.
- One programmable debouncer controlled by the VBUS_DEBOUNCE register. The debounce function delivers clean interrupts to the interrupt handlers. When a level change is detected on the VBUS line, a counter that holds the VBUS_DEBOUNCE value starts. When the count level is reached, the current value of the VBUS is passed on. During the count time, the previous stable value of the VBUS is maintained.

14.4.8.3 ID Pin Monitoring and Control

ID pin monitoring and control integrates the OTG and CEA-936-A carkit functions relative to the ID pin.

Figure 14-24 shows ID control and detection.

Figure 14-24. ID Control and Detection



Four comparators are implemented to sense the (external) ID resistance to the ground:

- ID_RES_40K detects resistors higher than 40 kΩ (nominal value).
- ID_RES_145K detects resistors higher than 145 kΩ (nominal value).
- ID_RES_290K detects resistors higher than 290 kΩ (nominal value).
- ID_RES_1055K detects resistors higher than 1055 kΩ (nominal value).

Additional logic between these comparators allows the decoding of five statuses and two interrupts:

- ID_GND (OTG purpose – status and interrupt)
- ID_RES_100K (carkit purpose – status only)
- ID_RES_200K (carkit purpose – status only)
- ID_RES_440K (carkit purpose – status only)
- ID_FLOAT (OTG purpose – status and interrupt)

The IDGND_LATCH interrupt is in the USB_INT_LATCH register, and the ID_FLOAT_LATCH interrupt is in the CARKIT_INT_LATCH register.

In the case of a CEA-936-A carkit, the ID resistor-to-ground value status is obtained by reading the ID_STATUS register.

The ID block also integrates the following:

- One switchable ID pullup resistor (RPH_ID_UP) controlled by the OTG_CTRL[0] ID_ PULLUP bit. This resistor is defined between 70 kΩ and 286 kΩ in normal operations and must be asserted to allow ID resistor measurement to occur.
- One ID switch to the ground controlled by IDGNDDRV in the CARKIT_CTRL register when the PSM is disabled or, if it is enabled, in the USB or PACC state; or solely by the PSM when enabled for all other states. This switch generates an interrupt during the 5-wire protocol or requests more current from a 5-wire type 1 charger.
- One programmable debouncer controlled by the ID_DEBOUNCE register. Debouncing delivers clean interrupts to the interrupt handlers. When a level change is detected on the ID line, a counter that holds an ID_DEBOUNCE value starts. When the count level is reached, the current value of the ID is passed on. During the count time, the previous stable value of the ID is maintained.

14.4.8.4 VBAT Monitoring Aspects

If VBAT < 3.3 V, the 3.1-V regulator may not regulate correctly. As a consequence, the 3.1-V regulator output voltage is less than 3 V (and not regulated), so transceiver LS/FS/HS functionality cannot be ensured. In the USB 2.0 standard, the pullup resistor on DP/DM must be connected to a voltage between 3.0 V and 3.6 V. In addition, the LS/FS high state output high voltage (VOH) is specified at 2.8 V minimum (high output level on DP/DM), which is impossible to achieve with an unregulated LDO or with less than 200 mV headroom from the minimum regulated voltage to the PHY output at DP/DM. See the *Universal Serial Bus Specification* document, Chapter 7.3.2.

The first workaround was to switch from VBAT to VBUS (4.4 V; 5.25 V) when the VBAT falling edge crossed 3.3 V (VBAT MADC monitoring result).

However, such switching is permissible only when the USB is configured.

Before being considered configured, the two connected devices must exchange data to deliver a specific address and set up the device (through PHY transceiver communication on DP/DM). To be OTG-compliant, the OTG device must draw less than 150 uA on VBUS. Because LS/FS transceivers consume more than 8 mA worst case, it is impossible to be OTG-compliant while the 3.1-V regulator input is switched to VBUS, and impossible for T2 USB to be functional when the 3.1-V regulator input stays at VBAT while VBAT < 3.3 V (PHY is not functional while 3.1-V regulated voltage is less than 3 V).

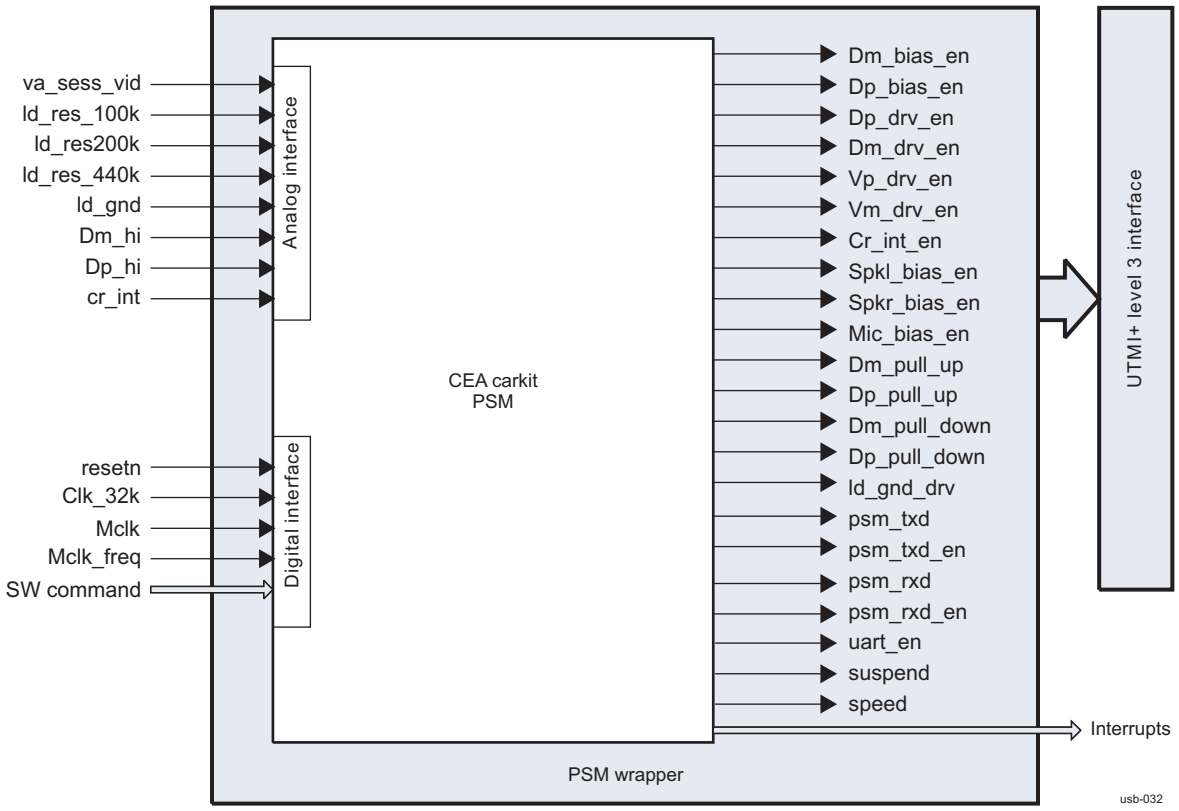
In addition to not being OTG-compliant while switched to VBUS and VBAT < 3.3 V, regulation may not be correct even for peripheral devices only, because a peripheral device must consume less than 8 mA on VBUS, and the transceiver LS/FS/HS consumes more than 8 mA.

To make USB work with VBAT < 3.3 V, switch the 3.1-V regulator from VBAT to VBUS. This causes consumption of more than 8 mA on VBUS.

14.4.9 CEA-936-A PSM

CEA-936-A USB carkit support relies on the PSM in the device USB. Figure 14-25 is the block diagram of the carkit PSM.

Figure 14-25. Carkit PSM Block Diagram



14.4.9.1 Carkit Digital Detailed Description

The following sections describe how the CEA standard is supported by the USB subsystem. The main states are described as important software bit registers and command bytes to send to the carkit. For a complete description of the protocol, see the CEA-936-A specification.

Table 14-19 lists the PSM transition definitions.

Table 14-19. PSM Transition Glossary

Prefix/Suffix	Description
(xxxxxx)	PSM state number
i	Set interrupt cross-reference number (for example, I0 or I1)
ic	Interrupt clear cross-reference number (for example, Ic4) **Note:** icx = All interrupts are cleared.
t	Timing cross-reference number (for example, t1)
to	Timing cross-reference number (for example, to2)
−hold	The signal was held for two cycles of the 32-kHz clock since its generation.
−lv	Denotes a signal level

14.4.9.2 PSM: Connection Sequence State Diagram

Figure 14-26 is the state diagram for the connection sequence for the PSM.

Figure 14-26. PSM Connection Sequence State Diagram

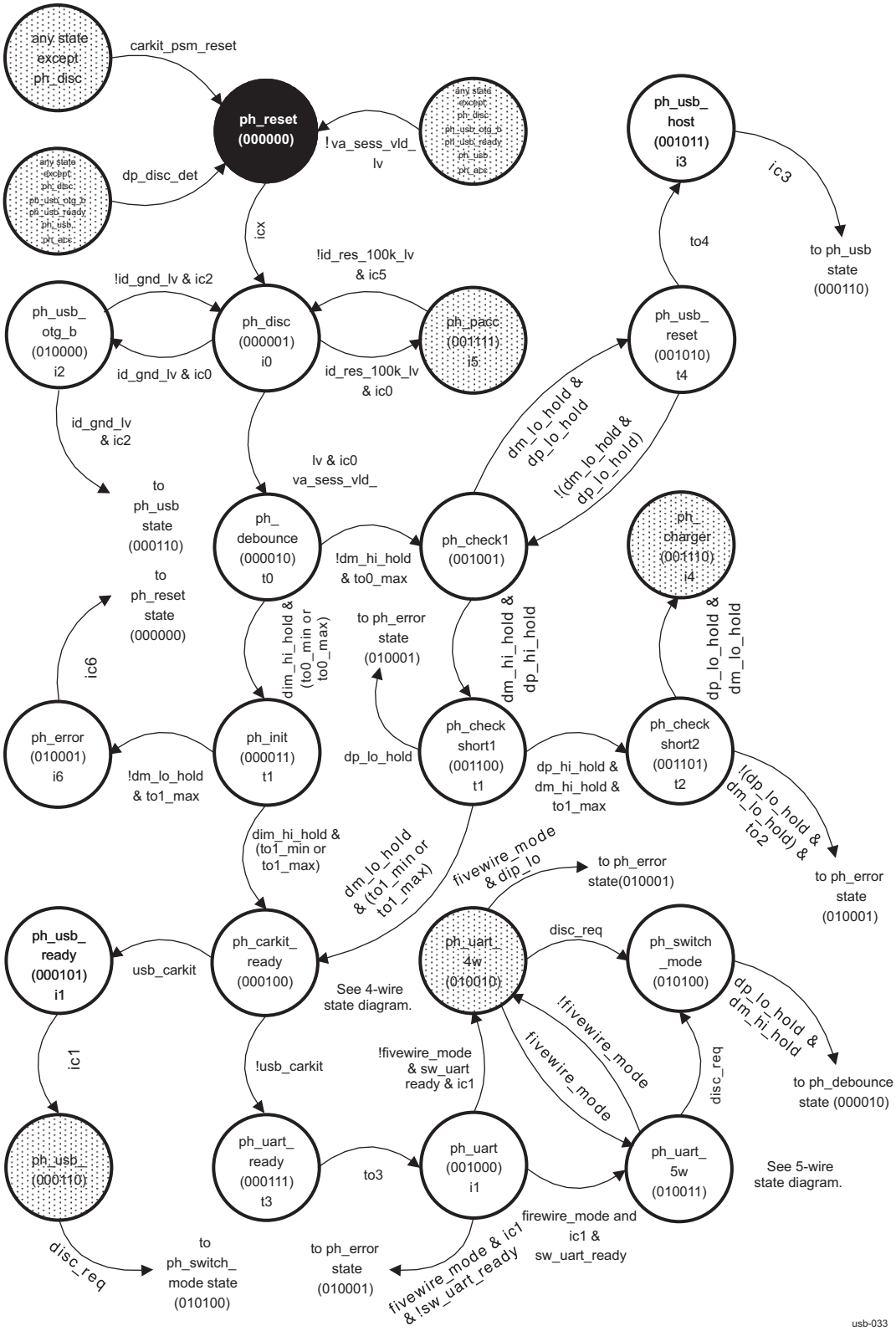


Figure 14-26 describes the handshaking between the device (the phone) and the other device that can be plugged into the phone when it is already powered up.

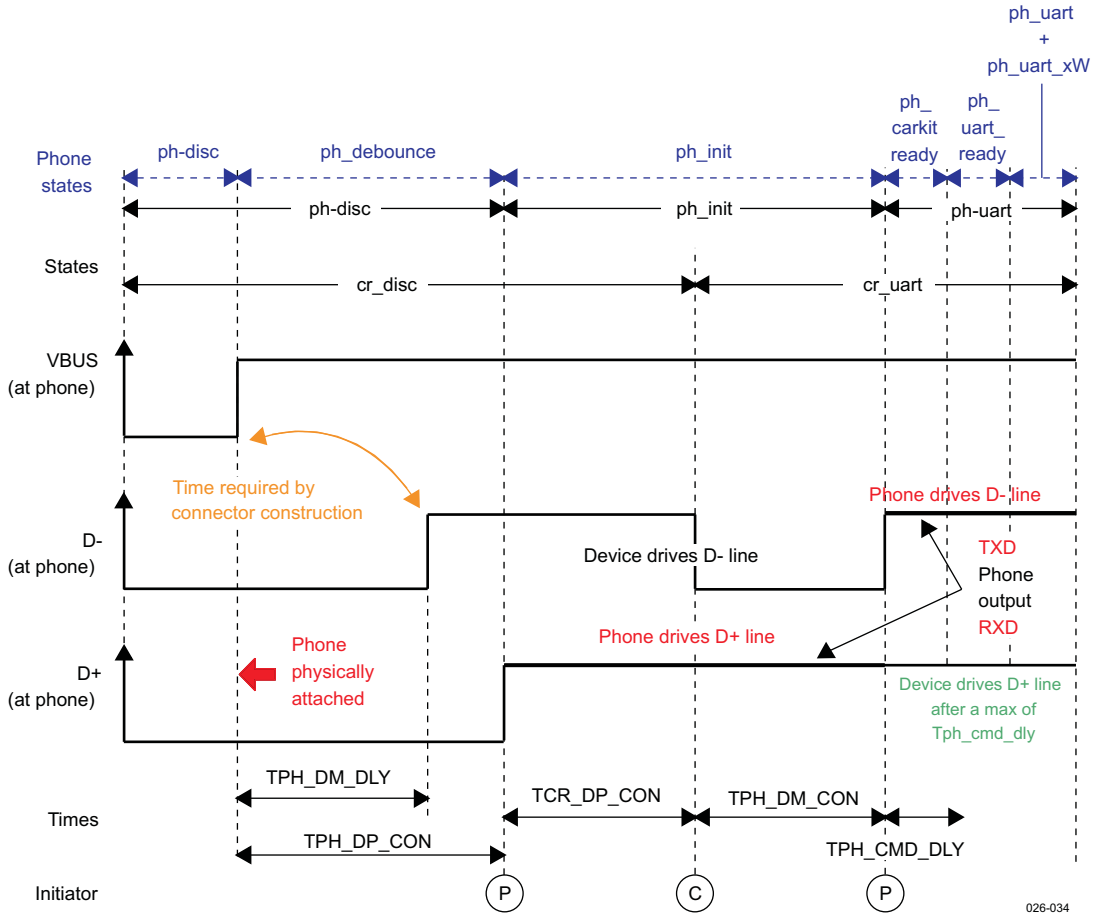
The connection sequence follows the steps described in the CEA-936-A specification.

Some interrupts are generated during this connection sequence to give a status to the application layer (or software) that uses the carkit functions. To use the PSM correctly, enable the following interrupt registers: CARKIT_SM_1_INT_EN, CARKIT_SM_2_INT_EN, and bits 2 and 3 in CARKIT_INT_EN.

14.4.9.2.1 Connection Sequence Description

Figure 14-27 is the CEA timing diagram of a carkit connection sequence. It shows the corresponding states of the hardware PSM that support the CEA carkit.

Figure 14-27. CEA Timing Diagram and PSM States Carkit Connection Sequence



NOTE: Courtesy CEA

To activate the state-machine, set the CARKIT_SM_CTRL_SET[0] CARKIT_PSM_EN bit to 1 and the CARKIT_SM_CTRL_SET[1] CARKIT_ PSM_RESET bit to 0. At this point, the application layer receives the DISCONNECTED interrupt because the default state is ph_disc. This is also the case for any reset of the PSM or a disconnection request. This interrupt is cleared to continue using the state-machine.

When a phone is connected to a carkit, the phone detects the voltage on the VBUS line (because a carkit always provides voltage on VBUS, and this corresponds to the ph_debounce state) and responds by pulling the D+ line high (ph_init state). The carkit detects that a phone is connected when the D+ line goes high.

As described in the CEA specification, because the USB supports USB and UART signaling protocols, by default the phone typically enters UART 4-wire mode after being attached to a carkit. The phone can query the carkit using the GET_FEATURES command to determine whether the carkit can act as a USB host. If the carkit supports USB signaling, the phone can reenter USB mode by setting the USB_CARKIT_MODE bit to 1 and sending a DISC_REQ command to exit UART mode.

If the USB_CARKIT_MODE bit is not set, the carkit drives D− low for a period of time, and then the phone recognizes that the carkit is in UART mode.

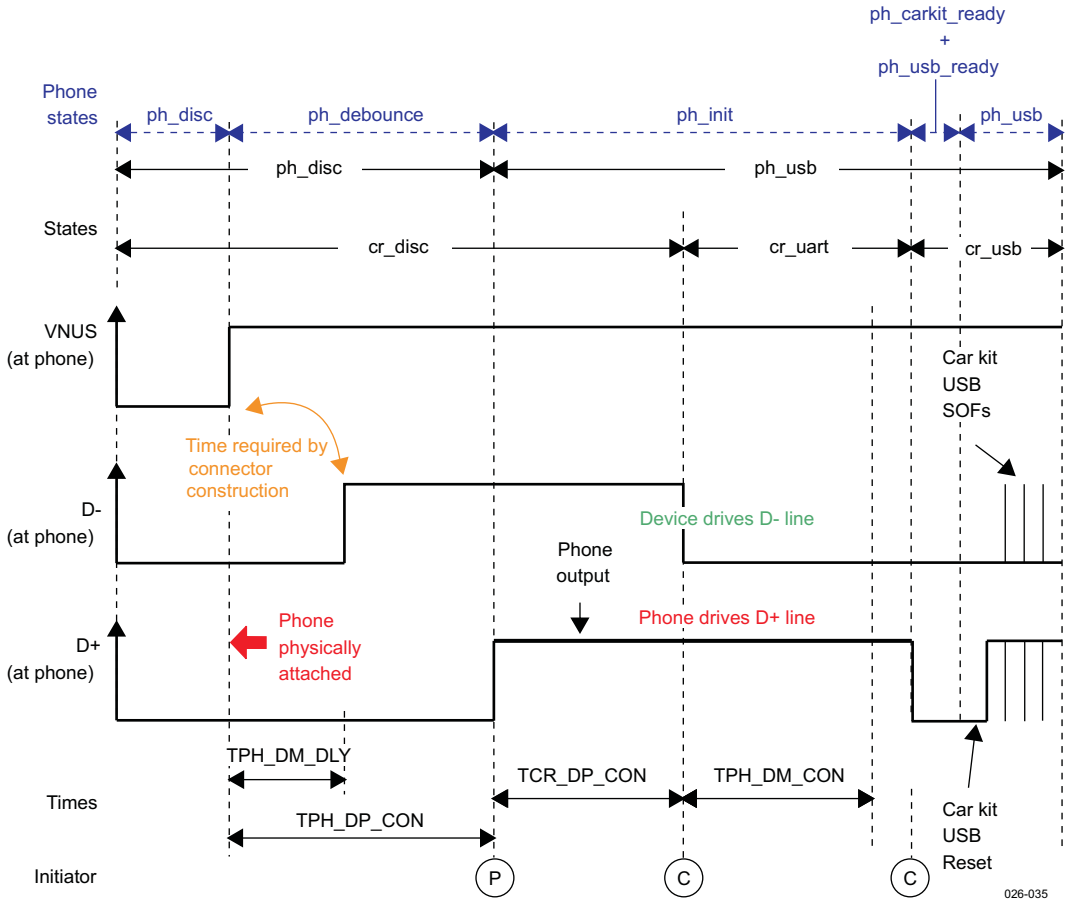
After detecting D− low, the phone asserts D+ high. To inform the software that it is now in UART mode, a CARKIT interrupt is generated. For the software to start using the D+/D− lines as UART lines, it must send a SW_UART_READY command before sending any UART commands to the carkit. If the carkit supports UART signaling, the phone can use these commands to configure the carkit or send information to it.

The phone can support 4-wire and 5-wire protocols. The customer decides which type of carkit software is to be supported.

The phone can use the OTHER_FUNCT_CTRL[2] FIVEWIRE_MODE bit to select 5-wire mode.

If the phone is in USB signaling mode, the application layer can quit USB mode for UART mode by setting the DISC_REQ bit to 1 and the USB_CARKIT_MODE bit to 0. Figure 14-28 shows CEA timing and the PSM states USB connection sequence.

Figure 14-28. CEA Timing Diagram and PSM States USB Connection Sequence



NOTE: Courtesy CEA

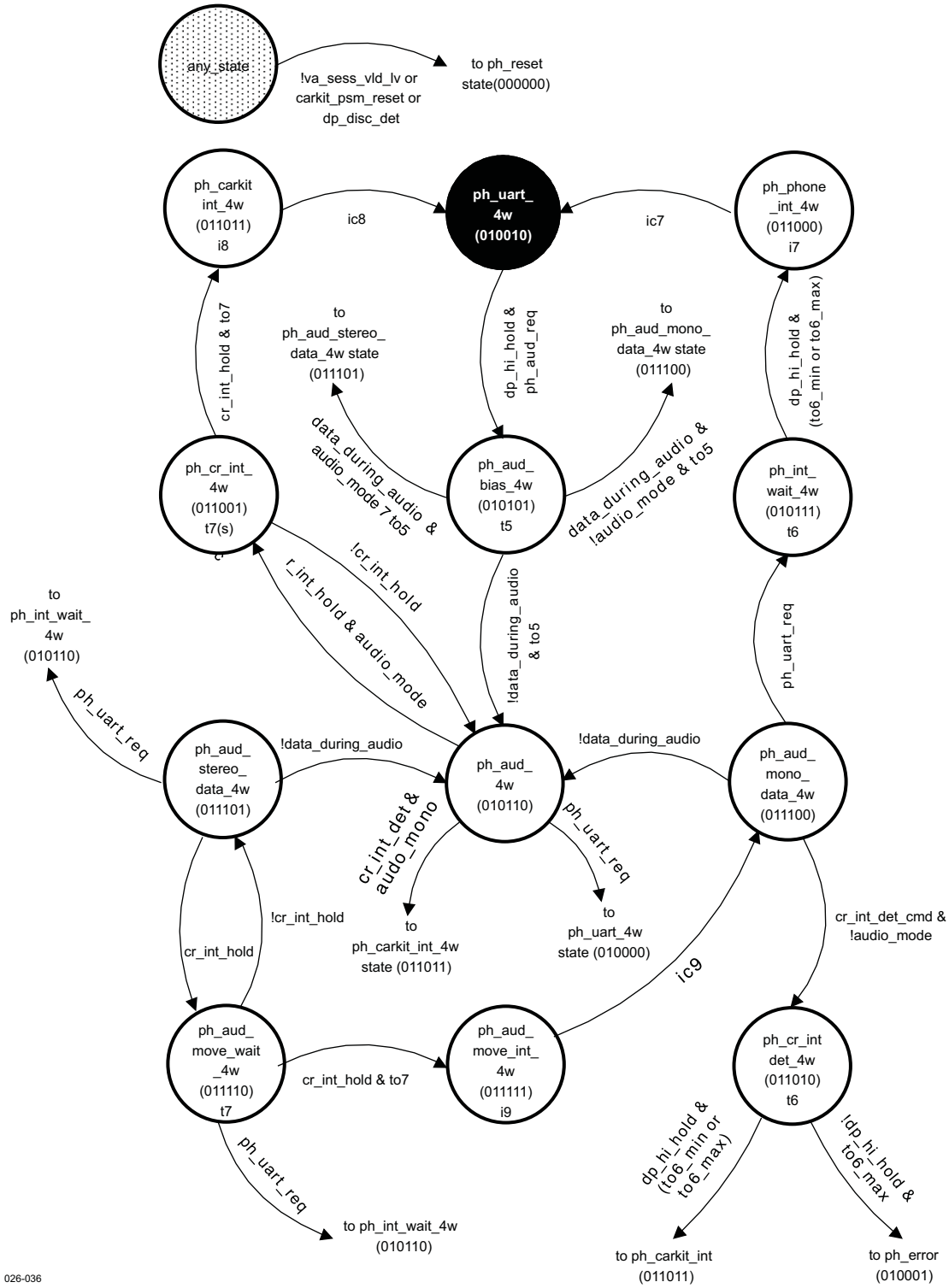
During the connection sequence, if the carkit does not act correctly, the state-machine goes to an error state and a PSM_ERROR interrupt is generated. A status is then available in the CARKIT_SM_ERR_STATUS register.

NOTE: To exit a state where an interrupt has been generated, the application layer must clear the interrupt. The phone can abort the system at any time by setting the CARKIT_PSM_RESET bit to 0. This is available for the entire state-machine. Also, a dp_disc_det event can abort the carkit function; this event indicates that the phone has detected that D+ is below its VPH_DP_LO threshold for a time of TPH_DISC_DET.

14.4.9.3 PSM: 4-Wire State Diagram

Figure 14-29 is the 4-wire state diagram.

Figure 14-29. 4-Wire State Diagram



14.4.9.3.1 4-Wire Description

After the phone clears the CARKIT interrupt, depending on the value of the OTHER_FUNCT_CTRL[2] FIVE_WIREMODE bit, the phone enters UART 4-wire or 5-wire state.

To exit UART 4-wire state, the application layer must set the PH_AUD_REQ command.

The phone is now in mono or stereo mode.

To enter stereo mode, the phone configures the carkit using the SET_CONFIG0 command (UART command), and then sets the CARKIT_SM_CTRL_SET[3] AUDIO_MODE bit to 1.

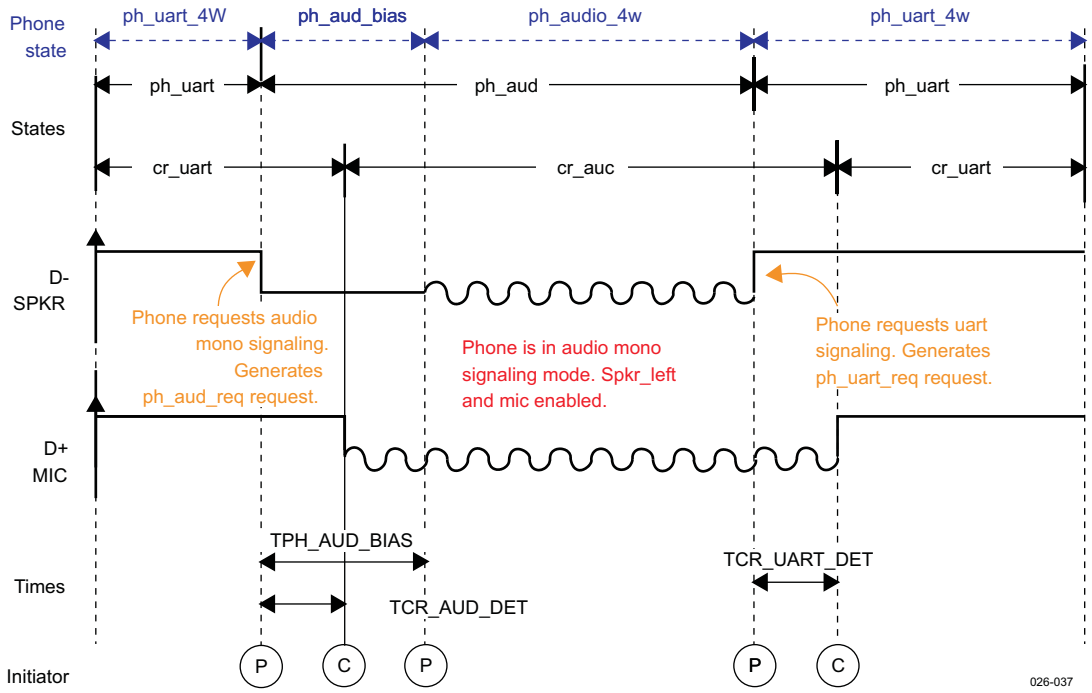
14.4.9.3.1.1 DATA_DURING_AUDIO Disable

In audio mode, the phone can interrupt audio signaling at any time. The application layer sets the CARKIT_SM_CMD[0] PH_UART_REQ bit to 1.

The phone then switches to UART state and drives the D– line high, as shown in Figure 14-30 (UART idle state in UART protocol).

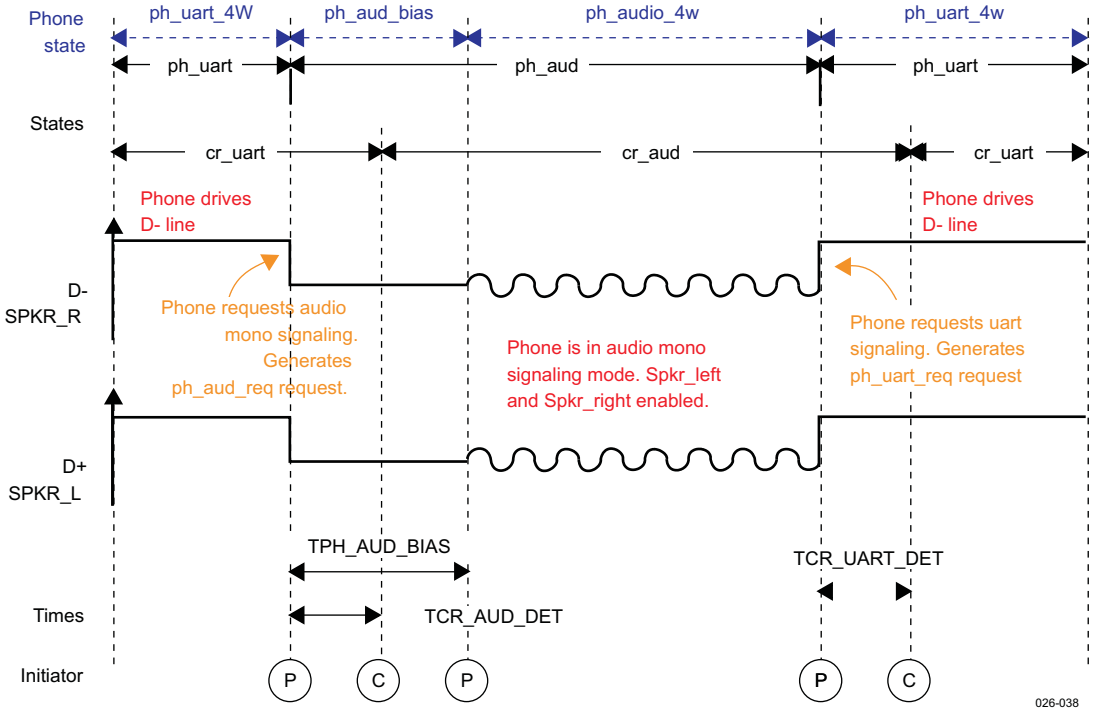
Figure 14-30 is the CEA timing diagram with PSM states for phone mono mode to UART. Figure 14-31 is the timing diagram with PSM states for phone stereo mode to UART.

Figure 14-30. CEA Timing Diagram and PSM States – Phone Mono to UART



NOTE: Courtesy CEA

Figure 14-31. CEA Timing Diagram and PSM States – Phone Stereo to UART



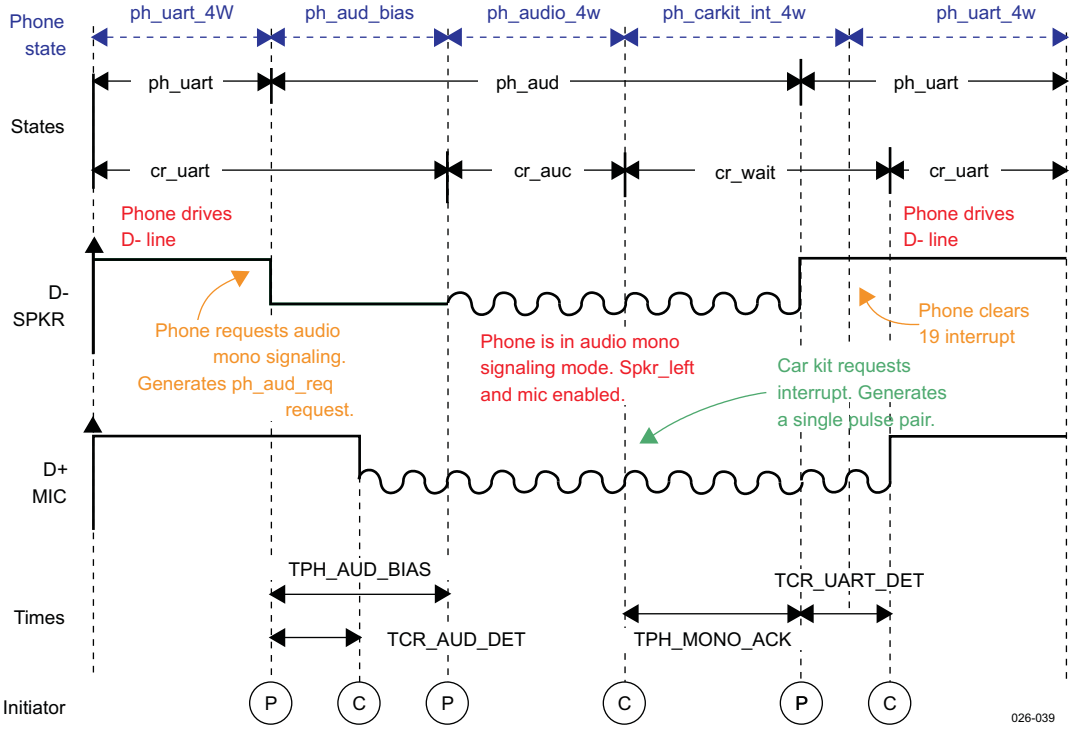
NOTE: Courtesy CEA

The phone can also be interrupted by the carkit during audio signaling. In this case, the application layer receives a CARINTDET(I8) interrupt for mono and stereo modes.

When this interrupt is cleared, the software is set in UART mode and drives the D− line (UART IDLE state) high.

Figure 14-32 is the CEA timing diagram with PSM states for carkit mono to UART.

Figure 14-32. CEA Timing Diagram and PSM States – Carkit Mono to UART

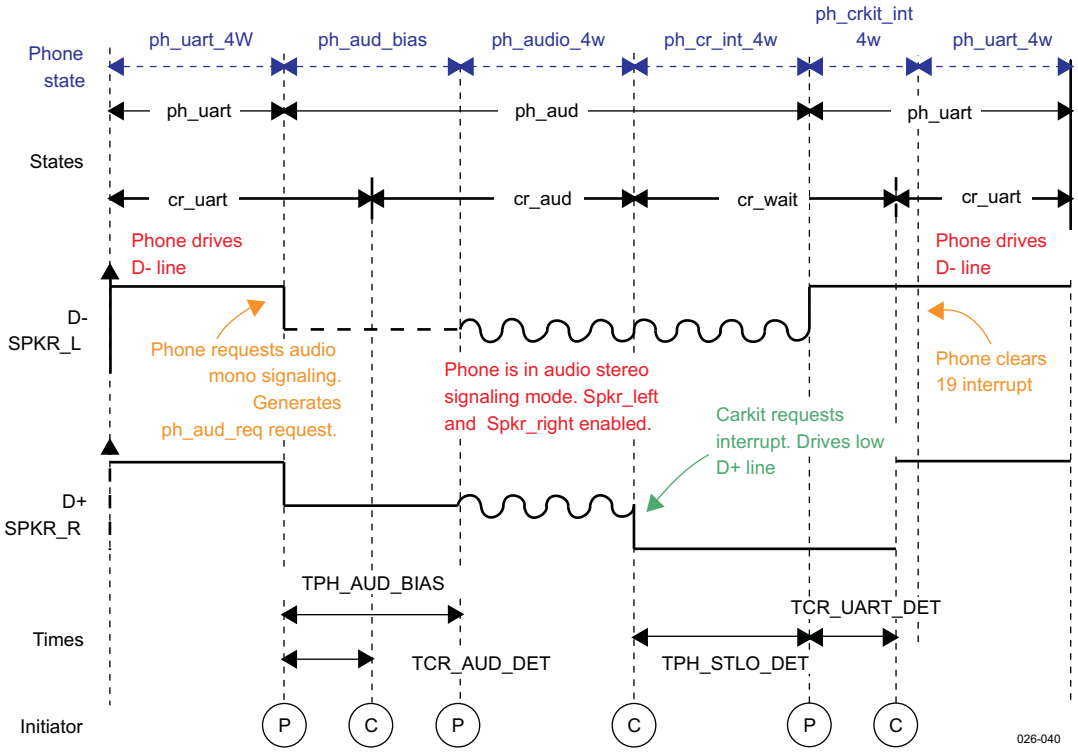


NOTE: Courtesy CEA

If DDA mode is enabled, the single pulse used by the carkit is replaced by a CR_INT_REQ byte (see Figure 14-33).

Depending on the status of UART traffic, the software interprets this interrupt differently. If UART traffic is not enabled, this interrupt corresponds to a button press on the carkit. If UART traffic is enabled, the phone must respond by issuing a GET_STATUS command to the carkit. Figure 14-33 is the CEA timing diagram with PSM states for carkit stereo to UART.

Figure 14-33. CEA Timing Diagram and PSM States Carkit Stereo to UART



NOTE: Courtesy CEA

14.4.9.3.1.2 DATA_DURING_AUDIO Enable

If the carkit supports the DDA mode setting, the CARKIT_SM_CTRL[5] DATA_DURING_AUDIO bit changes the interrupt method. The interrupt method is also affected by whether the phone is in mono or stereo mode.

During audio mono signaling, the phone can be interrupted by the carkit. The phone detects a CR_INT_REQ command sent by the carkit, and responds by sending a CR_INT_DET command.

When the application layer receives the CARINTDET (I8) interrupt, the phone sends a GET_STATUS command to the carkit, clears this interrupt, and then starts the UART protocol transmission.

When the phone is in audio stereo signaling and it detects a STEREO_TO_ MONO (I9) interrupt, the application layer sends a GET_STATUS command. This interrupt indicates that the carkit has interrupted the phone. The phone is now in mono signaling, not stereo signaling.

14.4.9.3.2 UART Details for Application Layer Programming

When a phone and a carkit are first connected, UART traffic is disabled (UART traffic is a software mode only). The carkit cannot send any UART traffic to the phone until the phone sends a UART command to the carkit.

While UART traffic is disabled, the carkit can signal an interrupt to the phone in UART mode by driving the D+ line low. This causes an interrupt if the CARKIT_INT_EN[3] CARDP_RISE_EN bit is set.

To enable UART traffic, the phone sends a UART command to the carkit. When the carkit receives a UART command with a valid cyclic redundancy check (CRC), UART traffic is enabled for the carkit.

When UART traffic is enabled and the carkit is in UART mode, the carkit cannot interrupt the phone with a single pulse on the D+ line; instead, it uses the CR_INT_REQ command to interrupt the phone.

If the phone receives a UART response from the carkit with a valid CRC, UART traffic is enabled for the phone. If the phone does not receive a valid response from the carkit during the time specified by TPH_UART_RPT (see *Phone Command Repeat Time* in the CEA-936-A specification), the phone can resend the UART command.

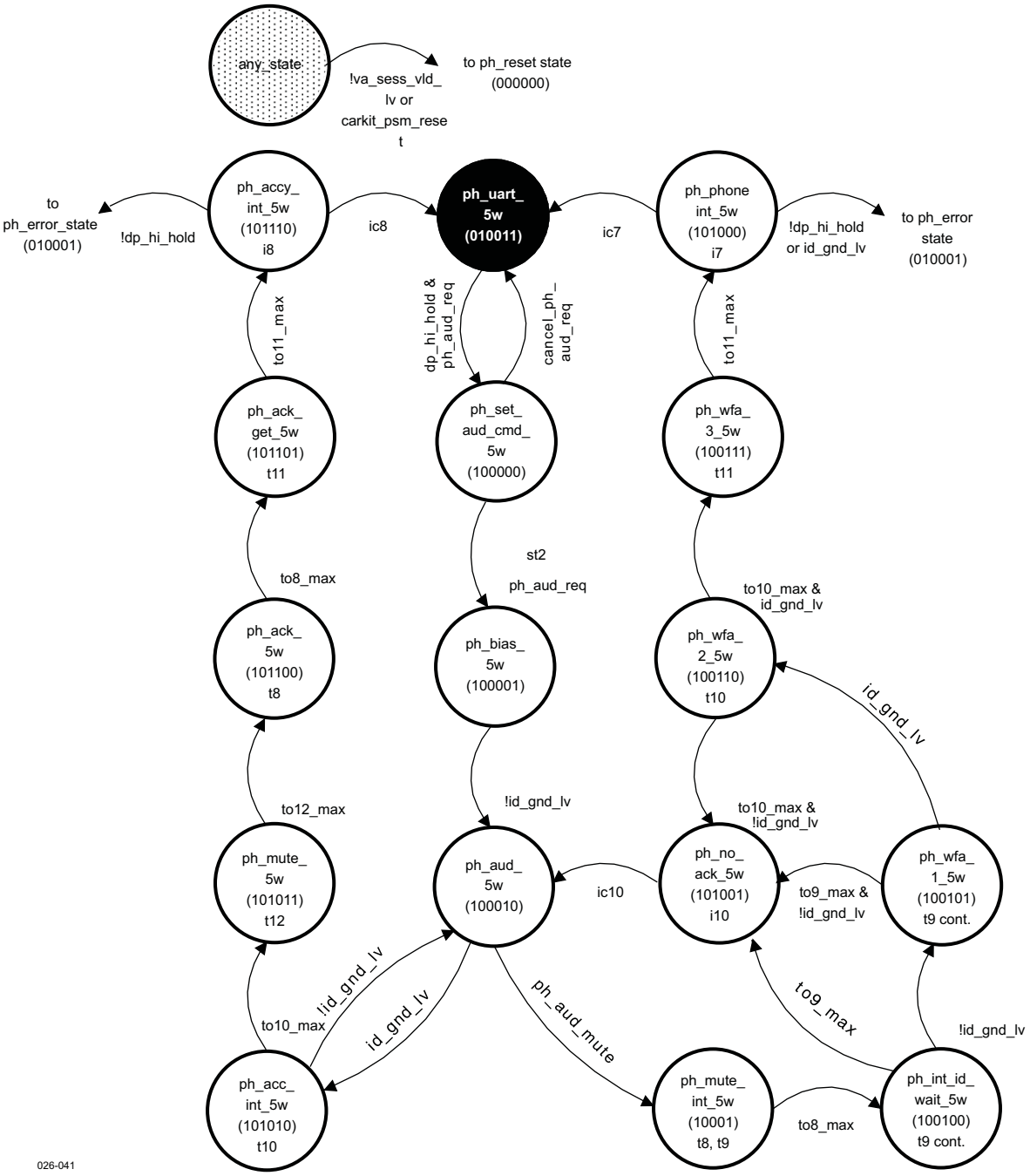
If the phone resends the command three times and receives no response, the assumption is that the carkit does not support UART traffic.

To determine whether the phone is connected to a basic carkit, the application layer sets the CARDP_RISE_EN bit to 1 to detect whether the carkit acknowledge is D− driven low. If the phone resends the command three times and detects the CARDP interrupt, the phone determines that it is connected to a basic carkit and sets the PH_AUD_REQ command to switch to audio signaling mode. If the phone resends the command three times and receives at least one corrupt response and no valid responses, the phone disconnects from the carkit with the DISC_REQ command.

14.4.9.4 PSM: 5-Wire State Diagram

Figure 14-34 is the 5-wire state diagram.

Figure 14-34. 5-Wire State Diagram

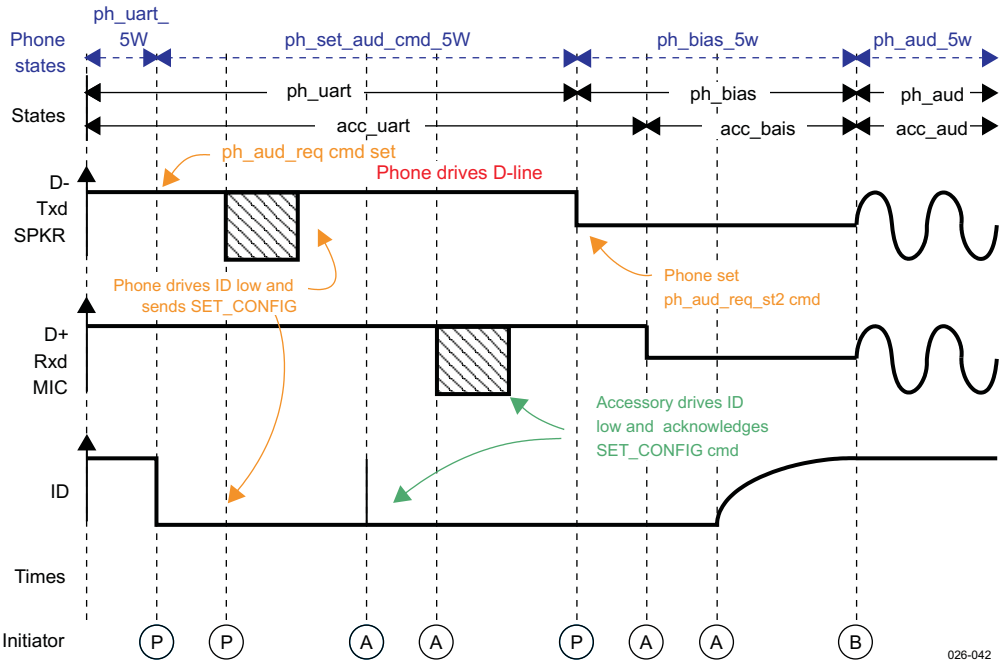


14.4.9.4.1 5-Wire Description

If the phone is in UART 5-wire state, it can use the PH_AUD_REQ command to initiate a transition to audio mode at any time. The phone then transmits the SET_CONFIG command to the accessory to change its state.

Figure 14-35 is the CEA timing diagram with PSM states for entering audio mode.

Figure 14-35. CEA Timing Diagram and PSM States: Entering Audio Mode



NOTE: Courtesy CEA

There is only one difference between entering mono mode and entering stereo mode. In mono mode, when the accessory receives the UART command to transition to mono mode, the accessory drives the ID low, and then acknowledges the SET_CONFIG command by sending another UART command (see the CEA-936-A specification, Section 10). In stereo mode, the phone does not drive the ID low, but it acknowledges by sending the same UART command.

When the phone receives the SET_CONFIG command acknowledgement from the accessory, the phone sets the PH_AUD_REQ_ST2 command.

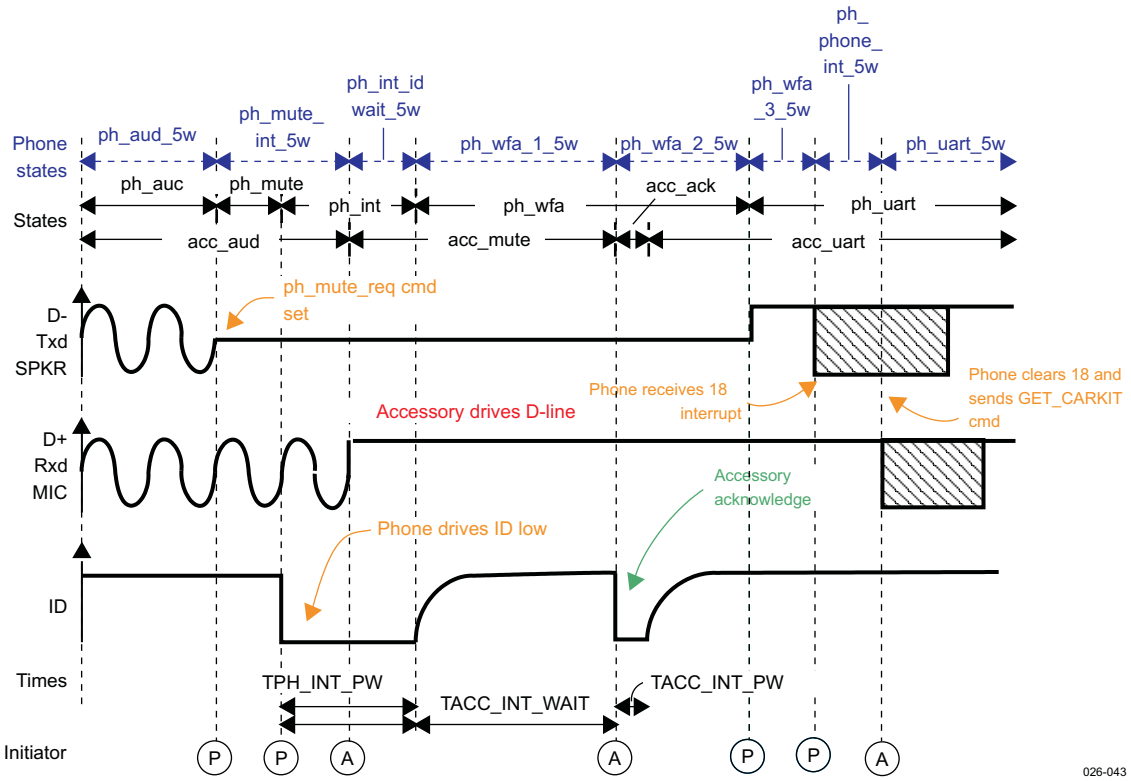
The phone is now in a biasing state and goes automatically to audio signaling mode when the ID line is released from the low level.

When the phone is in mono mode, the accessory releases the ID line when it starts to bias the microphone (MIC) line; in stereo mode, the phone releases the ID line when it goes to ph_bias_5w state, and the condition on the ID release to go to audio signaling mode is observed.

Mono and stereo modes are still chosen according to the setting of the AUDIO_MODE register bit.

Figure 14-36 is the CEA timing diagram with PSM states for phone to UART.

Figure 14-36. CEA Timing Diagram and PSM States: Phone to UART



A NOTE: Courtesy CEA

As with the 4-wire configuration, during audio signaling, the phone can interrupt the accessory at any time by setting the PH_MUTE_REQ command.

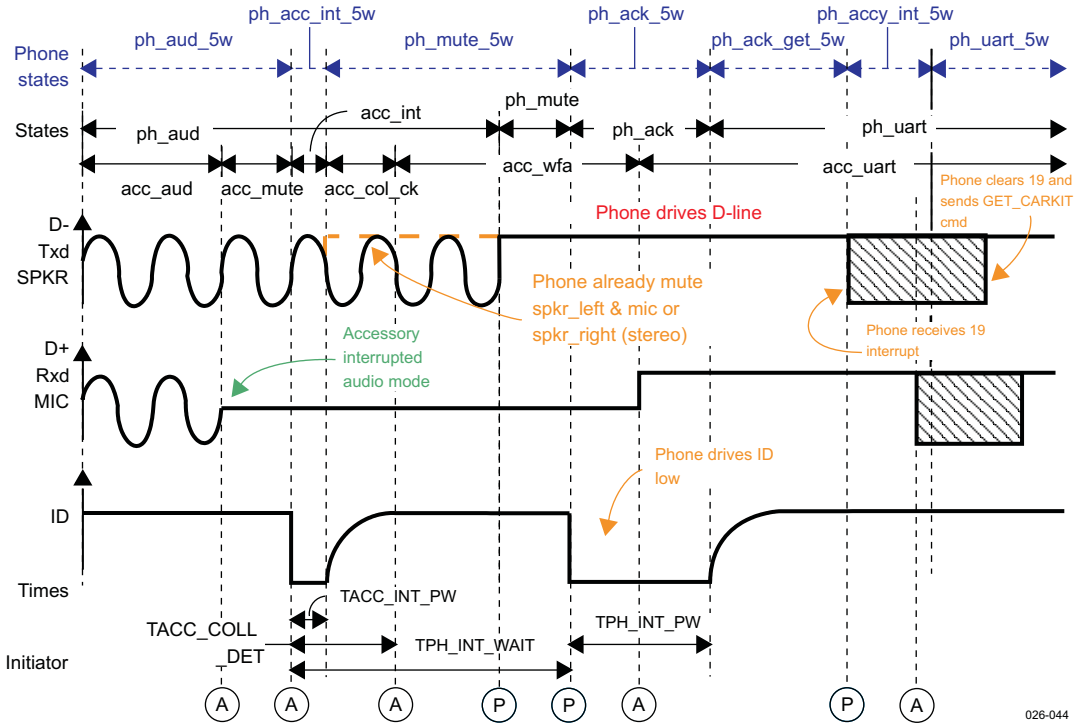
Figure 14-36 represents mono and stereo modes, because for the phone nothing changes in the interrupt mechanism. However, to be SPKR_R in stereo mode, the MIC line must be understood.

If the accessory does not correctly acknowledge the phone, the application layer detects a PH_NO_ACK (I10) interrupt. When the phone clears this interrupt, it can generate a new phone interrupt request.

If the accessory correctly acknowledges driving the ID low, the phone detects a PHONE_UART (I7) interrupt, sends a GET_CARKIT command, and clears the PHONE_UART interrupt to start any other UART exchanges.

Figure 14-37 is the CEA timing diagram with PSM states for accessory to UART.

Figure 14-37. CEA Timing Diagram and PSM States: Accessory to UART



NOTE: Courtesy CEA

When the accessory interrupts the phone, it asserts the ID low. The PSM then detects this event and stops audio signaling mode by muting SPKR (left in mono, and both in stereo).

14.4.9.5 DDA

The DDA feature lets the phone and the carkit send pulses to each other in audio mode without generating noticeable audio artifacts. These pulses can transfer digital data between the phone and the carkit.

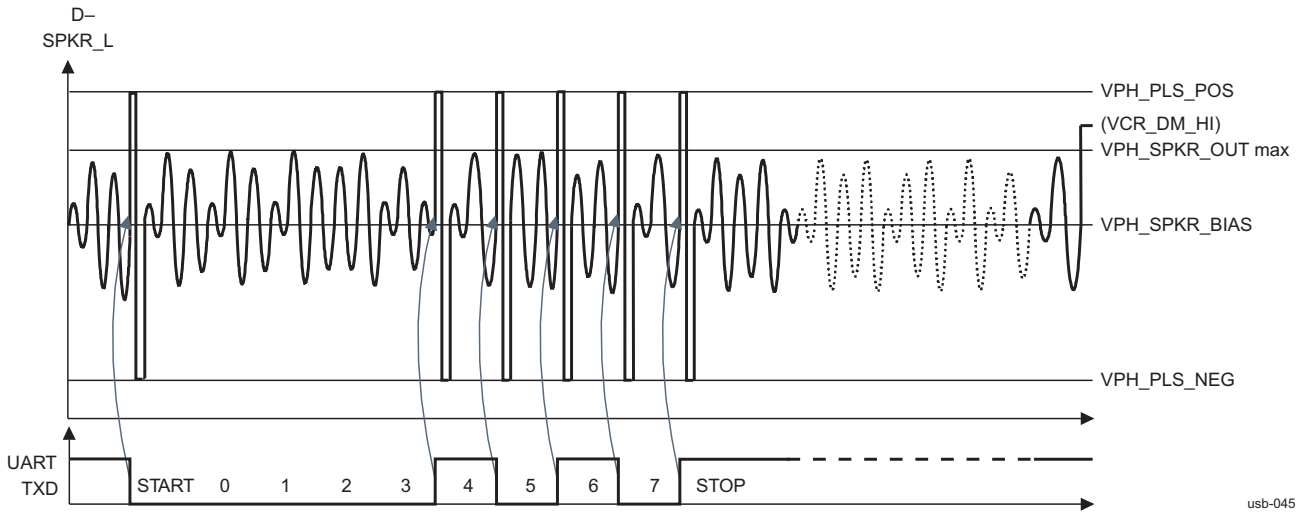
When the DDA feature is enabled in the CARKIT_SM_CTRL register, the carkit sends UART data to the phone by converting the nonreturn-to-zero (NRZ) UART signal to a series of pulses and transmitting them to the phone on the D+ line. The PHY in the phone then converts these pulses back to an NRZ UART signal by toggling the data line when a pulse is received.

14.4.9.5.1 DDA UART TX

When transmitting a UART byte, the phone outputs a pulse pair on the D− pin when its TXD signal changes state.

Figure 14-38 shows UART transmission during audio signaling.

Figure 14-38. UART TX During Audio Signaling



When outputting a pulse pair, the phone first outputs a positive pulse of amplitude VPH_PLS_POS and width TPH_PLS_POS. The phone then outputs a negative pulse of amplitude VPH_PLS_NEG and width TPH_PLS_NEG.

The width of the positive and negative pulses can be set through the TRANS_POS_WIDTH and the TRANS_NEG_WIDTH registers, respectively.

NOTE: To minimize distortion, the TRANS_POS_WIDTH register must be set to 0x0D and the TRANS_NEG_WIDTH register must be set to 0x09.

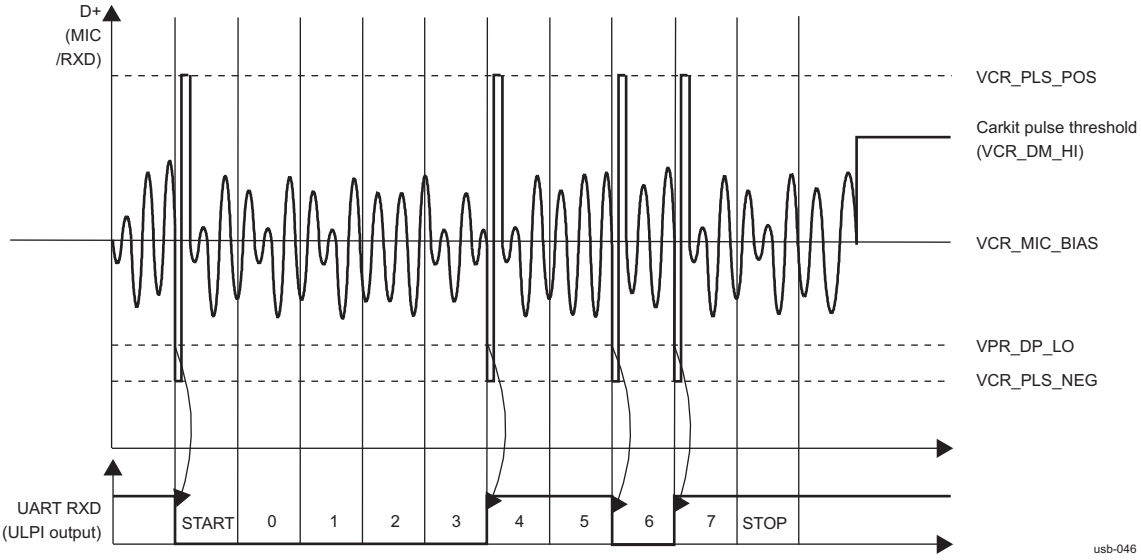
The application layer of the phone uses values so that the area of the positive pulse above the speaker bias voltage (VPH_SPKR_BIAS) is as close as possible to the area of the negative pulse below the speaker bias voltage. If the areas are equal, the pulse pair does not inject a dc bias onto the D− line, and the pulse pair does not create an audible artifact at the carkit speaker.

14.4.9.5.2 UART RX

When transmitting a UART byte, the carkit outputs a pulse pair when its TXD signal changes state.

When the phone receives a negative pulse on D+ below VPH_DP_LO, the phone toggles the state of an internal flip-flop to recover the RXD signal sent by the carkit (see Figure 14-39).

Figure 14-39. UART RX During Audio Signaling



If the PHY misses a pulse or detects an extra pulse, the polarity on the output line is incorrect. To recover from this condition, the PHY automatically resets the polarity of the output line to logic high when the polarity of the output line has been logic low for the time specified in the receive polarity recovery register.

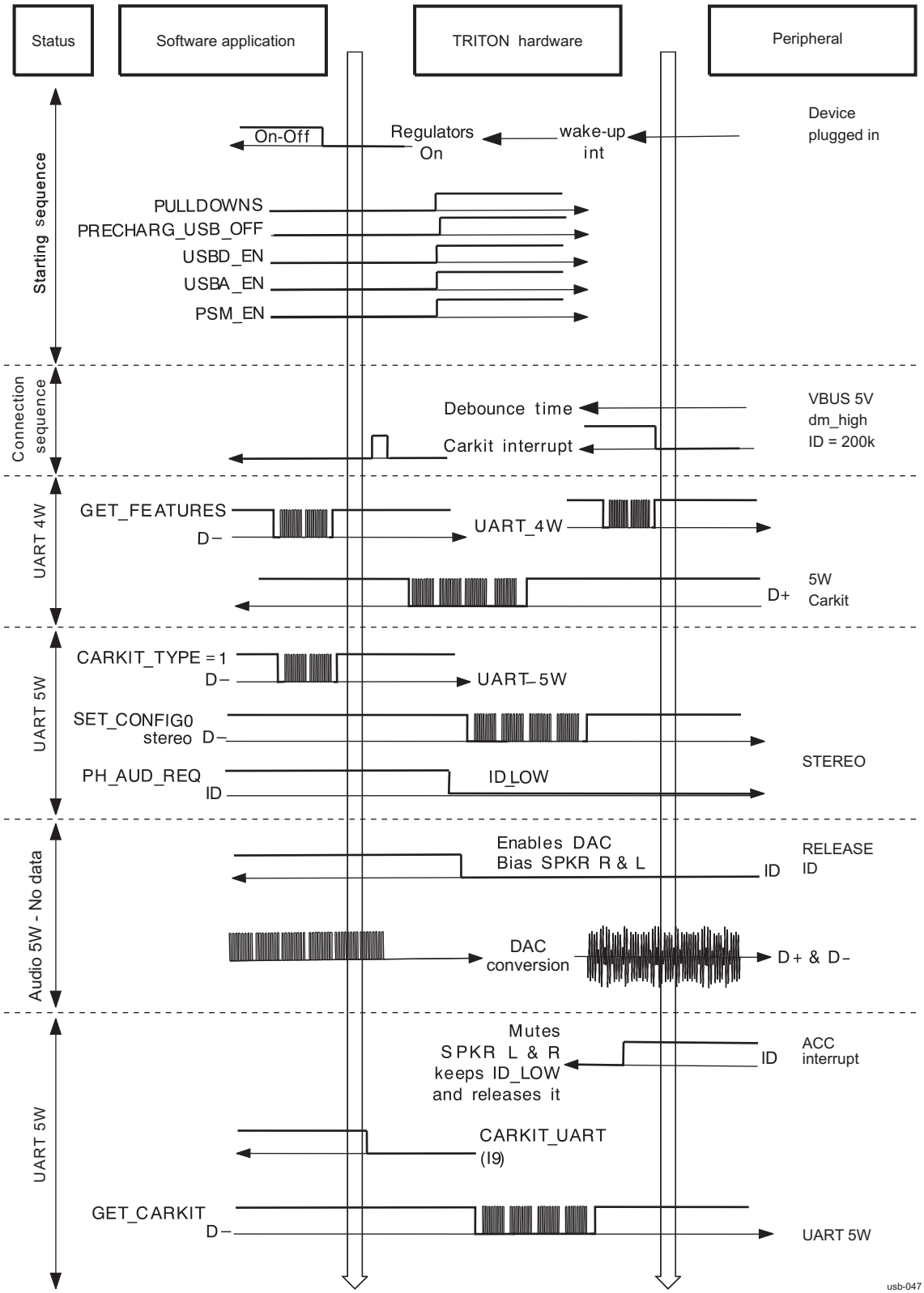
The receive polarity recovery is active only if the CARKIT_ PLS_CTRL[1] RXPLSEN bit = 1.

14.4.9.6 PSM Software Aspect

14.4.9.6.1 CEA Programming Model Sequence Overview

Figure 14-40 shows the CEA programming model sequence.

Figure 14-40. Programming Model



14.4.9.6.2 Hardware PSM Controlled by Application Layer

To minimize software control of the carkit, a hardware solution supports the CEA-936-A specification. Therefore, with a minimum of I^2C access, the phone can negotiate with a carkit device.

Although there is a hardware implementation, the software can force any state directly into the PSM by setting the CARKIT_SM_CTRL_STATE[1] CTRL_STATE_EN bit to 1, and can force the PSM state number using the CARKIT_SM_CTRL_STATE[5:0] CARKIT_SM_CTRL_STATE bit field.

The state-machine resumes from the state to which it was forced by clearing the CTRL_STATE_EN bit to 0.

Programmable timing values offer additional PSM flexibility.

NOTE: The PSM defined by the CEA is a basic behavior. For each state, many parameters are missing; for example, no difference is given between 4-wire and 5-wire protocols.

Here, the basic interrupt registers and command registers that must be set by the application layer to detect events from the analog side are defined. For each use (UART or USB signaling, etc.), however, interrupts and the commands to set differ and depend on the protocol.

14.4.9.6.3 PSM Timers and Time-Out Operations

Most CEA-936-A timings are controlled using a single 14-bit timer with two programmable comparator thresholds. This counter is usually cleared when a new state is entered, except for the TACC_ID_INT_WAIT timing control, which keeps incrementing its previous value over two states. Depending on which PSM states are entered, the thresholds are initialized with values corresponding to the encoded register settings as defined in the timing values in the CEA-936-A specification (see Table 14-20), and the timer starts counting in 32-kHz increments. The timer keeps counting while staying in the same state; if the programmed threshold is reached, a time-out event is generated to determine the next state. This counter is not used for states without timing indications.

These registers must be programmed to nominal timing requirements or minimum or maximum values.

Timing registers without the _MIN or _MAX suffix are set for nominal timings.

NOTE: Default timings are consistent with the requirements of the CEA-936-A specification.

Figure 14-41 shows the CEA timers in the PSM. Table 14-20 shows the CEA timings. Table 14-21 shows 7-bit register/14-bit counter encoding.

Figure 14-41. CEA Timers in the PSM

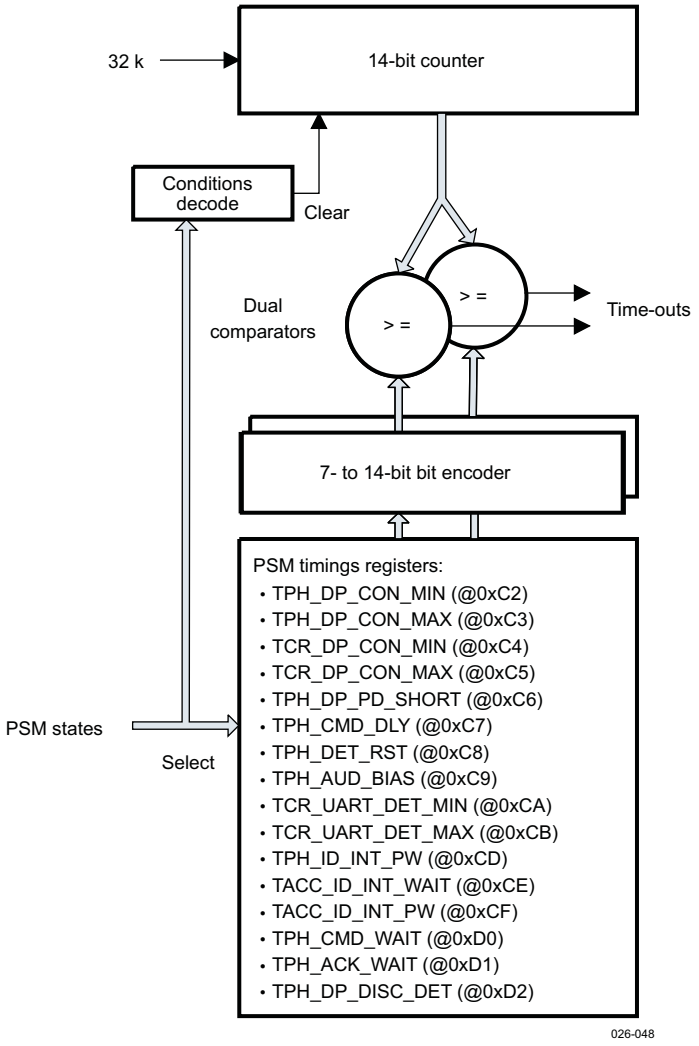


Table 14-20. CEA Timings

Timer	Register	Default Value	Description	Min	Typ	Max	Unit
t0 (minimum/ maximum)	TPH_DP_CON_MIN (0xC2) TPH_DP_CON_MAX (0xC3)	0x64 (100.5 ms) 0x7F (512 ms)	Phone D+ connect time	100		500	ms
t1 (minimum/ maximum)	TCR_DP_CON_MIN (0xC4) TCR_DP_CON_MAX (0xC5)	0x6C (171 ms) 0x75 (293 ms)	Carkit D+ connect time	150		300	ms
t2 (nominal)	TPH_DP_PD_SHORT (0xC6)	0x64 (100 ms)	D+ / D− short time		100		ms
t3 (nominal)	TPH_CMD_DLY (0xC7)	0x20 (2.25 ms)	Phone command delay	150			ms
t4 (nominal)	TPH_DET_RST (0xC8)	0x01 (60 ms)	Time to detect a reset from upstream	2.5		10,000	ms
t5 (nominal)	TPH_AUD_BIAS (0xC9)	0x17 (1.03 ms)	Phone AUDIO bias	1		10	ms
t6 (minimum/ maximum)	TCR_UART_DET_MIN (0xCA) TCR_UART_DET_MAX (0xCB)	0x01 (60 ms) 0x02 (60 ms)	Carkit UART detect	700		1200	ns
t7 (nominal)	CARKIT_INT_DELAY (0x1C)	0x52 (30.1 ms)	Phone STEREO D+ low detect	30	50	100	ms
t8 (nominal)	TPH_ID_INT_PW (0xCD)	0x36 (8.1 ms)	Phone ID interrupt pulse width	4		8	ms
t9 (nominal)	TACC_ID_INT_WAIT (0xCE)	0x44 (15.2 ms)	Accessory ID interrupt wait time	10		15	ms
t10 (nominal)	TACC_ID_INT_PW (0xCF)	0x07 (220 ms)	Accessory ID interrupt pulse width	200		400	ms
t11 (nominal)	TPH_CMD_WAIT (0xD0)	0x3B (10.22 ms)	Phone command wait time		10		ms
t12 (nominal)	TPH_ACK_WAIT (0xD1)	0x17 (1.03 ms)	Phone acknowledge wait time		1		ms
t13 (nominal)	TPH_DISC_DET (0xD2)	0x6B (160 ms)	Phone D+ disconnect time	150			ms

Table 14-21. 7-Bit Register/14-Bit Counter Encoding

Timer Value	Clock Cycles	Time (ms)	Timer Value	Clock Cycles	Time (ms)	Timer Value	Clock Cycles	Time (ms)	Timer Value	Clock Cycles	Time (ms)
0x00	2	0.06	0x20	72	2.25	0x40	408	12.75	0x60	2434	76.06
0x01	2	0.06	0x21	78	2.44	0x41	426	13.31	0x61	2611	81.59
0x02	2	0.06	0x22	84	2.63	0x42	445	13.91	0x62	2800	87.50
0x03	3	0.09	0x23	90	2.81	0x43	465	14.53	0x63	3002	93.81
0x04	4	0.13	0x24	96	3.00	0x44	486	15.19	0x64	3217	100.53
0x05	5	0.16	0x25	103	3.22	0x45	508	15.88	0x65	3446	107.69
0x06	6	0.19	0x26	110	3.44	0x46	531	16.59	0x66	3689	115.28
0x07	7	0.22	0x27	117	3.66	0x47	555	17.34	0x67	3947	123.34
0x08	8	0.25	0x28	124	3.88	0x48	580	18.13	0x68	4220	131.88
0x09	9	0.28	0x29	132	4.13	0x49	607	18.97	0x69	4509	140.91
0x0A	10	0.31	0x2A	140	4.38	0x4A	636	19.88	0x6A	4814	150.44
0x0B	11	0.34	0x2B	148	4.63	0x4B	667	20.84	0x6B	5136	160.50
0x0C	12	0.38	0x2C	156	4.88	0x4C	700	21.88	0x6C	5475	171.09
0x0D	13	0.41	0x2D	165	5.16	0x4D	736	23.00	0x6D	5832	182.25

Table 14-21. 7-Bit Register/14-Bit Counter Encoding (continued)

Timer Value	Clock Cycles	Time (ms)	Timer Value	Clock Cycles	Time (ms)	Timer Value	Clock Cycles	Time (ms)	Timer Value	Clock Cycles	Time (ms)
0x0E	14	0.44	0x2E	174	5.44	0x4E	775	24.22	0x6E	6207	193.97
0x0F	15	0.47	0x2F	183	5.72	0x4F	817	25.53	0x6F	6601	206.28
0x10	16	0.50	0x30	192	6.00	0x50	862	26.94	0x70	7014	219.19
0x11	18	0.56	0x31	202	6.31	0x51	911	28.47	0x71	7447	232.72
0x12	20	0.63	0x32	212	6.63	0x52	964	30.13	0x72	7900	246.88
0x13	22	0.69	0x33	223	6.97	0x53	1022	31.94	0x73	8374	261.69
0x14	24	0.75	0x34	234	7.31	0x54	1085	33.91	0x74	8869	277.16
0x15	27	0.84	0x35	246	7.69	0x55	1154	36.06	0x75	9386	293.31
0x16	30	0.94	0x36	258	8.06	0x56	1229	38.41	0x76	9926	310.19
0x17	33	1.03	0x37	271	8.47	0x57	1311	40.97	0x77	10,491	327.84
0x18	36	1.13	0x38	284	8.88	0x58	1400	43.75	0x78	11,084	346.38
0x19	40	1.25	0x39	298	9.31	0x59	1497	46.78	0x79	11,709	365.91
0x1A	44	1.38	0x3A	312	9.75	0x5A	1602	50.06	0x7A	12,371	386.59
0x1B	48	1.50	0x3B	327	10.22	0x5B	1716	53.63	0x7B	13,076	408.63
0x1C	52	1.63	0x3C	342	10.69	0x5C	1839	57.47	0x7C	13,830	432.19
0x1D	57	1.78	0x3D	358	11.19	0x5D	1972	61.63	0x7D	14,640	457.50
0x1E	62	1.94	0x3E	374	11.69	0x5E	2115	66.09	0x7E	15,513	484.78
0x1F	67	2.09	0x3F	391	12.22	0x5F	2269	70.91	0x7F	16,383	511.97

14.4.9.6.4 PSM States, Interrupts, and Timers Summary

Table 14-22 lists the PSM states, interrupts, and timers.

Table 14-22. PSM States, Interrupts, and Timers Summary

PSM States		Interrupts		Timers		PSM Figure		
Number	Name	Number	Name	Number	Parameter	con	4w	5w
000000	ph_reset	–		–		x		
000001	ph_disc	i0	DISCONNECTED	–		x		
000010	ph_debounce	–		t0	TPH_DP_CON	x		
000011	ph_init	–		t1		x		
000100	ph_carkit	–		–	TCR_DP_CON	x		
000101	ph_usb_ready	i1	CARKIT	–		x		
000110	ph_usb	–		–		x		
000111	ph_uart_ready	–		t3	TPH_CMD_DLY	x		

Table 14-22. PSM States, Interrupts, and Timers Summary (continued)

PSM States		Interrupts		Timers		PSM Figure		
Number	Name	Number	Name	Number	Parameter	con	4w	5w
001000	ph_uart	i1	CARKIT	–		x		
001001	ph_check1	–		–		x		
001010	ph_usb_reset	–		t4	TPH_DET_RST	x		
001011	ph_usb_host	i3	USB_HOST	–		x		
001100	ph_check_short1	–		t1	TCR_DP_CON	x		
001101	ph_check_short2	–		t2	TPH_DP_PD_SHORT	x		
001110	ph_charger	i4	CHARGER	–		x		
001111	ph_pacc	i5	PH_ACC	–		x		
010000	ph_usb_otg_b	i2	USB_OTG_B	–		x		
010001	ph_error	i6	PSM_ERROR	–		x		
010010	ph_uart_4w	–		–		x	x	
010011	ph_uart_5w	–		–		x		x
010100	ph_switch_mode	–		–				
010101	ph_aud_bias_4w	–		t5	TPH_AUD_BIAS		x	
010110	ph_aud_4w	–		–			x	
010111	ph_int_wait_4w	–		t6	TCR_UART_DET		x	
011000	ph_phone_int_4w	i7	PHONE_UART	–			x	
011001	ph_cr_int_4w	–		t7	TPH_STLO_DET		x	
011010	ph_cr_int_det_4w	–		t6	TCR_UART_DET		x	
011011	ph_carkit_int_4w	i8	CARINTDET	–			x	
011100	ph_audio_mono_data_4w	–		–			x	
011101	ph_aud_stereo_data_4w	–		–				
011110	ph_aud_move_wait_4w	–		t7	TPH_STLO_DET		x	
011111	ph_aud_move_int_4w	i9	STEREO_TO_MONO	–			x	
100000	ph_set_aud_cmd_5w	–		–				x
100001	ph_bias_5w	–		–				x
100010	ph_aud_5w	–		–				x
100011	ph_mute_int_5w	–		t8, t9	TPH_ID_INT_PW TACC_ID_INT_WAIT			x
100100	ph_int_id_wait_5w	–		t9c	TACC_ID_INT_WAIT(cont)			x
100101	ph_wfa_1_5w	–		t9c	TACC_ID_INT_WAIT(cont)			x
100110	ph_wfa_2_5w	–		t10	TACC_ID_INT_PW			x
100111	ph_wfa_3_5w	–		t11	TPH_CMD_WAIT			x

Table 14-22. PSM States, Interrupts, and Timers Summary (continued)

PSM States		Interrupts		Timers		PSM Figure		
Number	Name	Number	Name	Number	Parameter	con	4w	5w
101000	ph_phone_int_5w	i7	PHONE_UART	–				x
101001	ph_no_ack_5w	i10	PH_NO_ACK	–				x
101010	ph_acc_int_5w	–		t10	TACC_ID_INT_PW			x
101011	ph_mute_5w	–		t12	TPH_ACK_WAIT			x
101100	ph_ack_5w	–		t8	TPH_ID_INT_PW			x
101101	ph_ack_get_5w	–		t11	TPH_CMD_WAIT			x
101110	ph_accy_int_5w	i8	CARINTDET	–				x
101111	Reserved							
11xxxx	Reserved							

14.4.10 Analog Audio Control

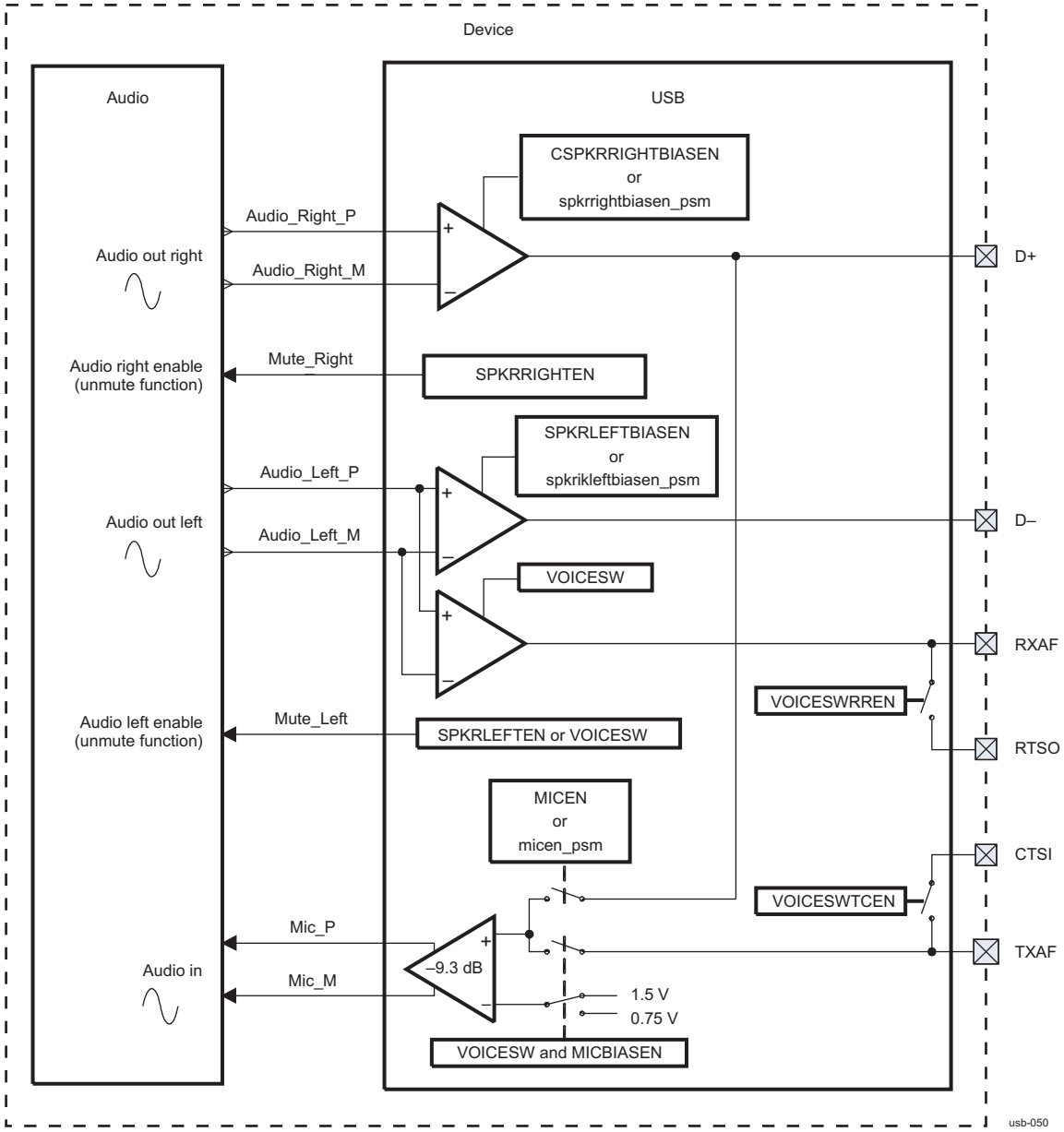
The USB architecture allows routing of the analog audio signals in and out by using the USB D+/D− device pins in a manner compliant with the CEA-936-A specification.

Besides analog audio signal routing control, the USB performs signal preamplification and dcline biasing.

To access this function, set the CARKIT_CTRL[0] CARKITPWR bit to 1.

Figure 14-42 shows the routing of the USB to audio.

Figure 14-42. USB-to-Audio Routing Overview



14.4.10.1 CEA-936-A Audio Mode

In this mode, the USB D− pin is the speaker analog audio output for the mono or stereo left channel in stereo modes; the USB D+ pin is the microphone analog audio input in audio mono mode or the speaker analog audio output right channel in stereo mode.

This mode is supported only with the PSM enabled (when the CARKIT_SM_CTRL[0] CARKIT_PSM_EN bit is set to 1). The correct setting of the audio controls is from PSM signals or register settings, depending on the current state of the PSM.

The SPKRRIGHTEN and SPKRLEFTEN bits in the CARKIT_CTRL register enable analog audio signals from the audio module (mute/unmute function). The SPKRRIGHTEN bit is set only for audio stereo operation. The phone speaker amplitude output is 0.5 V RMS maximum.

The SPKRRIGHTBIASEN and SPKRLEFTBIASEN bits in the CARKIT_PLS_CTRL register or the spkrrightbiasen_psm and spkrleftbiasen_psm signals from the PSM are used to bias the D+/D− lines to VPH_SPKR_BIAS voltage (0.7 V to 1.6 V).

The CARKIT_CTRL[6] MICEN bit or the micen_psm signal from the PSM enables the incoming audio signal to be sent to the audio module. The external microphone signal must not exceed 0.5 V RMS of amplitude and must be between 1.0 and 2.8 V.

The audio paths used for the MCPC mode are deactivated by setting the MCPC_CTRL[4] VOICESW bit to 0, and by setting the MCPC_IO_CTRL[5] MICBIASEN bit to 0.

The PSM versus register control implementation is as follows:

- MICEN = (micen_psm signal from PSM) or (MICEN register)
- SPKRRIGHTBIASEN = (spkrrightbiasen_psm signal from PSM) or (SPKRRIGHTBIASEN register)
- SPKRLEFTBIASEN = (spkrleftbiasen_psm signal from PSM) or (SPKRLEFTBIASEN register)

The PSM also supports DDA mode. When a digital pulse pair is transmitted on the left speaker output channel (the D− pin), the left speaker output analog amplifier is disabled for the time necessary to pass the digital signal.

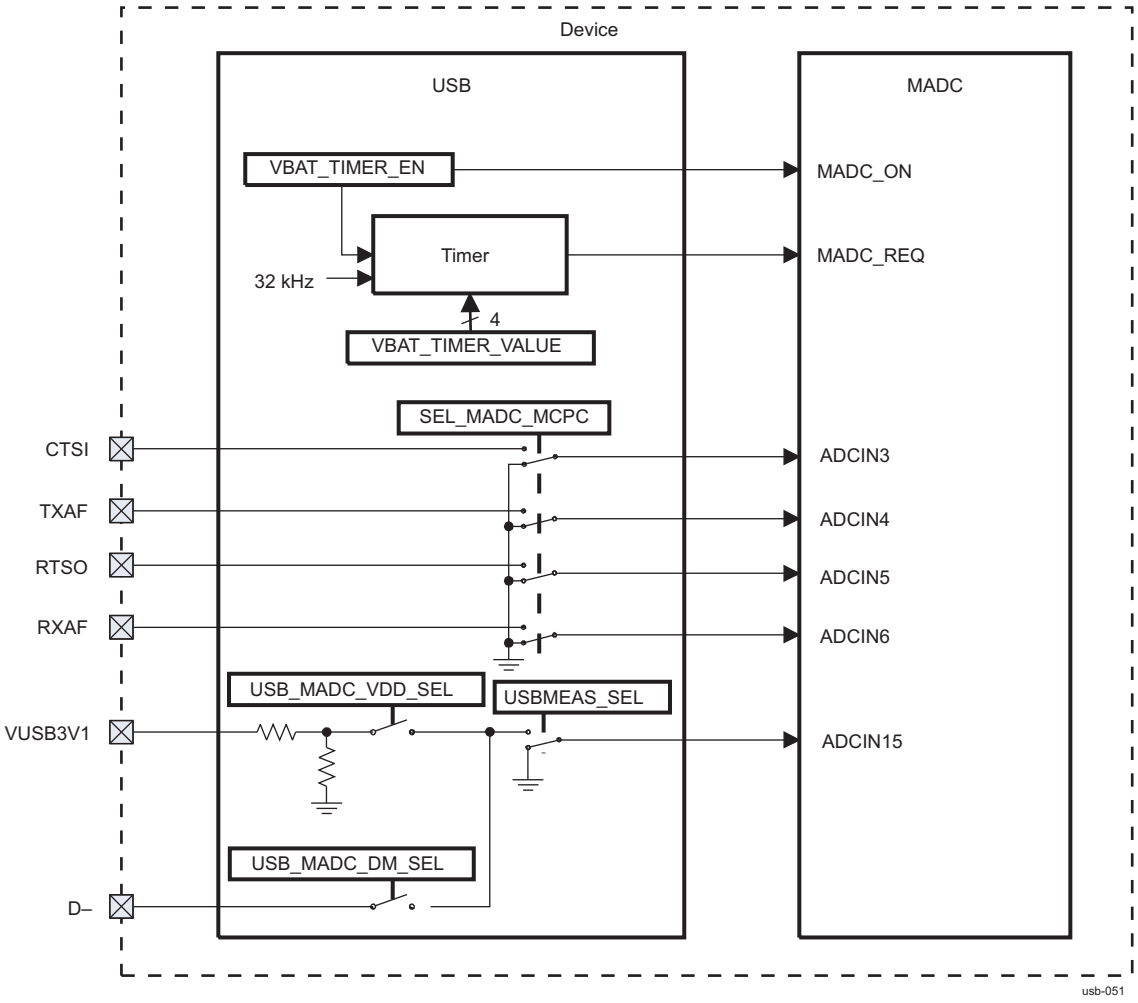
See Table 14-20 for the required register settings for CEA audio operations.

14.4.11 MADC Control

To access this function, set the CARKIT_CTRL[0] CARKITPWR bit to 1.

Figure 14-43 shows the routing of the USB to MADC.

Figure 14-43. USB to MADC Routing Overview



14.4.11.1 Using MADC for CEA-936-A DDA Pulse Area Calibration

The MADC can calibrate the DDA pulse area in CEA-636-A DDA mode by measuring the VUSB3V1 voltage and the common-mode voltage on DM.

To perform this measurement, configure the USB in mono audio mode. The left speaker signal on the DM should output common-mode voltage in mute mode during MADC (SPKR_LEFT_BIAS_EN = 1 and SPKR_LEFT_EN = 0).

Then the analog signal to be monitored must be routed to the USBMEAS input of the MADC by setting the USB_MADC_DM_SEL bit or the USB_MADC_VDD_ SEL bit in the CARKIT_ANA_CTRL register. This routes the DM (for the output common-mode measurement of SPKR_L) or the VUSB3V1 (after a divide-by-3 voltage divider) to USBMEAS.

Next, to select ADCIN15, set the CARKIT_ANA_CTRL[7] USBMEAS_SEL bit.

Finally, the MADC must be initiated. For information about how to initiate a MADC conversion, see Chapter 8, *Monitoring ADC*.

14.4.11.2 Use Case Restriction

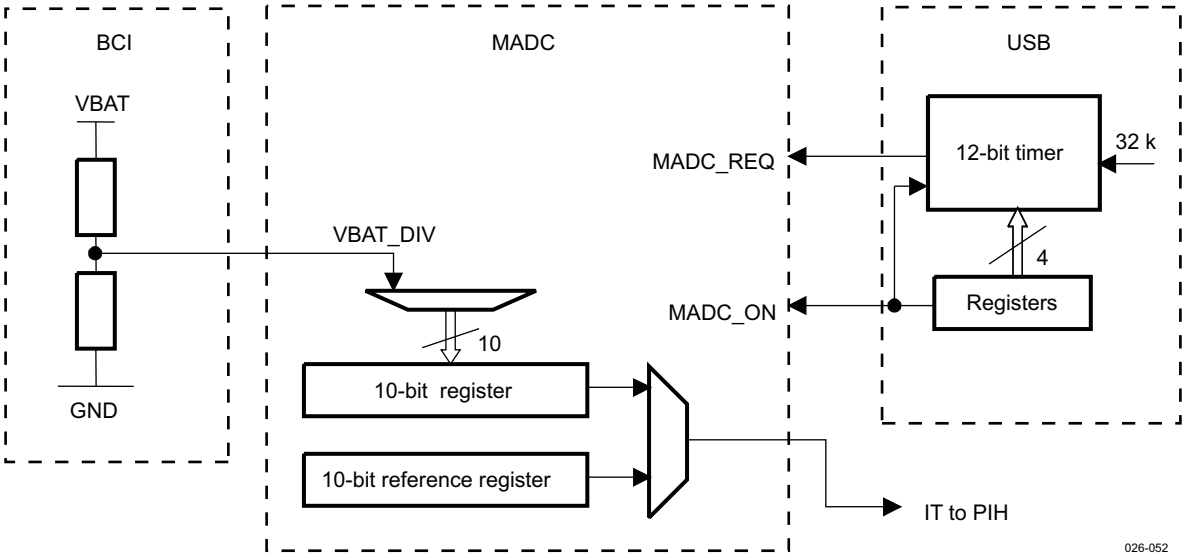
CAUTION

During the WAIT-ON power state (the VUSB3V1 regulator is off), nonzero dc voltage must not be applied on the CTSI/ADCIN3, TXAF/ADCIN4, RXAF/ADCIN6, RTSO/ADCIN5, DP/UART3.RXD, and DN/UART3.TXD pins. This is to avoid damage to the device caused by injection of large drain-bulk current on the speaker amp output stage (for the DP/UART3.RXD, DN/UART3.TXD, and RXAF pins) and on switches connected to the four MCPC pins (CTSI/ADCIN3, TXAF/ADCIN4, RXAF/ADCIN6, and RTSO/ADCIN5).

14.4.11.3 VBAT_CTRL Module

Figure 14-44 shows the VBAT monitoring function.

Figure 14-44. VBAT Monitoring Function



A VBAT monitoring function informs the host processor through an interrupt when the VBAT level crosses a programmable threshold voltage. The output of the VBUS/VBAT switch is connected to the input supply of the VRUSB3V1 regulator, which must always remain greater than the maximum regulator output voltage (3.2 V) plus the dropout voltage (100 mV); that is, the threshold must be set to 3.3 V. This interrupt can be used by the host processor to decide whether the VBUS/VBAT analog switch must be switched to VBUS or VBAT. This analog switch is controlled by the host processor. If switched to VBUS, the current drain exceeds the OTG specification, but it should function.

Sensitivity to a marginal VBAT level (near 3.3 V) is normally not a problem when the device functions as an A-device, because the USB charge pump is on (to supply VBUS) and this also provides input to VRUSB3V1. When the device is a B-device, the USB charge pump cannot be turned on (because its output is permanently connected to VBUS, and as a B-device the device cannot supply VBUS). When VBAT is marginal, the only option is to select VBUS as the input for VRUSB3V1.

VBAT is monitored by using an MADC channel. This channel is connected to a divide-by-4 resistive divider supplied by VBAT. The analog-to-digital conversion occurs in the MADC, and the result is compared with a reference value (the 3.3-V threshold described above).

If the VBAT level is lower than the reference, the MADC sends an interrupt to the PIH.

The default comparator reference level is equivalent to VBAT = 3.25 V, but this value is programmable.

The comparison can be performed with an average value of four VBAT conversions. This feature can be enabled and disabled by software (for more information, see Chapter 8, *Monitoring ADC*).

The USB system includes a timer and a control register for controlling the sampling rate for the MADC. MADC_ON is an enable signal for the MADC:

- The OTHER_FUNC_CTRL2[0] VBAT_TIMER_EN bit controls the MADC_ON enable signal and enables the 12-bit timer that generates the periodic conversion request.
- The VBAT_TIMER[3:0] VBAT_TIMER_VALUE bit field contains an encoded value that defines the periodicity of the sampling request (the MADC_REQ signal).

Table 14-23 lists the VBAT_TIMER_VALUE encoding.

Table 14-23. VBAT_TIMER_VALUE Encoding

VBAT_TIMER_VALUE	VBAT Conversion Request Rate (ms)
0	1.953
1	4.883
2	9.766
3	49.805
4	100.586
5	500
6	1000
7	2000
8	4000
9	8000
10	11,000
Others	15,000

14.5 Register Manual

For guidelines for accessing these registers, see Section 14.4.3, *Register Access and Arbitration Scheme*.

Table 14-24 lists the USB registers.

Table 14-25 through Table 14-148 describe the individual registers.

14.5.1 USB Register Mapping Summary

Table 14-24. USB Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	Reset Value
VENDOR_ID_LO	R	8	0x0000 0000	0x51
VENDOR_ID_HI	R	8	0x0000 0001	0x04
PRODUCT_ID_LO	R	8	0x0000 0002	0x02
PRODUCT_ID_HI	R	8	0x0000 0003	0xC0
FUNC_CTRL	RW	8	0x0000 0004	0x41
FUNC_CTRL_SET	RW	8	0x0000 0005	0x41
FUNC_CTRL_CLR	RW	8	0x0000 0006	0x41
IFC_CTRL	RW	8	0x0000 0007	0x10
IFC_CTRL_SET	RW	8	0x0000 0008	0x10
IFC_CTRL_CLR	RW	6	0x0000 0009	0x10
OTG_CTRL	RW	8	0x0000 000A	0x06
OTG_CTRL_SET	RW	8	0x0000 000B	0x06
OTG_CTRL_CLR	RW	8	0x0000 000C	0x06
USB_INT_EN_RISE	RW	8	0x0000 000D	0x1F
USB_INT_EN_RISE_SET	RW	8	0x0000 000E	0x1F
USB_INT_EN_RISE_CLR	RW	8	0x0000 000F	0x1F
USB_INT_EN_FALL	RW	8	0x0000 0010	0x1F
USB_INT_EN_FALL_SET	RW	8	0x0000 0011	0x1F
USB_INT_EN_FALL_CLR	RW	8	0x0000 0012	0x1F
USB_INT_STS	R	7	0x0000 0013	0x00
USB_INT_LATCH	R	8	0x0000 0014	0x00
DEBUG	R	8	0x0000 0015	0x00
SCRATCH_REG	RW	8	0x0000 0016	0x00
SCRATCH_REG_SET	RW	8	0x0000 0017	0x00
SCRATCH_REG_CLR	RW	8	0x0000 0018	0x00
CARKIT_CTRL	RW	8	0x0000 0019	0x00
CARKIT_CTRL_SET	RW	8	0x0000 001A	0x00
CARKIT_CTRL_CLR	RW	8	0x0000 001B	0x00
CARKIT_INT_DELAY	RW	8	0x0000 001C	0x52
CARKIT_INT_EN	RW	8	0x0000 001D	0x00
CARKIT_INT_EN_SET	RW	8	0x0000 001E	0x00
CARKIT_INT_EN_CLR	RW	8	0x0000 001F	0x00
CARKIT_INT_STS	R	8	0x0000 0020	0x00
CARKIT_INT_LATCH	R	8	0x0000 0021	0x00
CARKIT_PLS_CTRL	RW	8	0x0000 0022	0x00
CARKIT_PLS_CTRL_SET	RW	8	0x0000 0023	0x00
CARKIT_PLS_CTRL_CLR	RW	8	0x0000 0024	0x00
TRANS_POS_WIDTH	RW	8	0x0000 0025	0x05
TRANS_NEG_WIDTH	RW	8	0x0000 0026	0x0A
RCV_PLTY_RECOVERY	RW	8	0x0000 0027	0x03

Table 14-24. USB Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Reset Value
MCPC_CTRL	RW	8	0x0000 0030	0x00
MCPC_CTRL_SET	RW	8	0x0000 0031	0x00
MCPC_CTRL_CLR	RW	8	0x0000 0032	0x00
MCPC_IO_CTRL	RW	8	0x0000 0033	0x04
MCPC_IO_CTRL_SET	RW	8	0x0000 0034	0x04
MCPC_IO_CTRL_CLR	RW	8	0x0000 0035	0x04
MCPC_CTRL2	RW	8	0x0000 0036	0x00
MCPC_CTRL2_SET	RW	8	0x0000 0037	0x00
MCPC_CTRL2_CLR	RW	8	0x0000 0038	0x00
OTHER_FUNC_CTRL	RW	8	0x0000 0080	0x00
OTHER_FUNC_CTRL_SET	RW	8	0x0000 0081	0x00
OTHER_FUNC_CTRL_CLR	RW	8	0x0000 0082	0x00
OTHER_IFC_CTRL	RW	8	0x0000 0083	0x80
OTHER_IFC_CTRL_SET	RW	8	0x0000 0084	0x80
OTHER_IFC_CTRL_CLR	RW	8	0x0000 0085	0x80
OTHER_INT_EN_RISE_SET	RW	8	0x0000 0087	0x00
OTHER_INT_EN_RISE_CLR	RW	8	0x0000 0088	0x00
OTHER_INT_EN_FALL	RW	8	0x0000 0089	0x00
OTHER_INT_EN_FALL_SET	RW	8	0x0000 008A	0x00
OTHER_INT_EN_FALL_CLR	RW	8	0x0000 008B	0x00
OTHER_INT_STS	R	8	0x0000 008C	0x00
OTHER_INT_LATCH	R	8	0x0000 008D	0x00
Reserved for test	RW	8	0x0000 008E	0x00
Reserved for test	RW	8	0x0000 008F	0x00
Reserved for test	RW	8	0x0000 0090	0x00
Reserved for test	RW	8	0x0000 0091	0x00
Reserved for test	RW	8	0x0000 0092	0x00
Reserved for test	RW	8	0x0000 0093	0x00
Reserved for test	R	8	0x0000 0094	0x00
Reserved for test	R	8	0x0000 0095	0x00
ID_STATUS	R	8	0x0000 0096	0x00
CARKIT_SM_1_INT_EN	RW	8	0x0000 0097	0x00
CARKIT_SM_1_INT_EN_SET	RW	8	0x0000 0098	0x00
CARKIT_SM_1_INT_EN_CLR	RW	8	0x0000 0099	0x00
CARKIT_SM_1_INT_STS	R	8	0x0000 009A	0x00
CARKIT_SM_1_INT_LATCH	R	8	0x0000 009B	0x00
CARKIT_SM_2_INT_EN	RW	8	0x0000 009C	0x00
CARKIT_SM_2_INT_EN_SET	RW	8	0x0000 009D	0x00
CARKIT_SM_2_INT_EN_CLR	RW	8	0x0000 009E	0x00
CARKIT_SM_2_INT_STS	R	8	0x0000 009F	0x00
CARKIT_SM_2_INT_LATCH	R	8	0x0000 00A0	0x00
CARKIT_SM_CTRL	RW	8	0x0000 00A1	0x10
CARKIT_SM_CTRL_SET	RW	8	0x0000 00A2	0x08
CARKIT_SM_CTRL_CLR	RW	8	0x0000 00A3	0x08
CARKIT_SM_CMD	RW	8	0x0000 00A4	0x00
CARKIT_SM_CMD_SET	RW	8	0x0000 00A5	0x00
CARKIT_SM_CMD_CLR	RW	8	0x0000 00A6	0x00

Table 14-24. USB Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Reset Value
CARKIT_SM_CMD_STS	R	8	0x0000 00A7	0x00
CARKIT_SM_STATUS	R	8	0x0000 00A8	0x00
Reserved for test	R	8	0x0000 00A9	0x00
CARKIT_SM_ERR_STATUS	R	8	0x0000 00AA	0x00
CARKIT_SM_CTRL_STATE	RW	8	0x0000 00AB	0x00
POWER_CTRL	RW	8	0x0000 00AC	0x00
POWER_CTRL_SET	RW	8	0x0000 00AD	0x00
POWER_CTRL_CLR	RW	8	0x0000 00AE	0x00
OTHER_IFC_CTRL2	RW	8	0x0000 00AF	0x00
OTHER_IFC_CTRL2_SET	RW	8	0x0000 00B0	0x00
OTHER_IFC_CTRL2_CLR	RW	8	0x0000 00B1	0x00
REG_CTRL_EN	RW	8	0x0000 00B2	0x00
REG_CTRL_EN_SET	RW	8	0x0000 00B3	0x00
REG_CTRL_EN_CLR	RW	8	0x0000 00B4	0x00
REG_CTRL_ERROR	R	8	0x0000 00B5	0x00
OTHER_FUNC_CTRL2	RW	8	0x0000 00B8	0x00
OTHER_FUNC_CTRL2_SET	RW	8	0x0000 00B9	0x00
OTHER_FUNC_CTRL2_CLR	RW	8	0x0000 00BA	0x00
CARKIT_ANA_CTRL	RW	8	0x0000 00BB	0x00
CARKIT_ANA_CTRL_SET	RW	8	0x0000 00BC	0x00
CARKIT_ANA_CTRL_CLR	RW	8	0x0000 00BD	0x00
VBUS_DEBOUNCE	RW	8	0x0000 00C0	0xA0
ID_DEBOUNCE	RW	8	0x0000 00C1	0xA0
TPH_DP_CON_MIN	RW	8	0x0000 00C2	0x64
TPH_DP_CON_MAX	RW	8	0x0000 00C3	0x7F
TCR_DP_CON_MIN	RW	8	0x0000 00C4	0x6C
TCR_DP_CON_MAX	RW	8	0x0000 00C5	0x75
TPH_DP_PD_SHORT	RW	8	0x0000 00C6	0x64
TPH_CMD_DLY	RW	8	0x0000 00C7	0x20
TPH_DET_RST	RW	8	0x0000 00C8	0x01
TPH_AUD_BIAS	RW	8	0x0000 00C9	0x17
TCR_UART_DET_MIN	RW	8	0x0000 00CA	0x01
TCR_UART_DET_MAX	RW	8	0x0000 00CB	0x02
TPH_ID_INT_PW	RW	8	0x0000 00CD	0x36
TACC_ID_INT_WAIT	RW	8	0x0000 00CE	0x44
TACC_ID_INT_PW	RW	8	0x0000 00CF	0x07
TPH_CMD_WAIT	RW	8	0x0000 00D0	0x3B
TPH_ACK_WAIT	RW	8	0x0000 00D1	0x17
TPH_DP_DISC_DET	RW	8	0x0000 00D2	0x6B
VBAT_TIMER	RW	8	0x0000 00D3	0x04
CARKIT_4W_DEBUG	R	8	0x0000 00E0	0x00
CARKIT_5W_DEBUG	R	8	0x0000 00E1	0x00
Reserved for test	RW	8	0x0000 00EA	0x10
Reserved for test	RW	8	0x0000 00EB	0x10
Reserved for test	RW	8	0x0000 00EC	0x00
Reserved for test	RW	8	0x0000 00ED	0x00
Reserved for test	RW	8	0x0000 00EE	0x00

Table 14-24. USB Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Reset Value
Reserved for test	RW	8	0x0000 00EF	0x00
Reserved for test	RW	8	0x0000 00F0	0x00
Reserved for test	RW	8	0x0000 00F2	0x00
Reserved for test	RW	8	0x0000 00F3	0x00
Reserved for test	RW	8	0x0000 00F4	0x00
Reserved for test	RW	8	0x0000 00F5	0x00
Reserved for test	R	8	0x0000 00F6	0x00
Reserved for test	R	8	0x0000 00F7	0x00
Reserved for test	RW	8	0x0000 00FC	0x00
PHY_PWR_CTRL	RW	8	0x0000 00FD	0x00
PHY_CLK_CTRL	RW	8	0x0000 00FE	0x02
PHY_CLK_CTRL_STS	R	8	0x0000 00FF	0x00

Table 14-25. VENDOR_ID_LO

Address Offset	0x00
Description	Lower byte of vendor ID supplied by USB IF (Texas Instruments Vendor ID = 0x0451)
Type	R

7	6	5	4	3	2	1	0
VENDOR_ID							

Bits	Field Name	Description	Type	Reset
7:0	VENDOR_ID		R	0x51

Table 14-26. VENDOR_ID_HI

Address Offset	0x01
Description	Upper byte of vendor ID supplied by USB IF (Texas Instruments vendor ID = 0x0451)
Type	R

7	6	5	4	3	2	1	0
VENDOR_ID							

Bits	Field Name	Description	Type	Reset
7:0	VENDOR_ID		R	0x04

Table 14-27. PRODUCT_ID_LO

Address Offset	0x02
Description	Lower byte of product ID supplied by vendor (device product ID is 0xC002)
Type	R

7	6	5	4	3	2	1	0
PRODUCT_ID							

Bits	Field Name	Description	Type	Reset
7:0	PRODUCT_ID		R	0x02

Table 14-28. PRODUCT_ID_HI

Address Offset	0x03
Description	Upper byte of product ID supplied by vendor (device product ID is 0xC002)
Type	R

7	6	5	4	3	2	1	0
PRODUCT_ID							

Bits	Field Name	Description	Type	Reset
7:0	PRODUCT_ID		R	0xC0

Table 14-29. FUNC_CTRL

Address Offset	0x04
Description	Controls UTMI function settings of the PHY
Type	RW

7	6	5	4	3	2	1	0
Reserved	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	SUSPENDM	Active low PHY suspend. Puts PHY in low-power mode. In low-power mode, the PHY powers down all blocks except the FS receiver, OTG comparators, and the ULPI interface pins. The PHY automatically sets this bit to 1 when low-power mode is exited.	RW	1
5	RESET	Active high transceiver reset. Does not reset the ULPI interface or ULPI register set. Once set, the PHY asserts the DIR signal and resets the UTMI core. When the reset is complete, the PHY deasserts DIR and clears this bit. After deasserting DIR, the PHY reasserts DIR and sends an RX command update.	RW	0
4:3	OPMODE	Select the required bit encoding style during transmit. 0x0: Normal operation 0x1: Nondriving 0x2: Disable bit-stuff and NRZI encoding 0x3: Reserved	RW	0x0
2	TERMSELECT	Controls the internal 1.5-kΩ-pullup resistor and 45-Ω HS terminations. Control of bus resistors changes depending on XCVRSELECT, OPMODE, DPPULLDOWN, and DMPULLDOWN.	RW	0
1:0	XCVRSELECT	Select the required transceiver speed. 0x0: Enable HS transceiver. 0x1: Enable FS transceiver. 0x2: Enable LS transceiver. 0x3: Enable FS transceiver for LS packets (FS preamble is automatically prepended).	RW	0x1

Table 14-30. FUNC_CTRL_SET

Address Offset	0x05
Description	This register does not physically exist. It is the same as the FUNC_CTRL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	SUSPENDM		RW	1
5	RESET		RW	0
4:3	OPMODE		RW	0x0
2	TERMSELECT		RW	0
1:0	XCVRSELECT		RW	0x1

Table 14-31. FUNC_CTRL_CLR

Address Offset	0x06
Description	This register does not physically exist. It is the same as the FUNC_CTRL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	SUSPENDM		RW	1
5	RESET		RW	0
4:3	OPMODE		RW	0x0
2	TERMSELECT		RW	0
1:0	XCVRSELECT		RW	0x1

Table 14-32. IFC_CTRL

Address Offset	0x07
Description	Enables alternate interfaces and PHY features
Type	RW

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	Reserved	Reserved	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	Reserved

Bits	Field Name	Description	Type	Reset
7	INTERFACE_ PROTECT_ DISABLE	Controls circuitry built into the PHY to protect the ULPI interface when the link tristates STP and data. 0b: Enables the interface protect circuit 1b: Disables the interface protect circuit	RW	0
6	Reserved		R	0
5	Reserved		R	0
4	AUTORESUME	Enables the PHY to automatically transmit resume signaling. See USB specification 7.1.7.7 and 7.9 for more information. 0 = AUTORESUME disabled 1 = AUTORESUME enabled (default)	RW	1
3	CLOCK SUSPENDM	Active low clock suspend. Valid only in serial modes. Powers down only internal clock circuitry. Valid only when SUSPENDM = 1b. The PHY must ignore CLOCKSUSPENDM when SUSPENDM = 0b. 0b: Clock is not powered in serial and carkit modes. 1b: Clock is powered in serial and carkit modes. **Note:** By default, the clock is not powered down in serial or carkit mode.	RW	1
2	CARKITMODE	Changes the ULPI interface to carkit interface. The PHY automatically clears this field when carkit mode is exited. 0b: Carkit disabled 1b: Enable serial carkit mode.	RW	0
1	FSLSSERIALMODE_ 3PIN	Changes the ULPI interface to 3-pin serial mode using DAT/SE0 encoding. Alternately, changes the ULPI interface to 4-pin serial mode using VP/VM encoding if the FSLSSERIALMODE_ 4PIN bit in the OTHER_INTERFACE_CONTROL register is set. The PHY automatically clears this field when serial mode is exited. 0b: FS/LS packets are sent using the parallel interface. 1b: FS/LS packets are sent using the serial interface.	RW	0
0	Reserved		R	0

Table 14-33. IFC_CTRL_SET

Address Offset	0x08
Description	This register does not physically exist. It is the same as the IFC_CTRL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	Reserved	Reserved	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	Reserved

Bits	Field Name	Description	Type	Reset
7	INTERFACE_ PROTECT_ DISABLE		RW	0
6	Reserved		R	0
5	Reserved		R	0
4	AUTORESUME		RW	1
3	CLOCK SUSPENDM		RW	1
2	CARKITMODE		RW	0
1	FSLSSERIALMODE_ 3PIN		RW	0
0	Reserved		R	0

Table 14-34. IFC_CTRL_CLR

Address Offset	0x09
Description	This register does not physically exist. It is the same as the IFC_CTRL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	Reserved	Reserved	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	Reserved

Bits	Field Name	Description	Type	Reset
7	INTERFACE_ PROTECT_ DISABLE		RW	0
6	Reserved		R	0
5	Reserved		R	0
4	AUTORESUME		RW	1
3	CLOCK SUSPENDM		RW	1
2	CARKITMODE		RW	0
1	FSLSSERIALMODE_ 3PIN		RW	0
0	Reserved		R	0

Table 14-35. OTG_CTRL

Address Offset	0x0A
Description	Controls UTMI+ OTG functions of the PHY
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	DRVVBUS	Signals the internal charge pump to drive 5 V on VBUS 0b: Do not drive VBUS. 1b: Drive 5 V on VBUS.	RW	0
4	CHRGVBUS	Charge VBUS through a resistor. Used for VBUS pulsing SRP. The LINK must first check that VBUS has been discharged (see DISCHRGVBUS register bit), and that both D+ and D− data lines have been low (SE0) for 2 ms. 0b: Do not charge VBUS. 1b: Charge VBUS.	RW	0
3	DISCHRGVBUS	Discharge VBUS through a resistor. If the LINK sets this bit to 1, it waits for an RX CMD indicating that SESSEND transitioned from 0 to 1, and then resets this bit to 0 to stop the discharge. 0b: Do not discharge VBUS. 1b: Discharge VBUS.	RW	0
2	DMPULLDOWN	Enables the 15-kΩ pulldown resistor on D−. 0b: Pulldown resistor not connected to D−. 1b: Pulldown resistor connected to D−.	RW	1
1	DPPULLDOWN	Enables the 5 kΩ pulldown resistor on D+ 0b: Pulldown resistor not connected to D+ 1b: Pulldown resistor connected to D+	RW	1
0	IDPULLUP	Connects a pullup to the ID line and enables sampling of the signal level. 0b: Disable sampling of ID line. 1b: Enable sampling of ID line.	RW	0

Table 14-36. OTG_CTRL_SET

Address Offset	0x0B
Description	This register does not physically exist. It is the same as the OTG_CTRL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	DRVVBUS		RW	0
4	CHRGVBUS		RW	0
3	DISCHRGVBUS		RW	0
2	DMPULLDOWN		RW	1
1	DPPULLDOWN		RW	1
0	IDPULLUP		RW	0

Table 14-37. OTG_CTRL_CLR

Address Offset	0x0C
Description	This register does not physically exist. It is the same as the OTG_CTRL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	DRVVBUS		RW	0
4	CHRGVBUS		RW	0
3	DISCHRGVBUS		RW	0
2	DMPULLDOWN		RW	1
1	DPPULLDOWN		RW	1
0	IDPULLUP		RW	0

Table 14-38. USB_INT_EN_RISE

Address Offset	0x0D
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled.
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_RISE	Generate an interrupt event notification when IDGND changes from low to high. Event is automatically masked if the IDPULLUP bit is cleared to 0 and for ID_DEBOUNCE after IDPULLUP is set to 1.	RW	1
3	SESSEND_RISE	Generate an interrupt event notification when SESSEND changes from low to high.	RW	1
2	SESSVALID_RISE	Generate an interrupt event notification when SESSVALID changes from low to high. SESSVALID is the same as UTMI+ AValid.	RW	1
1	VBUSVALID_RISE	Generate an interrupt event notification when VBUSVALID changes from low to high.	RW	1
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when HOSTDISCONNECT changes from low to high. Applicable only in host mode (DPPULLDOWN and DMPULLDOWN both set to 1b).	RW	1

Table 14-39. USB_INT_EN_RISE_SET

Address Offset	0x0E
Description	This register does not physically exist. It is the same as the USB_INT_EN_RISE register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_RISE		RW	1
3	SESSEND_RISE		RW	1
2	SESSVALID_RISE		RW	1
1	VBUSVALID_RISE		RW	1
0	HOSTDISCONNECT_ RISE		RW	1

Table 14-40. USB_INT_EN_RISE_CLR

Address Offset	0xDF
Description	This register does not physically exist. It is the same as the USB_INT_EN_RISE register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_RISE		RW	1
3	SESSEND_RISE		RW	1
2	SESSVALID_RISE		RW	1
1	VBUSVALID_RISE		RW	1
0	HOSTDISCONNECT_RISE		RW	1

Table 14-41. USB_INT_EN_FALL

Address Offset	0x10
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled.
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_FALL	Generate an interrupt event notification when IDGND changes from high to low. Event is automatically masked if the IDPULLUP bit is cleared to 0 and for ID_DEBOUNCE after IDPULLUP is set to 1.	RW	1
3	SESSEND_FALL	Generate an interrupt event notification when SESSEND changes from high to low.	RW	1
2	SESSVALID_FALL	Generate an interrupt event notification when SESSVALID changes from high to low. SESSVALID is the same as UTMI+ AValid.	RW	1
1	VBUSVALID_FALL	Generate an interrupt event notification when VBUSVALID changes from high to low.	RW	1
0	HOSTDISCONNECT_FALL	Generate an interrupt event notification when HOSTDISCONNECT changes from high to low. Applicable only in host mode (DPPULLDOWN and DMPULLDOWN both set to 1b).	RW	1

Table 14-42. USB_INT_EN_FALL_SET

Address Offset	0x11
Description	This register does not physically exist. It is the same as the USB_INT_EN_FALL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_FALL		RW	1
3	SESSEND_FALL		RW	1
2	SESSVALID_FALL		RW	1

Bits	Field Name	Description	Type	Reset
1	VBUSVALID_FALL		RW	1
0	HOSTDISCONNECT_FALL		RW	1

Table 14-43. USB_INT_EN_FALL_CLR

Address Offset	0x12
Description	This register does not physically exist. It is the same as the USB_INT_EN_FALL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_FALL		RW	1
3	SESSEND_FALL		RW	1
2	SESSVALID_FALL		RW	1
1	VBUSVALID_FALL		RW	1
0	HOSTDISCONNECT_FALL		RW	1

Table 14-44. USB_INT_STS

Address Offset	0x13
Description	Indicates the current value of the interrupt source signal
Type	R

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND	SESSEND	SESSVALID	VBUSVALID	HOSTDISCONNECT

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0

Bits	Field Name	Description	Type	Reset
4	IDGND	Current value of UTMI+ IDGND output. This bit is not updated if the IDPULLUP bit is reset to 0 and for ID_DEBOUNCE after IDPULLUP is set to 1.	R	0
3	SESSEND	Current value of UTMI+ SESSEND output	R	0
2	SESSVALID	Current value of UTMI+ SESSVALID output. SESSVALID is the same as UTMI+ AValid.	R	0
1	VBUSVALID	Current value of UTMI+ VBUSVALID output	R	0
0	HOSTDISCONNECT	Current value of UTMI+ HOSTDISCONNECT output. Applicable only in host mode. Automatically reset to 0 when low-power mode is entered.	R	1

Table 14-45. USB_INT_LATCH

Address Offset	0x14
Description	These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY automatically clears all bits when the LINK reads this register, or when low-power mode is entered. The PHY also clears this register when serial mode or carkit mode is entered, regardless of the value of CLOCKSUSPENDM. The PHY follows the rules defined in Table 26 of the ULPI specification for setting any latch register bit. **Note:** If register read data is returned to the LINK in the same cycle that a USB interrupt latch bit is to be set, the interrupt condition is given immediately in the register read data and the latch bit is not set. It is not necessary for the LINK to read the USB interrupt latch register in synchronous mode, because the RX CMD byte already directly indicates the interrupt source.
Type	R

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_LATCH	SESSEND_LATCH	SESSVALID_LATCH	VBUSVALID_LATCH	HOSTDISCONNECT_LATCH

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_LATCH	Set to 1 by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read.	R	0
3	SESSEND_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read.	R	0
2	SESSVALID_ LATCH	Set to 1 by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read. SessValid is the same as UTMI+ AValid.	R	0
1	VBUSVALID_ LATCH	Set to 1 by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read.	R	0
0	HOSTDISCONNECT_ LATCH	Set to 1 by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode.	R	1

Table 14-46. DEBUG

Address Offset	0x15
Description	Indicates the current value of signals useful for debugging
Type	R

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LINESTATE	

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1:0	LINESTATE	These signals reflect the current state of the single-ended receivers. They directly reflect the current state of the DP (LINESTATE[0]) and DM (LINESTATE [1]) signals. Read 0x0: SE0 (LS/FS), Squelch (HS/Chirp) Read 0x1: LS: K state FS: J state HS: !Squelch Chirp: !Squelch & HS_Differential_Receiver_Output Read 0x2: LS: J state FS: K state HS: Invalid Chirp: !Squelch & !HS_Differential_ Receiver_Output Read 0x3: SE1 (LS/FS), Invalid (HS/Chirp)	R	0x0

Table 14-47. SCRATCH_REG

Address Offset	0x16
Description	Empty register byte for testing. Software can read, write, set, and clear this register, and PHY functionality is not affected.
Type	RW

7	6	5	4	3	2	1	0
SCRATCH							

Bits	Field Name	Description	Type	Reset
7:0	SCRATCH	Scratch data	RW	0x00

Table 14-48. SCRATCH_REG_SET

Address Offset	0x17
Description	This register does not physically exist. It is the same as the SCRATCH_REG register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
SCRATCH							

Bits	Field Name	Description	Type	Reset
7:0	SCRATCH		RW	0x00

Table 14-49. SCRATCH_REG_CLR

Address Offset	0x18
Description	This register does not physically exist. It is the same as the SCRATCH_REG with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
SCRATCH							

Bits	Field Name	Description	Type	Reset
7:0	SCRATCH		RW	0x00

Table 14-50. CARKIT_CTRL

Address Offset	0x19
Description	Controls the operation of the carkit circuitry in the PHY. Valid only if CARKITMODE in the INTERFACE_CONTROL register is set to 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	MICEN	SPKRIGHTEN	SPKLEFTEN	RXDEN	TXDEN	IDGNDDRV	CARKITPWR

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	MICEN	Routes analog audio signal from D+ pin to the microphone amplifier input This bit must not be set if the VOICESW bit in the MCPC_CONTROL register is set to 1.	RW	0
5	SPKRIGHTEN	Routes speaker right analog audio amplifier output to D+ pin (must only be set for CEA-936-A stereo mode). This bit must not be set if the VOICESW bit in the MCPC_CONTROL register is set to 1.	RW	0
4	SPKLEFTEN	Routes speaker left analog audio amplifier output to D− pin. If set, also forces UART over audio pulse mode. This bit must not be set if the VOICESW bit in the MCPC_CONTROL register is set to 1.	RW	0
3	RXDEN	Routes RXD signal from D+ pin to DATA[1] pin. This bit must not be set if the HS_UART bit in the MCPC_CONTROL register is set to 1. 0b: D+ paths open if CARKITMODE = 1 (incoming signal from D+ pin is don't care, DATA[1] is held high if HS_UART = 0) 1b: D+ → DATA[1]	RW	0

Bits	Field Name	Description	Type	Reset
2	TXDEN	Routes TXD signal from DATA[0] pin onto D− pin. This bit must not be set if the HS_UART bit in the MCPC_CONTROL register is set to 1. 0b: D− paths open if CARKITMODE = 1 (incoming signal from DATA[0] pin is don't care, D− is held high if HS_UART = 0 and not in audio mode) 1b: DATA[0] → D−	RW	0
1	IDGNDDRV	Drives ID pin to ground	RW	0
0	CARKITPWR	Applies power to carkit circuitry: MCPC and CEA carkit audio drivers, CEA carkit comparator	RW	0

Table 14-51. CARKIT_CTRL_SET

Address Offset	0x1A
Description	This register does not physically exist. It is the same as the CARKIT_CTRL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	MICEN	SPKRIGHTEN	SPKLEFTEN	RXDEN	TXDEN	IDGNDDRV	CARKITPWR

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	MICEN		RW	0
5	SPKRIGHTEN		RW	0
4	SPKLEFTEN		RW	0
3	RXDEN		RW	0
2	TXDEN		RW	0
1	IDGNDDRV		RW	0
0	CARKITPWR		RW	0

Table 14-52. CARKIT_CTRL_CLR

Address Offset	0x1B
Description	This register does not physically exist. It is the same as the CARKIT_CTRL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	MICEN	SPKRIGHTEN	SPKLEFTEN	RXDEN	TXDEN	IDGNDDRV	CARKITPWR

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	MICEN		RW	0
5	SPKRIGHTEN		RW	0
4	SPKLEFTEN		RW	0
3	RXDEN		RW	0
2	TXDEN		RW	0
1	IDGNDDRV		RW	0
0	CARKITPWR		RW	0

Table 14-53. CARKIT_INT_DELAY

Address Offset	0x1C
Description	Controls TPH_STLO_DET timing during CEA carkit stereo mode. If the CARINTDET bit in the CARKIT_INT_LATCH register and the SPKRRIGHTBIASEN bit in the CARKIT_PULSE_CONTROL register are set, the carkit interrupt timer increments when the D+ voltage is below VPH_DP_LO. It resets if the D+ voltage is above VPH_DP_LO. When the timer reaches the value stored in CarIntDly, a CarIntDet event is generated (see Table 14-58). **Note:** Definition changed from ULPI1.1 definition (because CEA carkit specification was modified). The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1. For this implementation, the MSB is reserved for the counter value.
Type	RW

7	6	5	4	3	2	1	0
Reserved	CARINTDLY						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	CARINTDLY	Stereo pulse width	RW	0x52

Table 14-54. CARKIT_INT_EN

Address Offset	0x1D
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes.
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	CARDP_FALL_EN	CARDP_RISE_EN	CARINTDET_EN	IDFLOAT_FALL_EN	IDFLOAT_RISE_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	CARDP_FALL_EN	Generate an interrupt event notification when a falling voltage on the D+ line crosses the VPH_DP_LO threshold. **Caution:** Do not set if RXPLSEN in the CARKIT_PULSE_CONTROL register is set.	RW	0
3	CARDP_RISE_EN	Generate an interrupt event notification when a rising voltage on the D+ line crosses the VPH_DP_LO threshold. **Caution:** Do not set if RXPLSEN in the CARKIT_PULSE_CONTROL register is set.	RW	0
2	CARINTDET_EN	Generate an interrupt event notification when the carkit interrupt timer reaches the value stored in the carkit interrupt delay register. This bit is set only during stereo mode (SPKRIGHTEN is set and MICEN is cleared in the CARKIT_CONTROL register). 0b: Disabled 1b: Enabled	RW	0
1	IDFLOAT_FALL_EN	Generate an interrupt event notification when the ID pin changes from floating to not floating. The IDPULLUP bit in the OTG CONTROL register must be set.	RW	0

Bits	Field Name	Description	Type	Reset
0	IDFLOAT_RISE_EN	Generate an interrupt event notification when the ID pin changes from not floating to floating. The IDPULLUP bit in the OTG CONTROL register must be set.	RW	0

Table 14-55. CARKIT_INT_EN_SET

Address Offset	0x1E
Description	This register does not physically exist. It is the same as the CARKIT_INT_EN register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	CARDP_FALL_EN	CARDP_RISE_EN	CARINTDET_EN	IDFLOAT_FALL_EN	IDFLOAT_RISE_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	CARDP_FALL_EN		RW	0
3	CARDP_RISE_EN		RW	0
2	CARINTDET_EN		RW	0
1	IDFLOAT_FALL_EN		RW	0
0	IDFLOAT_RISE_EN		RW	0

Table 14-56. CARKIT_INT_EN_CLR

Address Offset	0x1F
Description	This register does not physically exist. It is the same as the CARKIT_INT_EN register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	CARDP_FALL_EN	CARDP_RISE_EN	CARINTDET_EN	IDFLOAT_FALL_EN	IDFLOAT_RISE_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	CARDP_FALL_EN		RW	0
3	CARDP_RISE_EN		RW	0

Bits	Field Name	Description	Type	Reset
2	CARINTDET_EN		RW	0
1	IDFLOAT_FALL_EN		RW	0
0	IDFLOAT_RISE_EN		RW	0

Table 14-57. CARKIT_INT_STS

Address Offset	0x20
Description	When a carkit interrupt event notification occurs, the LINK can read this register to determine which event triggered the interrupt.
Type	R

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	CARDP	CARINTDET	IDFLOAT

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	CARDP	Asserted when the D+ line is above the VPH_DP_LO threshold	R	0
1	CARINTDET	Asserted when the CARINTDET bit in the CARKIT INTERRUPT LATCH register is set	R	0
0	IDFLOAT	Asserted when the ID pin is floating	R	0

Table 14-58. CARKIT_INT_LATCH

Address Offset	0x21
Description	These bits are set by the PHY when an unmasked carkit event occurs. The PHY automatically clears all bits when the LINK reads this register, or when low-power mode is entered. **Note:** If register read data is returned to the LINK in the same cycle that a carkit interrupt latch bit is to be set, the interrupt condition is given immediately in the register read data and the latch bit is not set.
Type	R

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	CARDP	CARINTDET	IDFLOAT

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	CARDP	Asserted if the CARDP_FALL bit in the CARKIT_ INTERRUPT_ENABLE register is set when a falling voltage on the D+ line crosses the VPH_DP_LO threshold. Also asserted if the CARDP_RISE bit is set when a rising voltage crosses the VPH_DP_LO threshold.	R	0
1	CARINTDET	Asserted if the CARINTDET bit in the CARKIT INTERRUPT ENABLE register is set and the carkit interrupt timer reaches the value stored in the CARKIT_ INTERRUPT_DELAY register. This bit is used only to detect an interrupt from a CEA carkit during stereo audio.	R	0

Bits	Field Name	Description	Type	Reset
0	IDFLOAT	Asserted if the IDFLOAT RISE bit in the CARKIT INTERRUPT ENABLE register is set, and the ID line changes from not floating to floating. Also asserted if the IDFLOAT FALL bit in the CARKIT INTERRUPT ENABLE register is set, and the ID line changes from floating to not floating.	R	0

Table 14-59. CARKIT_PLS_CTRL

Address Offset	0x22
Description	This register controls the operation of the carkit DDA function in the PHY. The TXPLSEN and RXPLSEN bits are ignored if the CARKITMODE bit in the interface control register is not set.
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	SPKRRIGHTBIASEN	SPKRLEFTBIASEN	RXPLSEN	TXPLSEN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	SPKRRIGHT BIASEN	Enables bias for the right speaker (stereo mode only) 0 = Disabled 1 = Enabled	RW	0
2	SPKRLEFT BIASEN	Enables bias for the left speaker 0 = Disabled 1 = Enabled	RW	0
1	RXPLSEN	Enables DDA pulse receive When the RXPLSEN bit is set and the MICEN bit in the CARKIT_CTRL register is set, the PHY toggles the data(1) output when a falling edge is detected on the D+ line that crosses the carkit interrupt threshold of VPH_DP_LO. When the RXPLSEN bit is set, the receive polarity recovery timer is enabled. 0 = Disabled (a negative pulse on D+ is a carkit interrupt) 1 = Enabled (a negative pulse on D+ is a UART RX transition)	RW	0
0	TXPLSEN	Enables DDA pulse transmit When the TXPLSEN bit is set and the SPKLEFTEN bit in the CARKIT CONTROL register is set, the PHY outputs a positive pulse followed by a negative pulse on the D− line after each rising or falling edge on the data(0) line. 0b: Transmit DDA disabled 1b: Transmit DDA enabled	RW	0

Table 14-60. CARKIT_PLS_CTRL_SET

Address Offset	0x23
Description	This register does not physically exist. It is the same as the CARKIT_PLS_CTRL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	SPKRRIGHTBIASEN	SPKRLEFTBIASEN	RXPLSEN	TXPLSEN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	SPKRRIGHT BIASEN		RW	0
2	SPKRLEFT BIASEN		RW	0
1	RXPLSEN		RW	0
0	TXPLSEN		RW	0

Table 14-61. CARKIT_PLS_CTRL_CLR

Address Offset	0x24
Description	This register does not physically exist. It is the same as the CARKIT_PLS_CTRL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	SPKRRIGHTBIASEN	SPKRLEFTBIASEN	RXPLSEN	TXPLSEN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	SPKRRIGHT BIASEN		RW	0
2	SPKRLEFT BIASEN		RW	0
1	RXPLSEN		RW	0
0	TXPLSEN		RW	0

Table 14-62. TRANS_POS_WIDTH

Address Offset	0x25
Description	This register specifies the width of the positive pulse that is output on the D− line when the TXPLSEN bit is set. The time is measured in units of 60-MHz clock periods.
Type	RW

7	6	5	4	3	2	1	0
TXPOSWDTH							

Bits	Field Name	Description	Type	Reset
7:0	TXPOSWDTH	Transmit positive pulse width. Default value is 450 ns.	RW	0x1B

Table 14-63. TRANS_NEG_WIDTH

Address Offset	0x26
Description	This register specifies the width of the negative pulse that is output on the D− line when the TXPLSEN bit is set. The time is measured in units of 60-MHz clock periods.
Type	RW

7	6	5	4	3	2	1	0
TXNEGWDTH							

Bits	Field Name	Description	Type	Reset
7:0	TXNEGWDTH	Transmit negative pulse width. Default value is 200 ns.	RW	0x0C

Table 14-64. RCV_PLTY_RECOVERY

Address Offset	0x27
Description	When the DDA feature is enabled in the carkit, the carkit sends UART data to the phone by converting the NRZ UART signal to a series of pulses, and transmitting these pulses to the phone on the D+ line. The PHY in the phone converts these pulses back to an NRZ UART signal by toggling to the data(1) line when a pulse is received. If the PHY misses a pulse or detects an extra pulse, the polarity on the data(1) line is incorrect. To recover from this condition, the PHY automatically resets the polarity of the data(1) line to logic high when the polarity of the data(1) line has been logic low for the time specified in the receive polarity recovery register. The receive polarity recovery is active only if the RXPLSEN bit in the carkit pulse control register is set. The time is measured in units of 0.25 ms. The minimum RxPolRcvry that must be supported is 1. The maximum RxPolRcvry that must be supported is 255. When 00000000 is written into this register, the function is disabled.
Type	RW

7	6	5	4	3	2	1	0
RXPOLRCVRY							

Bits	Field Name	Description	Type	Reset
7:0	RXPOLRCVRY	Receive polarity recovery time The time is measured in units of 0.25 ms. The minimum RxPolRcvry that must be supported is 1. The maximum RxPolRcvry that must be supported is 255. When 00000000 is written into this register, the function is disabled. Reset value is 40 ms.	RW	0xA0

Table 14-65. MCPC_CTRL

Address Offset	0x30
Description	This register provides additional control for digital and analog audio paths in support of an MCPC application.
Type	RW

7	6	5	4	3	2	1	0
RTSOL	EXTSWR	EXTSWC	VOICESW	OUT64K	RTSCTSSW	Reserved	HS_UART

Bits	Field Name	Description	Type	Reset
7	RTSOL	Drives a low signal on RTSO	RW	0
6	EXTSWR	Routes BERCLK pin (input) to RTSO pin (output). This bit is set only when 64KOUT, RTSCTSSW, RTSOL, and VOICESW bits are cleared. 0b: Path open 1b: BERCLK => RTSO (if 64KOUT = 0 and RTSCTSSW = 0 and RTSOL = 0 and VOICESW = 0)	RW	0
5	EXTSWC	Routes BERDATA pin (input) to CTSI pin (also enables CTSI as an output). This bit is set only when RTSCTSSW and VOICESW bits are cleared. 0b: Path open 1b: BERDATA => CTSI (if RTSCTSSW = 0 and VOICESW = 0)	RW	0
4	VOICESW	Routes speaker left analog audio amplifier output to RXAF pin and analog audio signal from TXAF pin to the microphone amplifier input. This bit must not be set if any of the MICEN, SPKLEFTEN, or SPKRIGHTEN bits in the CARKIT_CTRL register are set to 1.	RW	0
3	OUT64K	Output a 64-kHz signal on the RSTO pin. This bit is set only when EXTSWR, RTSCTSSW, RTSOL, and VOICESW bits are cleared. 0b: Path open 1b: 64 kHz => RTSO (if EXTSWR = 0 and RTSCTSSW = 0 and RTSOL = 0 and VOICESW = 0)	RW	0
2	RTSCTSSW	Routes RTS signal from DATA(2) pin to RTS0 and CTS signal from CTSI pin to DATA(3) pin. 0b: Paths open 1b: DATA[2] => RTSO, CTSI => DATA[3]	RW	0
1	Reserved		R	0
0	HS_UART	Routes UART TXD signal from DATA[0] pin to HSTXD pin and RXD signal from HSRXD pin to DATA[1] pin This bit is not set if the RXDEN bit in the CARKIT_CTRL register is set to 1. 0b: HS paths open (TXD signal to HS IF held high, incoming signal from HSRXD pin is don't care) 1b: DATA[0] => HSTXD, HSRXD => DATA[1]	RW	0

Table 14-66. MCPC_CTRL_SET

Address Offset	0x31
Description	This register does not physically exist. It is the same as the MCPC_CTRL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
RTSOL	EXTSWR	EXTSWC	VOICESW	OUT64K	RTSCTSSW	Reserved	HS_UART

Bits	Field Name	Description	Type	Reset
7	RTSOL		RW	0
6	EXTSWR		RW	0
5	EXTSWC		RW	0
4	VOICESW		RW	0
3	OUT64K		RW	0

Bits	Field Name	Description	Type	Reset
2	RTSCTSSW		RW	0
1	Reserved		R	0
0	HS_UART		RW	0

Table 14-67. MCPC_CTRL_CLR

Address Offset	0x32
Description	This register does not physically exist. It is the same as the MCPC_CTRL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
RTSOL	EXTSWR	EXTSWC	VOICESW	OUT64K	RTSCTSSW	Reserved	HS_UART

Bits	Field Name	Description	Type	Reset
7	RTSOL		RW	0
6	EXTSWR		RW	0
5	EXTSWC		RW	0
4	VOICESW		RW	0
3	OUT64K		RW	0
2	RTSCTSSW		RW	0
1	Reserved		R	0
0	HS_UART		RW	0

Table 14-68. MCPC_IO_CTRL

Address Offset	0x33
Description	This register provides additional control for configuring the device I/Os in support of an MCPC application.
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	MICBIASEN	CTS_NPU	RXD_PU	TXDTYP	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	MICBIASEN	Enables bias for microphone amplifier. This mode is used only for MCPC operation where microphone TXAF input is ac-coupled to the MCPC connector in the phone.	RW	0
4	CTS_NPU	Deasserts the 4.7 − 10K internal pullup on CTSI pin 0b: No pullup on CTSI 1b: Pullup value is per MCPC specification. **Note:** CTSI pullup is automatically disabled when the MCPC_CTRL[6] EXTSWR bit = 1 and the MCPC_CTRL[5] EXTSWC bit = 1 (BER mode).	RW	0

Bits	Field Name	Description	Type	Reset
3	RXD_PU	Asserts a 4.7−10K pullup on D+ (RXD) pin and configures D− (TXD) in open-drain mode 0b: Pullup value is per USB ECN value if asserted (see TERMSELECT in the FUNCTION_CONTROL register) and D− is in CMOS mode. 1b: Pullup value is per MCPC specification and D− is in open-drain mode. **Note:** RXD_PU must be set after the MCPC_CK_EN bit in the MCPC_CTRL2 register, because, although the ULPI interface is in synchronous mode (the default), the data sent to the MCPC driver is tied low.	RW	0
2	TXDTYP	Enable the MCPC data transmit path when D− is set in open-drain mode by RXD_PU: 0b: MCPC UART transmit path is enabled. 1b: MCPC UART transmit path is disabled. **Note:** This bit has no effect if RXD_PU = 0. **Note:** TXDTYP must be set after the MCPC_CK_EN bit in the MCPC_CTRL2 register, because, although the ULPI interface is in synchronous mode (the default), the data sent to the MCPC driver is tied low.	RW	1
1	Reserved		RW	0
0	Reserved		RW	0

Table 14-69. MCPC_IO_CTRL_SET

Address Offset	0x34
Description	This register does not physically exist. It is the same as the MCPC_IO_CTRL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	MICBIASEN	CTS_NPU	RXD_PU	TXDTYP	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	MICBIASEN		RW	0
4	CTS_NPU		RW	0
3	RXD_PU		RW	0
2	TXDTYP		RW	1
1	Reserved		RW	0
0	Reserved		RW	0

Table 14-70. MCPC_IO_CTRL_CLR

Address Offset	0x35
Description	This register does not physically exist. It is the same as the MCPC_IO_CTRL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	MICBIASEN	CTS_NPU	RXD_PU	TXDTYP	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	MICBIASEN		RW	0
4	CTS_NPU		RW	0
3	RXD_PU		RW	0
2	TXDTYP		RW	1
1	Reserved		RW	0
0	Reserved		RW	0

Table 14-71. MCPC_CTRL2

Address Offset	0x36
Description	This register provides additional control for support of an MCPC application.
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCPC_CK_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	Reserved		R	0
0	MCPC_CK_EN	Enable MCPC UART mode (must not be set if CARKITMODE is set in IFC_CTRL register) 0b: All modes except MCPC UART 1b: UART operation for MCPC	RW	0

Table 14-72. MCPC_CTRL2_SET

Address Offset	0x37
Description	This register does not physically exist. It is the same as the MCPC_CTRL2 register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCPC_CK_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	Reserved		R	0
0	MCPC_CK_EN		RW	0

Table 14-73. MCPC_CTRL2_CLR

Address Offset	0x38
Description	This register does not physically exist. It is the same as the MCPC_CTRL2 register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCPC_CK_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	Reserved		R	0
0	MCPC_CK_EN		RW	0

Table 14-74. OTHER_FUNC_CTRL

Address Offset	0x80
Description	Provides additional control for carkit support
Type	RW

7	6	5	4	3	2	1	0
DM_PULLUP	DP_PULLUP	Reserved	BDIS_ACON_EN	Reserved	FIVEWIRE_MODE	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7	DM_PULLUP	Enables the pullup resistor on D− 0b: Pullup resistor not connected to D− 1b: Pullup resistor connected to D−	RW	0
6	DP_PULLUP	Enables the pullup resistor on D+ 0b: Pullup resistor not connected to D+ 1b: Pullup resistor connected to D+	RW	0
5	Reserved	Enables A-device to connect if B-device disconnect is detected. Conditions: Detect a continuous SE0 on the line for >2.5 μs. A USB reset from the A-device is ignored. 0b: No action 1b: Automatically asserts a pullup on D+ to connect after B-device disconnect Not implemented in current design	R	0
4	BDIS_ACON_EN	Enables A-device to connect if B-device disconnect is detected Conditions: Detect a continuous SE0 on the line for > 2.5 μs. A USB reset from the A-device is ignored. 0b: No action 1b: Automatically asserts a pullup on D+ to connect after B-device disconnect	RW	0

Bits	Field Name	Description	Type	Reset
3	Reserved	Enables A-device to connect if B-device disconnect is detected. Conditions: Detect a continuous SE0 on the line for > 2.5 μs. A USB reset from the A-device is ignored. 0b: No action 1b: Automatically asserts a pullup on D+ to connect after B-device disconnect Not implemented in current design	R	0
2	FIVEWIRE_MODE	If in carkit, use 5-wire protocol instead of 4-wire. 0b: 4-wire CEA carkit 1b: 5-wire CEA carkit	RW	0
1	Reserved		R	0
0	Reserved		R	0

Table 14-75. OTHER_FUNC_CTRL_SET

Address Offset	0x81
Description	This register does not physically exist. It is the same as the OTHER_FUNC_CTRL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved(T)	Reserved(T)	Reserved	BDIS_ACON_EN	Reserved	FIVEWIRE_MODE	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7	Reserved(T)		RW	0
6	Reserved(T)		RW	0
5	Reserved		R	0
4	BDIS_ACON_EN		RW	0
3	Reserved		R	0
2	FIVEWIRE_MODE		RW	0
1	Reserved		R	0
0	Reserved		R	0

Table 14-76. OTHER_FUNC_CTRL_CLR

Address Offset	0x82
Description	This register does not physically exist. It is the same as the OTHER_FUNC_CTRL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved(T)	Reserved(T)	Reserved	BDIS_ACON_EN	Reserved	FIVEWIRE_MODE	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7	Reserved(T)		RW	0
6	Reserved(T)		RW	0
5	Reserved		R	0
4	BDIS_ACON_EN		RW	0
3	Reserved		R	0
2	FIVEWIRE_MODE		RW	0
1	Reserved		R	0
0	Reserved		R	0

Table 14-77. OTHER_IFC_CTRL

Address Offset	0x83
Description	This register is used to reroute the module interrupts to the device instead of to ULPI and to optionally tristate the ULPI I/F. It can be accessed only through I^2C.
Type	RW

7	6	5	4	3	2	1	0
Reserved(T)	OE_INT_EN	CEA2011_MODE	FSLSSERIALMODE_4PIN	HIZ_ULPI_60MHZ_OUT	HIZ_ULPI	Reserved	ALT_INT_REROUTE

Bits	Field Name	Description	Type	Reset
7	Reserved(T)	Test bit – Must remain set to 1 for normal operation	RW	1
6	OE_INT_EN	Enables interrupt to be signaled on OE_INTN (ULPI DAT2) pin. This bit is set if the CEA2011_MODE bit is set. 0b: No effect 1b: Allows interrupt support on OE_INTN pin	RW	0
5	CEA2011_MODE	Compatibility mode with legacy with USB FS/UART interconnect based on CEA-2011 specification 0b: ULPI mode 1b: CEA-2011 mode	RW	0
4	FSLSSERIALMODE_ 4PIN	Modify the behavior of the FSLSSERIALMODE_3PIN bit in the INTERFACE_CONTROL register. 0b: No effect 1b: Use VP/VM encoding instead of DAT/SE0.	RW	0
3	HIZ_ULPI_60MHZ_ OUT	Tristate 11-pin of the ULPI interface. The clock pin output a 60-MHz clock. 0b: Normal operation 1b: Output 60-MHz clock + HiZ the other 11 ULPI pins	RW	0
2	HIZ_ULPI	Tristate the 12-pin of the ULPI interface including the clock pin. 0b: Normal operation 1b: HiZ the 12-pin ULPI bus	RW	0
1	Reserved		R	0
0	ALT_INT_ REROUTE	Routes interrupt as a device interrupt instead of using an ULPI RX command (ALT_INT bit remains unasserted if any other RX command is sent by the PHY) 0b: Interrupts are signaled using an RX command (ULPI) with ALT_INT bit set. 1b: Interrupts are signaled as a device interrupt.	RW	0

Table 14-78. OTHER_IFC_CTRL_SET

Address Offset	0x84
Description	This register does not physically exist. It is the same as the OTHER_IFC_CTRL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved(T)	OE_INT_EN	CEA2011_MODE	FSLSSERIALMODE_4PIN	HIZ_ULPI_60MHZ_OUT	HIZ_ULPI	Reserved	ALT_INT_REROUTE

Bits	Field Name	Description	Type	Reset
7	Reserved(T)		RW	1
6	OE_INT_EN		RW	0
5	CEA2011_MODE		RW	0
4	FSLSSERIALMODE_ 4PIN		RW	0
3	HIZ_ULPI_60MHZ_ OUT		RW	0
2	HIZ_ULPI		RW	0
1	Reserved		R	0
0	ALT_INT_ REROUTE		RW	0

Table 14-79. OTHER_IFC_CTRL_CLR

Address Offset	0x85
Description	This register does not physically exist. It is the same as the OTHER_IFC_CTRL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved(T)	OE_INT_EN	CEA2011_MODE	FSLSSERIALMODE_4PIN	HIZ_ULPI_60MHZ_OUT	HIZ_ULPI	Reserved	ALT_INT_REROUTE

Bits	Field Name	Description	Type	Reset
7	Reserved(T)		RW	1
6	OE_INT_EN		RW	0
5	CEA2011_MODE		RW	0
4	FSLSSERIALMODE_ 4PIN		RW	0
3	HIZ_ULPI_60MHZ_ OUT		RW	0

Bits	Field Name	Description	Type	Reset
2	HIZ_ULPI		RW	0
1	Reserved		R	0
0	ALT_INT_ REROUTE		RW	0

Table 14-80. OTHER_INT_EN_RISE

Address Offset	0x86
Description	If set, the bits in this register generate an interrupt event notification when the corresponding PHY signal changes.
Type	RW

7	6	5	4	3	2	1	0
VB_SESS_VLD_RISE_EN	DM_HI_RISE_EN	DP_HI_RISE_EN	Reserved	BDIS_ACON_RISE_EN	Reserved	MANU_RISE_EN	ABNORMAL_STRESS_RISE_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_ RISE_EN	If this bit is set, it generates an interrupt event notification when the VB_SESS_VLD pin changes from low to high.	RW	0
6	DM_HI_RISE_EN	If this bit is set, it generates an interrupt event notification when the DM_HI pin changes from low to high.	RW	0
5	DP_HI_RISE_EN	If this bit is set, it generates an interrupt event notification when the DP_HI pin changes from low to high.	RW	0
4	Reserved		R	0
3	BDIS_ACON_ RISE_EN	If this bit is set, it generates an interrupt event notification when a pullup is automatically asserted on D+ after B-device disconnect.	R	0
2	Reserved		R	0
1	MANU_RISE_EN	If this bit is set, it generates an interrupt event notification when the MANU pin changes from low to high.	RW	0
0	ABNORMAL_ STRESS_ RISE_EN	If this bit is set, it generates an interrupt event notification if the stress protection circuit is active.	RW	0

Table 14-81. OTHER_INT_EN_RISE_SET

Address Offset	0x87
Description	This register does not physically exist. It is the same as the OTHER_INT_EN_RISE register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
VB_SESS_VLD_RISE_EN	DM_HI_RISE_EN	DP_HI_RISE_EN	Reserved	BDIS_ACON_RISE_EN	Reserved	MANU_RISE_EN	ABNORMAL_STRESS_RISE_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_ RISE_EN		RW	0
6	DM_HI_RISE_EN		RW	0
5	DP_HI_RISE_EN		RW	0
4	Reserved		R	0
3	BDIS_ACON_ RISE_EN		R	0
2	Reserved		R	0
1	MANU_RISE_EN		RW	0
0	ABNORMAL_ STRESS_ RISE_EN		RW	0

Table 14-82. OTHER_INT_EN_RISE_CLR

Address Offset	0x88
Description	This register does not physically exist. It is the same as the OTHER_INT_EN_RISE register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
VB_SESS_VLD_RISE_EN	DM_HI_RISE_EN	DP_HI_RISE_EN	Reserved	BDIS_ACON_RISE_EN	Reserved	MANU_RISE_EN	ABNORMAL_STRESS_RISE_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_RISE_EN		RW	0
6	DM_HI_RISE_EN		RW	0
5	DP_HI_RISE_EN		RW	0
4	Reserved		R	0
3	BDIS_ACON_ RISE_EN		R	0
2	Reserved		R	0
1	MANU_RISE_EN		RW	0
0	ABNORMAL_STRESS_ RISE_EN		RW	0

Table 14-83. OTHER_INT_EN_FALL

Address Offset	0x89
Description	If set, the bits in this register generate an interrupt event notification when the corresponding PHY signal changes.
Type	RW

7	6	5	4	3	2	1	0
VB_SESS_VLD_FALL_EN	DM_HI_FALL_EN	DP_HI_FALL_EN	Reserved	Reserved	Reserved	MANU_FALL_EN	ABNORMAL_STRESS_FALL_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_ FALL_EN	If this bit is set, it generates an interrupt event notification when the VB_SESS_VLD pin changes from low to high.	RW	0
6	DM_HI_FALL_EN	If this bit is set, it generates an interrupt event notification when the DM_HI pin changes from low to high.	RW	0
5	DP_HI_FALL_EN	If this bit is set, it generates an interrupt event notification when the DP_HI pin changes from low to high.	RW	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	MANU_FALL_EN	If this bit is set, it generates an interrupt event notification when the MANU pin changes from low to high.	RW	0
0	ABNORMAL_ STRESS_FALL_EN	If this bit is set, it generates an interrupt event notification if the stress protection circuit is active.	RW	0

Table 14-84. OTHER_INT_EN_FALL_SET

Address Offset	0x8A
Description	This register does not physically exist. It is the same as the OTHER_INT_EN_FALL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
VB_SESS_VLD_FALL_EN	DM_HI_FALL_EN	DP_HI_FALL_EN	Reserved	Reserved	Reserved	MANU_FALL_EN	ABNORMAL_STRESS_FALL_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_ FALL_EN		RW	0
6	DM_HI_FALL_EN		RW	0
5	DP_HI_FALL_EN		RW	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	MANU_FALL_EN		RW	0
0	ABNORMAL_STRESS_FALL_EN		RW	0

Table 14-85. OTHER_INT_EN_FALL_CLR

Address Offset	0x8B
Description	This register does not physically exist. It is the same as the OTHER_INT_EN_FALL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
VB_SESS_VLD_FALL_EN	DM_HI_FALL_EN	DP_HI_FALL_EN	Reserved	Reserved	Reserved	MANU_FALL_EN	ABNORMAL_STRESS_FALL_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_FALL_EN		RW	0
6	DM_HI_FALL_EN		RW	0
5	DP_HI_FALL_EN		RW	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	MANU_FALL_EN		RW	0
0	ABNORMAL_STRESS_FALL_EN		RW	0

Table 14-86. OTHER_INT_STS

Address Offset	0x8C
Description	Indicates the current value of the interrupt source signal
Type	R

7	6	5	4	3	2	1	0
VB_SESS_VLD	DM_HI	DP_HI	Reserved	BDIS_ACON	Reserved	MANU	ABNORMAL_STRESS

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD	Same as VB_SESS_VLD pin	R	0
6	DM_HI	Same as DM_HI pin	R	0
5	DP_HI	Same as DP_HI pin	R	0
4	Reserved		R	0
3	BDIS_ACON	Asserted when the BDIS_ACON bit in the OTHER_ INTERRUPT_LATCH register is set	R	0
2	Reserved		R	0
1	MANU	Same as the MANU pin	R	0
0	ABNORMAL_STRESS	An abnormal condition activated the short withstand protection circuit. This may be the result of the attachment of a defective cable or a defective device.	R	0

Table 14-87. OTHER_INT_LATCH

Address Offset	0x8D
Description	These bits are set by the PHY when an unmasked specific event occurs. The PHY automatically clears all bits when the LINK reads this register, or when low-power mode is entered. **Note:** If register read data is returned to the LINK in the same cycle that an OTHER_ INTERRUPT_LATCH bit is to be set, the interrupt condition is given immediately in the register read data and the latch bit is not set.
Type	R

7	6	5	4	3	2	1	0
VB_SESS_VLD	Reserved(T)	Reserved(T)	Reserved	BDIS_ACON	Reserved	MANU_LATCH	ABNORMAL_STRESS_LATCH

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD	Set when VB_SESS_VLD changes level and the event is unmasked.	R	0
6	Reserved(T)		R	0

Bits	Field Name	Description	Type	Reset
5	Reserved(T)		R	0
4	Reserved		R	0
3	BDIS_ACON	Set when BDIS_ACON_EN is set, and transceiver asserts dp_pullup after detecting B-device disconnect	R	0
2	Reserved		R	0
1	MANU_LATCH	Asserted if the MANU_RISE bit in the OTHER_INTERRUPT_ ENABLE register is set, and the MANU input pin changes from low to high Also asserted if the MANU_FALL bit in the OTHER_ INTERRUPT_ENABLE register is set, and the MANU input pin changes from high to low	R	0
0	ABNORMAL_STRESS_LATCH	Asserted if the ABNORMAL_STRESS bit in the OTHER_INTERRUPT_ENABLE register is set, and a stress condition is detected (for example, shorts)	R	0

Table 14-88. ID_STATUS

Address Offset	0x96
Description	Indicates the resistor value connected on the ID pin These bits read as 0 while IDPULLUP = 0b in the OTG_CONTROL register. The link must wait at least 50 ms after setting IDPULLUP to 1b before reading this register.
Type	R

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	ID_RES_FLOAT	ID_RES_440K	ID_RES_200K	ID_RES_102K	ID_RES_GND

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	ID_RES_FLOAT	Set if the ID pin has no resistor to ground (open connection)	R	0
3	ID_RES_440K	Set if the resistor on ID pin is typically 440K. Indicates a type 2 carkit or type 2 charger	R	0
2	ID_RES_200K	Set if the resistor on ID pin is typically 200K. Indicates a type 1 carkit or a type 1 charger	R	0
1	ID_RES_102K	Set if the resistor on ID pin is typically 102K. Indicates an accessory that must be powered by phone	R	0
0	ID_RES_GND	Set if the ID pin is grounded	R	0

Table 14-89. CARKIT_SM_1_INT_EN

Address Offset	0x97
Description	If set, the bits in this register generate an interrupt event notification when the corresponding interrupt event is activated in the carkit state-machine.
Type	RW

7	6	5	4	3	2	1	0
Reserved	PSM_ERROR_EN	PH_ACC_EN	CHARGER_EN	USB_HOST_EN	USB_OTG_B_EN	CARKIT_EN	DISCONNECTED_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	PSM_ERROR_EN	If this bit is set, it generates an interrupt event notification when the device enters PH_ERROR state in the hardware state-machine.	RW	0
5	PH_ACC_EN	If this bit is set, it generates an interrupt event notification when the device enters PH_PACC state in the hardware state-machine.	RW	0
4	CHARGER_EN	If this bit is set, it generates an interrupt event notification when the device enters PH_CHARGER state in the hardware state-machine.	RW	0
3	USB_HOST_EN	If this bit is set, it generates an interrupt event notification when the device enters PH_USB_HOST state in the hardware state-machine.	RW	0
2	USB_OTG_B_EN	If this bit is set, it generates an interrupt event notification when the device enters PH_USB_OTG_B state in the hardware state-machine.	RW	0
1	CARKIT_EN	If this bit is set, it generates an interrupt event notification when the device enters PH_UART or PH_USB_READY state in the hardware state-machine.	RW	0
0	DISCONNECTED_EN	If this bit is set, it generates an interrupt event notification when the device enters PH_DISC state in the hardware state-machine.	RW	0

Table 14-90. CARKIT_SM_1_INT_EN_SET

Address Offset	0x98
Description	This register does not physically exist. It is the same as the CARKIT_SM_1_INT_EN register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	PSM_ERROR_EN	PH_ACC_EN	CHARGER_EN	USB_HOST_EN	USB_OTG_B_EN	CARKIT_EN	DISCONNECTED_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	PSM_ERROR_EN		RW	0
5	PH_ACC_EN		RW	0
4	CHARGER_EN		RW	0
3	USB_HOST_EN		RW	0
2	USB_OTG_B_EN		RW	0

Bits	Field Name	Description	Type	Reset
1	CARKIT_EN		RW	0
0	DISCONNECTED_EN		RW	0

Table 14-91. CARKIT_SM_1_INT_EN_CLR

Address Offset	0x99
Description	This register does not physically exist. It is the same as the CARKIT_SM_1_INT_EN register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	PSM_ERROR_EN	PH_ACC_EN	CHARGER_EN	USB_HOST_EN	USB_OTG_B_EN	CARKIT_EN	DISCONNECTED_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	PSM_ERROR_EN		RW	0
5	PH_ACC_EN		RW	0
4	CHARGER_EN		RW	0
3	USB_HOST_EN		RW	0
2	USB_OTG_B_EN		RW	0
1	CARKIT_EN		RW	0
0	DISCONNECTED_EN		RW	0

Table 14-92. CARKIT_SM_1_INT_STS

Address Offset	0x9A
Description	Indicates the current value of the interrupt source signal from the carkit hardware state-machine
Type	R

7	6	5	4	3	2	1	0
Reserved	PSM_ERROR	PH_ACC	CHARGER	USB_HOST	USB_OTG_B	CARKIT	DISCONNECTED

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	PSM_ERROR	Active high when psm_error interrupt source signal is valid	R	0
5	PH_ACC	Active high when ph_acc interrupt source signal is valid	R	0
4	CHARGER	Active high when charger interrupt source signal is valid	R	0

Bits	Field Name	Description	Type	Reset
3	USB_HOST	Active high when usb_host interrupt source signal is valid	R	0
2	USB_OTG_B	Active high when usb_otg_b interrupt source signal is valid	R	0
1	CARKIT	Active high when carkit interrupt source signal is valid	R	0
0	DISCONNECTED	Active high when disconnected interrupt source signal is valid	R	0

Table 14-93. CARKIT_SM_1_INT_LATCH

Address Offset	0x9B
Description	These bits are set when an unmasked carkit state-machine event occurs. All set bits are automatically cleared when the LINK reads this register, or when low-power mode is entered.
Type	R

7	6	5	4	3	2	1	0
Reserved	PSM_ERROR_LATCH	PH_ACC_LATCH	CHARGER_LATCH	USB_HOST_LATCH	USB_OTG_B_LATCH	CARKIT_LATCH	DISCONNECTED_LATCH

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	PSM_ERROR_LATCH	Set when PH_ERROR is entered in the hardware state-machine and the event is unmasked	R	0
5	PH_ACC_LATCH	Set when PH_PACC is entered in the hardware state-machine and the event is unmasked	R	0
4	USB_HOST_LATCH	Set when PH_CHARGER is entered in the hardware state-machine and the event is unmasked	R	0
3	USB_HOST_LATCH	Set when PH_USB_HOST is entered in the hardware state-machine and the event is unmasked	R	0
2	USB_OTG_B_LATCH	Set when PH_USB_OTG_B is entered in the hardware state-machine and the event is unmasked	R	0
1	CARKIT_LATCH	Set when PH_UART or PH_USB_READY is entered in the hardware state-machine and the event is unmasked	R	0
0	DISCONNECTED_LATCH	Set when PH_DISC is entered in the hardware state-machine and the event is unmasked	R	0

Table 14-94. CARKIT_SM_2_INT_EN

Address Offset	0x9C
Description	If set, the bits in this register generate an interrupt event notification when the corresponding interrupt event is activated in the carkit state-machine.
Type	RW

7	6	5	4	3	2	1	0
STOP_PLS_MISS_EN	Reserved	Reserved	Reserved	STEREO_TO_MONO_EN	Reserved	PHONE_UART_EN	PH_NO_ACK_EN

Bits	Field Name	Description	Type	Reset
7	STOP_PLS_MISS_EN	If this bit is set, it generates an interrupt event notification when the device is in DDA mode and the pulse is not received successfully.	RW	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	STEREO_TO_MONO_EN	If this bit is set, it generates an interrupt event notification when the PH_AUD_MOVE_INT_4W state is entered in the hardware state-machine.	RW	0
2	Reserved		R	0
1	PHONE_UART_EN	If this bit is set, it generates an interrupt event notification when the PH_PHONE_INT_4W or PH_PHONE_INT_5W state is entered in the hardware state-machine.	RW	0
0	PH_NO_ACK_EN	If this bit is set, it generates an interrupt event notification when the PH_NO_ACK_5W state is entered in the hardware state-machine.	RW	0

Table 14-95. CARKIT_SM_2_INT_EN_SET

Address Offset	0x9D
Description	This register does not physically exist. It is the same as the CARKIT_SM_2_INT_EN register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
STOP_PLS_MISS_EN	Reserved	Reserved	Reserved	STEREO_TO_MONO_EN	Reserved	PHONE_UART_EN	PH_NO_ACK_EN

Bits	Field Name	Description	Type	Reset
7	STOP_PLS_MISS_EN		RW	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	STEREO_TO_MONO_EN		RW	0
2	Reserved		R	0
1	PHONE_UART_EN		RW	0

Bits	Field Name	Description	Type	Reset
0	PH_NO_ACK_EN		RW	0

Table 14-96. CARKIT_SM_2_INT_EN_CLR

Address Offset	0x9E
Description	This register does not physically exist. It is the same as the CARKIT_SM_2_INT_EN register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
STOP_PLS_MISS_EN	Reserved	Reserved	Reserved	STEREO_TO_MONO_EN	Reserved	PHONE_UART_EN	PH_NO_ACK_EN

Bits	Field Name	Description	Type	Reset
7	STOP_PLS_MISS_EN		RW	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	STEREO_TO_MONO_EN		RW	0
2	Reserved		R	0
1	PHONE_UART_EN		RW	0
0	PH_NO_ACK_EN		RW	0

Table 14-97. CARKIT_SM_2_INT_STS

Address Offset	0x9F
Description	Indicates the current value of the interrupt source signal from the carkit hardware state-machine
Type	R

7	6	5	4	3	2	1	0
STOP_PLS_MISS	Reserved	Reserved	Reserved	STEREO_TO_MONO	Reserved	PHONE_UART	PH_NO_ACK

Bits	Field Name	Description	Type	Reset
7	STOP_PLS_MISS	Active high when stop_pls_miss interrupt source signal is valid	R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	STEREO_TO_MONO	Active high when stereo_to_mono interrupt source signal is valid	R	0
2	Reserved		R	0

Bits	Field Name	Description	Type	Reset
1	PHONE_UART	Active high when phone_uart interrupt source signal is valid	R	0
0	PH_NO_ACK	Active high when ph_no_ack interrupt source signal is valid	R	0

Table 14-98. CARKIT_SM_2_INT_LATCH

Address Offset	0xA0
Description	These bits are set when an unmasked carkit state-machine event occurs. All set bits are automatically cleared when the LINK reads this register, or when low-power mode is entered.
Type	R

7	6	5	4	3	2	1	0
STOP_PLS_MISS	Reserved	Reserved	Reserved	STEREO_TO_MONO	Reserved	PHONE_UART	PH_NO_ACK

Bits	Field Name	Description	Type	Reset
7	STOP_PLS_MISS	Set when DDA mode is entered and the pulse is not received successfully and the event is unmasked	R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	STEREO_TO_ MONO	Set when PH_AUD_MOVE_INT_4W is entered in the hardware state-machine and the event is unmasked	R	0
2	Reserved		R	0
1	PHONE_UART	Set when PH_PHONE_INT_4W or PH_PHONE_INT_5W is entered in the hardware state-machine and the event is unmasked	R	0
0	PH_NO_ACK	Set when PH_NO_ACK_5W is entered in the hardware state-machine and the event is unmasked	R	0

Table 14-99. CARKIT_SM_CTRL

Address Offset	0xA1
Description	Control signals required by the CEA carkit state-machine
Type	RW

7	6	5	4	3	2	1	0
Reserved(T)	Reserved(T)	DATA_DURING_AUDIO	DP_DISC_DET_EN	AUDIO_MODE	USB_CARKIT_MODE	CARKIT_PSM_RESET	CARKIT_PSM_EN

Bits	Field Name	Description	Type	Reset
7	Reserved(T)	Test bit: Must remain clear to 0 for normal operation	RW	0
6	Reserved(T)	Test bit: Must remain clear to 0 for normal operation	RW	0
5	DATA_DURING_AUDIO	Enables DDA mode	RW	0

Bits	Field Name	Description	Type	Reset
4	DP_DISC_DET_EN	Enables the DP_DISC_DET function; enabled by default	RW	1
3	AUDIO_MODE	The audio is mono (0) or stereo (1).	RW	0
2	USB_CARKIT_MODE	Enables the PSM to support USB signaling. This bit is set only if the connected CEA carkit device supports USB signaling. 0b: Carkit USB signaling disabled 1b: Carkit USB signaling enabled	RW	0
1	CARKIT_PSM_RESET	Resets the CEA carkit hardware state-machine	RW	0
0	CARKIT_PSM_EN	Enables the CEA carkit hardware state-machine	RW	0

Table 14-100. CARKIT_SM_CTRL_SET

Address Offset	0xA2
Description	This register does not physically exist. It is the same as the CARKIT_SM_CTRL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved(T)	Reserved(T)	DATA_DURING_AUDIO	DP_DISC_DET_EN	AUDIO_MODE	USB_CARKIT_MODE	CARKIT_PSM_RESET	CARKIT_PSM_EN

Bits	Field Name	Description	Type	Reset
7	Reserved(T)		RW	0
6	Reserved(T)		RW	0
5	DATA_DURING_AUDIO		RW	0
4	DP_DISC_DET_EN		RW	1
3	AUDIO_MODE		RW	0
2	USB_CARKIT_MODE		RW	0
1	CARKIT_PSM_RESET		RW	0
0	CARKIT_PSM_EN		RW	0

Table 14-101. CARKIT_SM_CTRL_CLR

Address Offset	0xA3
Description	This register does not physically exist. It is the same as the CARKIT_SM_CTRL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved(T)	Reserved(T)	DATA_DURING_AUDIO	DP_DISC_DET_EN	AUDIO_MODE	USB_CARKIT_MODE	CARKIT_PSM_RESET	CARKIT_PSM_EN

Bits	Field Name	Description	Type	Reset
7	Reserved(T)		RW	0
6	Reserved(T)		RW	0
5	DATA_DURING_AUDIO		RW	0
4	DP_DISC_DET_EN		RW	1
3	AUDIO_MODE		RW	0
2	USB_CARKIT_MODE		RW	0
1	CARKIT_PSM_RESET		RW	0
0	CARKIT_PSM_EN		RW	0

Table 14-102. CARKIT_SM_CMD

Address Offset	0xA4
Description	Carkit commands featured in the CEA carkit state-machine. The bits are auto-cleared when the command is executed. When set, a command remains pending until it reaches a valid state where it can be executed. If this state is never reached, the command remains pending without further effect until cleared by software.
Type	RW

7	6	5	4	3	2	1	0
CR_INT_DET	DISC_REQ	SW_UART_READY	CANCEL_PH_AUD_REQ	PH_AUD_REQ_ST2	PH_AUD_REQ	PH_AUD_MUTE	PH_UART_REQ

Bits	Field Name	Description	Type	Reset
7	CR_INT_DET	Carkit interrupt detect for when the state-machine is in DDA mode in 4-wire protocol	RW	0
6	DISC_REQ	Disconnect request for the state-machine to leave USB or UART mode in 4-wire or 5-wire	RW	0
5	SW_UART_READY	Software UART ready for when the state-machine is about to enter UART mode for 4-wire or 5-wire mode	RW	0
4	CANCEL_PH_AUD_REQ	Cancel phone audio request for when the state-machine is in 5-wire mode.	RW	0
3	PH_AUD_REQ_ST2	Phone audio request for when the state-machine is in 5-wire mode	RW	0
2	PH_AUD_REQ	Phone audio request for when the state-machine is in either 4-wire or 5-wire mode	RW	0
1	PH_AUD_MUTE	Phone audio mute for when the state-machine is in 5-wire mode	RW	0
0	PH_UART_REQ	Phone UART request for when the state-machine is in 4-wire mode	RW	0

Table 14-103. CARKIT_SM_CMD_SET

Address Offset	0xA5
Description	This register does not physically exist. It is the same as the CARKIT_SM_CMD register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
CR_INT_DET	DISC_REQ	SW_UART_READY	CANCEL_PH_AUD_REQ	PH_AUD_REQ_ST2	PH_AUD_REQ	PH_AUD_MUTE	PH_UART_REQ

Bits	Field Name	Description	Type	Reset
7	CR_INT_DET		RW	0
6	DISC_REQ		RW	0
5	SW_UART_READY		RW	0
4	CANCEL_PH_AUD_REQ		RW	0
3	PH_AUD_REQ_ST2		RW	0
2	PH_AUD_REQ		RW	0
1	PH_AUD_MUTE		RW	0
0	PH_UART_REQ		RW	0

Table 14-104. CARKIT_SM_CMD_CLR

Address Offset	0xA6
Description	This register does not physically exist. It is the same as the CARKIT_SM_CMD register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
CR_INT_DET	DISC_REQ	SW_UART_READY	CANCEL_PH_AUD_REQ	PH_AUD_REQ_ST2	PH_AUD_REQ	PH_AUD_MUTE	PH_UART_REQ

Bits	Field Name	Description	Type	Reset
7	CR_INT_DET		RW	0
6	DISC_REQ		RW	0
5	SW_UART_READY		RW	0
4	CANCEL_PH_AUD_REQ		RW	0
3	PH_AUD_REQ_ST2		RW	0
2	PH_AUD_REQ		RW	0

Bits	Field Name	Description	Type	Reset
1	PH_AUD_MUTE		RW	0
0	PH_UART_REQ		RW	0

Table 14-105. CARKIT_SM_CMD_STS

Address Offset	0xA7
Description	Status of the carkit commands issued to the state-machine. When any bit is set to 1, this triggers the autoclear function in the CARKIT_SM_CMD register.
Type	R

7	6	5	4	3	2	1	0
CR_INT_DET	DISC_REQ	SW_UART_READY	CANCEL_PH_AUD_REQ	PH_AUD_REQ_ST2	PH_AUD_REQ	PH_AUD_MUTE	PH_UART_REQ

Bits	Field Name	Description	Type	Reset
7	CR_INT_DET		R	0
6	DISC_REQ		R	0
5	SW_UART_READY	Set when the SW_UART_READY command is acknowledged by the state-machine	R	0
4	CANCEL_PH_AUD_REQ	Set when the CANCEL_PH_AUD_REQ command is acknowledged by the state-machine	R	0
3	PH_AUD_REQ_ST2	Set when the PH_AUD_REQ_ST2 command is acknowledged by the state-machine	R	0
2	PH_AUD_REQ	Set when the PH_AUD_REQ command is acknowledged by the state-machine	R	0
1	PH_AUD_MUTE	Set when the PH_AUD_MUTE command is acknowledged by the state-machine	R	0
0	PH_UART_REQ	Set when the PH_UART_REQ command is acknowledged by the state-machine	R	0

Table 14-106. CARKIT_SM_STATUS

Address Offset	0xAA
Description	Displays the last state that caused the CEA carkit state-machine to enter PH ERROR state
Type	R

7	6	5	4	3	2	1	0
Reserved	Reserved	CARKIT_SM_STATUS					

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5:0	CARKIT_SM_STATUS	Indicates which state caused the state-machine to enter PH_ERROR state	R	0x00

Table 14-107. CARKIT_SM_ERR_STATUS

Address Offset	0xA8
Description	Displays the current state in the CEA carkit state-machine
Type	R

7	6	5	4	3	2	1	0
Reserved	Reserved	CARKIT_SM_STATUS					

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5:0	CARKIT_SM_STATUS	Indicates the current status of the state-machine	R	0x00

Table 14-108. CARKIT_SM_CTRL_STATE

Address Offset	0xAB
Description	When CTRL_STATE_EN is set to 1, the CEA carkit state-machine jumps to the state defined in the CARKIT_SM_CTRL_STATE bits. This register is active only when the hardware CEA carkit state-machine is active.
Type	RW

7	6	5	4	3	2	1	0
CTRL_STATE_EN	Reserved	CARKIT_SM_CTRL_STATE					

Bits	Field Name	Description	Type	Reset
7	CTRL_STATE_EN	Activates the ability to force any state in the CEA carkit hardware state-machine, according to the bit value in CARKIT_SM_CTRL_STATE	RW	0
6	Reserved		R	0
5:0	CARKIT_SM_CTRL_STATE	These bits are active only when the CTRL_STATE_EN bit is set to 1. Selects which state to move to in the CEA carkit hardware state-machine.	RW	0x00

Table 14-109. POWER_CTRL

Address Offset	0xAC
Description	Controls OTG power section of the USB
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	OTG_EN	Reserved	Reserved (T)	Reserved (T)	Reserved (T)	Reserved (T)

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	OTG_EN	Enable complete OTG block (enable all OTG comparators and reference circuitry in VUSB3V1 supply domain).	RW	0

Bits	Field Name	Description	Type	Reset
4	Reserved		R	0
3	Reserved(T)	Test bit. Remains clear to 0 for normal operation.	RW	0
2	Reserved(T)	Test bit. Remains clear to 0 for normal operation.	RW	0
1	Reserved(T)	Test bit. Remains clear to 0 for normal operation.	RW	0
0	Reserved(T)	Test bit. Remains clear to 0 for normal operation.	RW	0

Table 14-110. POWER_CTRL_SET

Address Offset	0xAD
Description	This register does not physically exist. It is the same as the POWER_CTRL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	OTG_EN	Reserved	Reserved (T)	Reserved (T)	Reserved (T)	Reserved (T)

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	OTG_EN		RW	0
4	Reserved		R	0
3	Reserved(T)		RW	0
2	Reserved(T)		RW	0
1	Reserved(T)		RW	0
0	Reserved(T)		RW	0

Table 14-111. POWER_CTRL_CLR

Address Offset	0xAE
Description	This register does not physically exist. It is the same as the POWER_CTRL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	OTG_EN	Reserved	Reserved (T)	Reserved (T)	Reserved (T)	Reserved (T)

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	OTG_EN		RW	0
4	Reserved		R	0
3	Reserved(T)		RW	0
2	Reserved(T)		RW	0
1	Reserved(T)		RW	0
0	Reserved(T)		RW	0

Table 14-112. OTHER_IFC_CTRL2

Address Offset	0xAF
Description	This register controls an optional ULPI serial mode and reroutes the interrupts.
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	ULPI_STP_LOW	ULPI_TXEN_POL	ULPI_4PIN_2430	USB_INT_OUTSEL	

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	ULPI_STP_LOW	0b: ULPI state is controlled by OTHER_IFC_CTRL. 1b: Force the STP input line low when it is multiplexed with GPIO.	RW	0
3	ULPI_TXEN_POL	Controls the TXEN active level when the ULPI interface is set in ULPI serial mode 0b: TXEN is active high. 1b: TXEN is active low.	RW	0
2	ULPI_4PIN_2430	Changes the ULPI interface to a 4-pin serial mode based on OMAP2430C port map 0b: ULPI interface is defined by OTHER_IFC_ CONTROL and IFC_CTRL register. 1b: FS/LS packets are sent using 4-pin ULP.	RW	0
1:0	USB_INT_OUTSEL	Reroute interrupts. Valid only if ALT_INT_REROUTE bit of OTHER_IFC_CTRL is asserted. 00b: Reroute interrupt to the processor1 (INT1N line). 01b: Reroute interrupt to the processor2 (INT2N line). Others: Reserved	RW	0x0

Table 14-113. OTHER_IFC_CTRL2_SET

Address Offset	0xB0
Description	This register does not physically exist. It is the same as the OTHER_IFC_CTRL2 register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	ULPI_STP_LOW	ULPI_TXEN_POL	ULPI_4PIN_2430	USB_INT_OUTSEL	

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	ULPI_STP_LOW		RW	0

Bits	Field Name	Description	Type	Reset
3	ULPI_TXEN_POL		RW	0
2	ULPI_4PIN_2430		RW	0
1:0	USB_INT_OUTSEL		RW	0x0

Table 14-114. OTHER_IFC_CTRL2_CLR

Address Offset	0xB1
Description	This register does not physically exist. It is the same as the OTHER_IFC_CTRL2 register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	ULPI_STP_LOW	ULPI_TXEN_POL	ULPI_4PIN_2430	USB_INT_OUTSEL	

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	ULPI_STP_LOW		RW	0
3	ULPI_TXEN_POL		RW	0
2	ULPI_4PIN_2430		RW	0
1:0	USB_INT_OUTSEL		RW	0x0

Table 14-115. REG_CTRL_EN

Address Offset	0xB2
Description	Interrupt enable to detect conflict when ULPI and I^2C access occur at the same time
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ULPI_I2C_CONFLICT_INTEN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0

Bits	Field Name	Description	Type	Reset
2	Reserved		R	0
1	Reserved		R	0
0	ULPI_I2C_CONFLICT_INTEN	If this bit is enabled, any collisions between ULPI and I^2C register access are reported as interrupt events.	RW	0

Table 14-116. REG_CTRL_EN_SET

Address Offset	0xB3
Description	This register does not physically exist. It is the same as the REG_CTRL_EN register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ULPI_I2C_CONFLICT_INTEN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	Reserved		R	0
0	ULPI_I2C_CONFLICT_INTEN		RW	0

Table 14-117. REG_CTRL_EN_CLR

Address Offset	0xB4
Description	This register does not physically exist. It is the same as the REG_CTRL_EN register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ULPI_I2C_CONFLICT_INTEN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	Reserved		R	0
0	ULPI_I2C_CONFLICT_INTEN		RW	0

Table 14-118. REG_CTRL_ERROR

Address Offset	0xB5
Description	Interrupt latch that reports if a conflict occurs between ULPI and I^2C register access
Type	R

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ULPI_I2C_CONFLICT_ERROR

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	Reserved		R	0
0	ULPI_I2C_CONFLICT_ERROR	If this bit is set, it means a collision occurred between ULPI and I^2C access. To clear this interrupt latch, the software must make a read access.	R	0

Table 14-119. OTHER_FUNC_CTRL2

Address Offset	0xB8
Description	Provides additional control for carkit support
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VBAT_TIMER_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	Reserved		R	0
0	VBAT_TIMER_EN	Enable the VBAT function for MADC/BCI.	RW	0

Table 14-120. OTHER_FUNC_CTRL2_SET

Address Offset	0xB9
Description	This register does not physically exist. It is the same as the OTHER_FUNC_CTRL2 register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VBAT_TIMER_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	Reserved		R	0
0	VBAT_TIMER_EN		RW	0

Table 14-121. OTHER_FUNC_CTRL2_CLR

Address Offset	0xBA
Description	This register does not physically exist. It is the same as the OTHER_FUNC_CTRL2 register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VBAT_TIMER_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	Reserved		R	0
0	VBAT_TIMER_EN		RW	0

Table 14-122. CARKIT_ANA_CTRL

Address Offset	0xBB
Description	Offers control of several functions of the USB carkit; enables comparator, activates switch, and allows some signal monitoring
Type	RW

7	6	5	4	3	2	1	0
USBMEAS_SEL	CR_INT_EN	VOICESWTCEN	VOICESWRREN	SEL_MADC_MCPC	USB_MADC_VDD_SEL	USB_MADC_DM_SEL	Reserved(T)

Bits	Field Name	Description	Type	Reset
7	USBMEAS_SEL	0: USBMEAS/ADCIN15 tied to ground 1: USBMEAS/ADCIN15 connected to DP, DM, or resistor divider under VUSB3V1 according to CARKIT_ANA_CTRL	RW	0
6	CR_INT_EN	Lets the comparator detect a DDA pulse on DP. This DDA pulse is generated by the external carkit. 0: Disable comparator. 1: Enable comparator.	RW	0
5	VOICESWTCEN	0: VOICESWTC switch is opened (default). This is done in MCPC analog signaling modes when TXAF and CTSI are to be capacitively coupled by the external capacitor. 1: VOICESWTC is closed. TXAF and CTSI pins are shorted in UART signaling modes, to reduce load on the CTSI pin.	RW	0

Bits	Field Name	Description	Type	Reset
4	VOICESWRREN	0: VOICESWRR switch is opened (default). This is done in MCPC analog signaling modes when RXAF and RTSO are to be capacitively coupled by external capacitor. 1: VOICESWRR is closed. RXAF and RTSO pins are shorted in UART signaling modes, to reduce load on the RTSO pin.	RW	0
3	SEL_MADC_MCPC	Routes all four MCPC pins to the MADC for monitoring: RXAF to ADCIN6 RTSO to ADCIN5 TXAF to ADCIN4 CTSI to ADCIN3 When the bit is cleared to 0, the ADCIN3 to ADCIN6 inputs are tied low.	RW	0
2	USB_MADC_VDD_SEL	Routes resistor divider under VUSB3V1 voltage to the MADC USBMEAS input for monitoring. The USBMEAS_SEL bit must also be set to 1. 0: Disabled (disconnected to MADC) 1: Enabled (connected to MADC)	RW	0
1	USB_MADC_DM_SEL	Routes DM voltage to the MADC USBMEAS input for monitoring common mode voltage during audio mode **Note:** Audio speaker_L amp must be in mute mode to measure stable Vcmo. The USBMEAS_SEL bit must also be set to 1. 0: Disabled (disconnected to MADC) 1: Enabled (connected to MADC)	RW	0
0	Reserved(T)	Test bit: Must remain clear to 0 for normal operation	RW	0

Table 14-123. CARKIT_ANA_CTRL_SET

Address Offset	0xBC
Description	This register does not physically exist. It is the same as the CARKIT_ANA_CTRL register with read/set-only property (write 1 to set a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
USBMEAS_SEL	CR_INT_EN	VOICESWTCEN	VOICESWRREN	SEL_MADC_MCPC	USB_MADC_VDD_SEL	USB_MADC_DM_SEL	Reserved(T)

Bits	Field Name	Description	Type	Reset
7	USBMEAS_SEL		RW	0
6	CR_INT_EN		RW	0
5	VOICESWTCEN		RW	0
4	VOICESWRREN		RW	0
3	SEL_MADC_MCPC		RW	0
2	USB_MADC_VDD_SEL		RW	0
1	USB_MADC_DM_SEL		RW	0
0	Reserved(T)		RW	0

Table 14-124. CARKIT_ANA_CTRL_CLR

Address Offset	0xBD
Description	This register does not physically exist. It is the same as the CARKIT_ANA_CTRL register with read/clear-only property (write 1 to clear a bit; writing 0 has no effect).
Type	RW

7	6	5	4	3	2	1	0
USBMEAS_SEL	CR_INT_EN	VOICESWTCEN	VOICESWRREN	SEL_MADC_MCPC	USB_MADC_VDD_SEL	USB_MADC_DM_SEL	Reserved(T)

Bits	Field Name	Description	Type	Reset
7	USBMEAS_SEL		RW	0
6	CR_INT_EN		RW	0
5	VOICESWTCEN		RW	0
4	VOICESWRREN		RW	0
3	SEL_MADC_MCPC		RW	0
2	USB_MADC_VDD_SEL		RW	0
1	USB_MADC_DM_SEL		RW	0
0	Reserved(T)		RW	0

Table 14-125. VBUS_DEBOUNCE

Address Offset	0xC0
Description	This register controls when the VBUS pin status is captured after an edge transition of the VBUS signal. The time is measured in units of (32/32768 seconds). The default value corresponds to 30 ms. A value of 0 bypasses the VBUS debounce counter.
Type	RW

7	6	5	4	3	2	1	0
VBUS_DEBOUNCE							

Bits	Field Name	Description	Type	Reset
7:0	VBUS_DEBOUNCE	Programmable counter value for debounce for VBUS	RW	0x1F

Table 14-126. ID_DEBOUNCE

Address Offset	0xC1
Description	This register controls when the ID pin status is captured after setting IDPULLUP = 1. The time is measured in units of (32/32768 seconds). The default value corresponds to 50 ms. A value of 0 bypasses the ID debounce counter.
Type	RW

7	6	5	4	3	2	1	0
ID_DEBOUNCE							

Bits	Field Name	Description	Type	Reset
7:0	ID_DEBOUNCE	Programmable counter value for debounce for ID	RW	0x34

Table 14-127. TPH_DP_CON_MIN

Address Offset	0xC2
Description	CEA carkit counter value tph_dp_con_min. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TPH_DP_CON_MIN						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TPH_DP_CON_MIN	Programmable counter value for CEA carkit timer tph_dp_con_min	RW	0x64

Table 14-128. TPH_DP_CON_MAX

Address Offset	0xC3
Description	CEA carkit counter value tph_dp_con_max. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TPH_DP_CON_MAX						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TPH_DP_CON_MAX	Programmable counter value for CEA carkit timer tph_dp_con_max	RW	0x7F

Table 14-129. TCR_DP_CON_MIN

Address Offset	0xC4
Description	CEA carkit counter value tcr_dp_con_min. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TCR_DP_CON_MIN						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TCR_DP_CON_MIN	Programmable counter value for CEA carkit timer tcr_dp_con_min	RW	0x6C

Table 14-130. TCR_DP_CON_MAX

Address Offset	0xC5
Description	CEA carkit counter value tcr_dp_con_max. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TCR_DP_CON_MAX						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TCR_DP_CON_MAX	Programmable counter value for CEA carkit timer tcr_dp_con_max	RW	0x75

Table 14-131. TPH_DP_PD_SHORT

Address Offset	0xC6
Description	CEA carkit counter value tph_dp_pd_short. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TPH_DP_PD_SHORT						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TPH_DP_PD_SHORT	Programmable counter value for CEA carkit timer tph_dp_pd_short	RW	0x64

Table 14-132. TPH_CMD_DLY

Address Offset	0xC7
Description	CEA carkit counter value tph_cmd_dly. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TPH_CMD_DLY						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TPH_CMD_DLY	Programmable counter value for CEA carkit timer tph_cmd_dly	RW	0x20

Table 14-133. TPH_DET_RST

Address Offset	0xC8
Description	CEA carkit counter value tph_det_rst. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TPH_DET_RST						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TPH_DET_RST	Programmable counter value for CEA carkit timer tph_det_rst	RW	0x01

Table 14-134. TPH_AUD_BIAS

Address Offset	0xC9
Description	CEA carkit counter value tph_aud_bias. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TPH_AUD_BIAS						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TPH_AUD_BIAS	Programmable counter value for CEA carkit timer tph_aud_bias	RW	0x17

Table 14-135. TCR_UART_DET_MIN

Address Offset	0xCA		
Physical address	0x0000 00CA	**Instance**	USB_SCUSB
Description	CEA-carkit counter value tcr_uart_det_min. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	TCR_UART_DET_MIN						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TCR_UART_DET_MIN	Programmable counter value for CEA carkit timer tcr_uart_det_min	RW	0x01

Table 14-136. TCR_UART_DET_MAX

Address Offset	0xCB
Description	CEA carkit counter value tcr_uart_det_max. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TCR_UART_DET_MAX						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TCR_UART_DET_MAX	Programmable counter value for CEA carkit timer tcr_uart_det_max	RW	0x02

Table 14-137. TPH_ID_INT_PW

Address Offset	0xCD
Description	CEA carkit counter value tph_id_int_pw. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TPH_ID_INT_PW						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TPH_ID_INT_PW	Programmable counter value for CEA carkit timer tph_id_int_pw	RW	0x36

Table 14-138. TACC_ID_INT_WAIT

Address Offset	0xCE
Description	CEA carkit counter value tacc_id_int_wait. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TACC_ID_INT_WAIT						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TACC_ID_INT_WAIT	Programmable counter value for CEA carkit timer tacc_id_int_wait	RW	0x44

Table 14-139. TACC_ID_INT_PW

Address Offset	0xCF
Description	CEA carkit counter value tacc_id_int_pw. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TACC_ID_INT_PW						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TACC_ID_INT_PW	Programmable counter value for CEA carkit timer tacc_id_int_pw	RW	0x07

Table 14-140. TPH_CMD_WAIT

Address Offset	0xD0
Description	CEA carkit counter value tph_cmd_wait. The contents can be changed only when carkit_ psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TPH_CMD_WAIT						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TPH_CMD_WAIT	Programmable counter value for CEA carkit timer tph_cmd_wait	RW	0x3B

Table 14-141. TPH_ACK_WAIT

Address Offset	0xD1
Description	CEA carkit counter value tph_ack_wait. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TPH_ACK_WAIT						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TPH_ACK_WAIT	Programmable counter value for CEA carkit timer tph_ack_wait	RW	0x17

Table 14-142. TPH_DP_DISC_DET

Address Offset	0xD2
Description	CEA carkit counter value tph_dp_disc_det. The contents can be changed only when carkit_psm_en = 0 or carkit_psm_reset = 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved	TPH_DP_DISC_DET						

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6:0	TPH_DP_DISC_DET	Programmable counter value for CEA carkit timer tph_dp_disc_det	RW	0x6B

Table 14-143. VBAT_TIMER

Address Offset	0xD3
Description	Counter value for VBAT function. It can be accessed only through I^2C. This register can be modified only when vbat_timer_en_rg = 0.
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	VBAT_TIMER_VALUE			

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3:0	VBAT_TIMER_VALUE	Programmable counter value for vbat_timer for BCI	RW	0x6

Table 14-144. CARKIT_4W_DEBUG

Address Offset	0xE0
Description	Image of the software phone state-machine while in 4-wire CEA carkit mode This register is not in use when the hardware state-machine is in use.
Type	R

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	PH_AUDIO_4W	PH_UART_4W	PH_INIT_4W	PH_USB_4W	PH_DISC_4W

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	PH_AUDIO_4W	Set if the software state-machine is in ph_audio_4w	R	0
3	PH_UART_4W	Set if the software state-machine is in ph_uart_4w	R	0
2	PH_INIT_4W	Set if the software state-machine is in ph_init_4w	R	0
1	PH_USB_4W	Set if the software state-machine is in ph_usb_4w	R	0
0	PH_DISC_4W	Set if the software state-machine is in ph_disc_4w	R	0

Table 14-145. CARKIT_5W_DEBUG

Address Offset	0xE1
Description	Image of the software phone state-machine while in 5-wire CEA carkit mode This register is not in use when the hardware state-machine is in use.
Type	R

7	6	5	4	3	2	1	0
PH_WFA_5W	PH_INT_5W	PH_MUTE_P_5W	PH_ACK_5W	PH_MUTE_A_5W	PH_AUDIO_5W	PH_BIAS_5W	PH_UART_5W

Bits	Field Name	Description	Type	Reset
7	PH_WFA_5W	Set if the software state-machine is in ph_wfa_5w	R	0
6	PH_INT_5W	Set if the software state-machine is in ph_int_5w	R	0
5	PH_MUTE_P_5W	Set if the software state-machine is in ph_mute_p_5w	R	0
4	PH_ACK_5W	Set if the software state-machine is in ph_ack_5w	R	0
3	PH_MUTE_A_5W	Set if the software state-machine is in ph_mute_a_5w	R	0
2	PH_AUDIO_5W	Set if the software state-machine is in ph_audio_5w	R	0
1	PH_BIAS_5W	Set if the software state-machine is in ph_bias_5w	R	0
0	PH_UART_5W	Set if the software state-machine is in ph_uart_5w	R	0

Table 14-146. PHY_PWR_CTRL

Address Offset	0xFD
Description	Controls the PHY state. It can be accessed only through I^2C.
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PHYPWD

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	Reserved		R	0
0	PHYPWD	Powers down entire PHY and stops MCLK 0b: Normal state 1b: Power down	RW	0

Table 14-147. PHY_CLK_CTRL

Address Offset	0xFE
Description	Controls the DPLL clock state. It can be accessed only through I^2C.
Type	RW

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	CLOCKGATING_EN	CLK32K_EN	REQ_PHY_DPLL_CLK

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	CLOCKGATING_EN	Enable automatic clock gating of the ULPI register clock. 0b: Gating is disabled. 1b: Gating is enabled.	RW	0
1	CLK32K_EN	32-kHz clock enable 0b: 32-kHz clock is disabled. 1b: 32-kHz clock is enabled.	RW	1
0	REQ_PHY_DPLL_CLK	Active high DPLL clock request 0b: PHY state depends on the SUSPENDM bit in the FUNC_CTRL register. 1b: Powers the PHY and wakes up the clock	RW	0

Table 14-148. PHY_CLK_CTRL_STS

Address Offset	0xFF
Description	Indicates the current state of the PHY DPLL. It can be accessed only through I^2C.
Type	R

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PHY_DPLL_CLK

Bits	Field Name	Description	Type	Reset
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1	Reserved		R	0

Bits	Field Name	Description	Type	Reset
0	PHY_DPLL_CLK	Asserted when the PHY DPLL is locked	R	0

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