TPS65950 Layout Guide

User's Guide

Literature Number: SWCU055A
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TPS65950 Layout Guide

This document describes constraints and special guidelines for designing with the TPS65950 device. The TPS65950 is a high-end analog companion baseband that contains several blocks with different layout constraints. This guide describes these constraints and shows examples of good layout practice. The design model is a proven design.

The guide is organized as a design process:

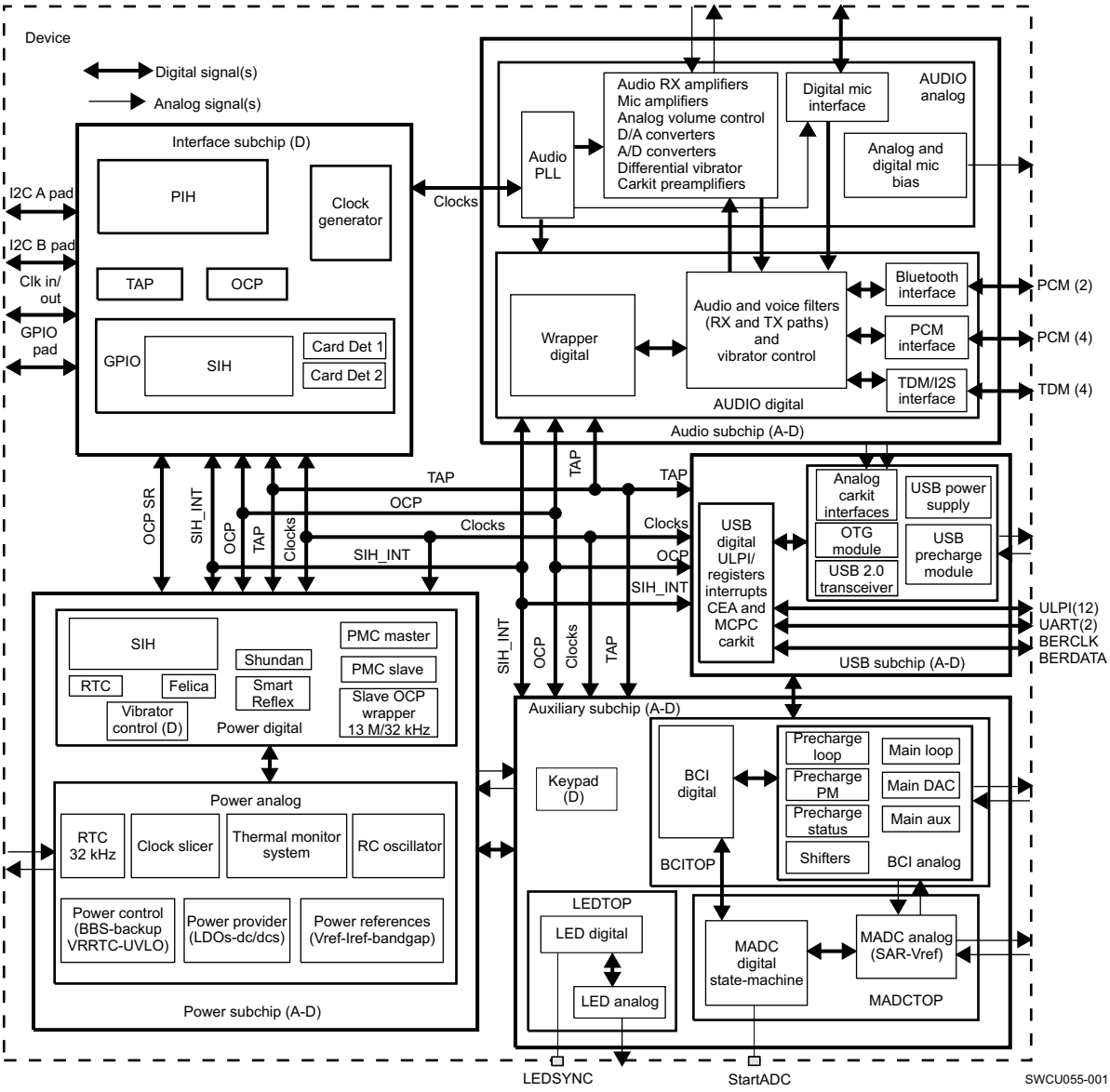
- Definition of the printed circuit board (PCB).
- Division of signals into groups; description of group requirements and constraints
- Placement of external components
- Use of tunnels for shielding
- Design example: PCB design

1 TPS65950 Component Description

The TPS65950 is an integrated power-management/audio coder/decoder (codec) device for use in portable cellular telephone designs that derive their power from batteries based on Li-ion, Li-ion polymer, or manganese-cobalt chemistries. The TPS65950 typically receives its commands from an applications processor or a modem and provides power conversion/regulation duties, a complete audio codec section, and a class-D audio amplifier. In addition to generic support capabilities, the TPS65950 meets the specific power requirements of the Texas Instruments OMAP™ family, especially OMAP3430 and OMAP2430 devices.

Figure 1 is a block diagram of the TPS65950.

Figure 1. TPS65950 Block Diagram



2 PCB Design

Before layout, PCB analysis is needed to determine a good strategy of what to place on which layer. Many theories must be considered to determine a good design; however, some theories conflict with others, so a perfect strategy is not always possible. Because the design of the PCB includes compromises, strategy is critical to achieving the best possible design.

2.1 Routing Strategy

Routing on different layers is an advantage for the CAD designer, but constraints must still be met. Because some signals are sensitive to influence from other signals, they must be spaced a specific distance from other signals, even if the signals are on different layers. Routing a sensitive signal on a different layer from a noisy signal does not solve all problems. The PCB does not shield for capacitive or inductive coupling between signals.

When determining the PCB design, multiple factors must be considered: number of layers, number of micro via layers, buried via, and stacked via layers. These factors are related to cost; each decision affects the cost, and vice versa. Cost determines design choices.

2.1.1 60/60 Track Strategy

Figure 2 shows the TPS65950 ball placement. The balls are placed in 3 and 4 rows or columns. This sets the requirement for the PCB design to have three levels of stackable vias or to have tracks between the balls.

Figure 2. TPS65950 Ball Placement

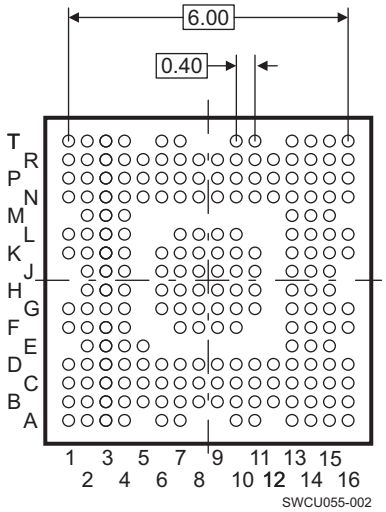


Figure 3 shows tracks between the balls, which is the recommended solution using a 60/60 spacing strategy.

Figure 3. Recommended Solution for 60/60 Spacing

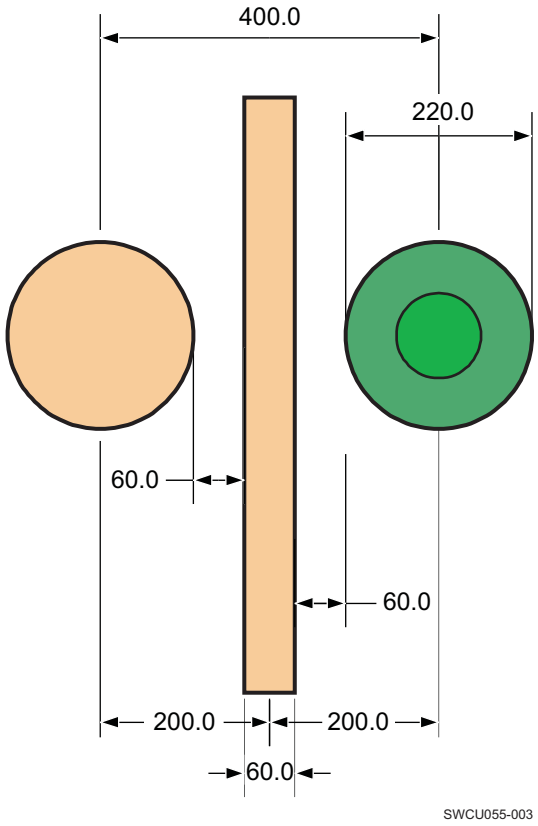
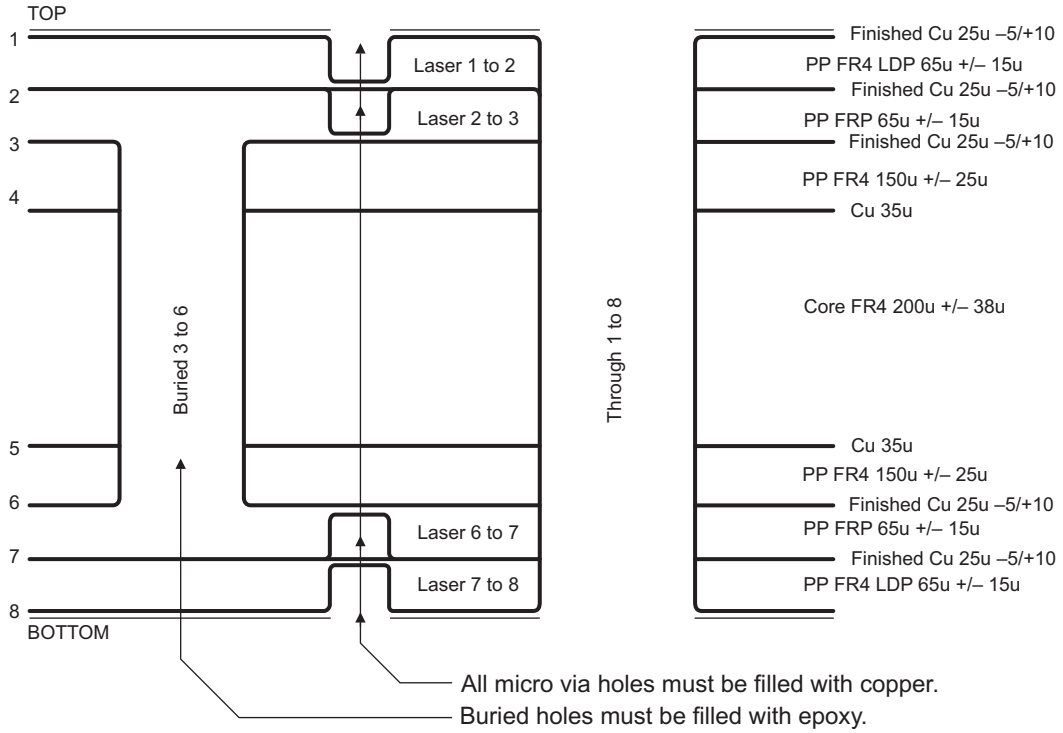
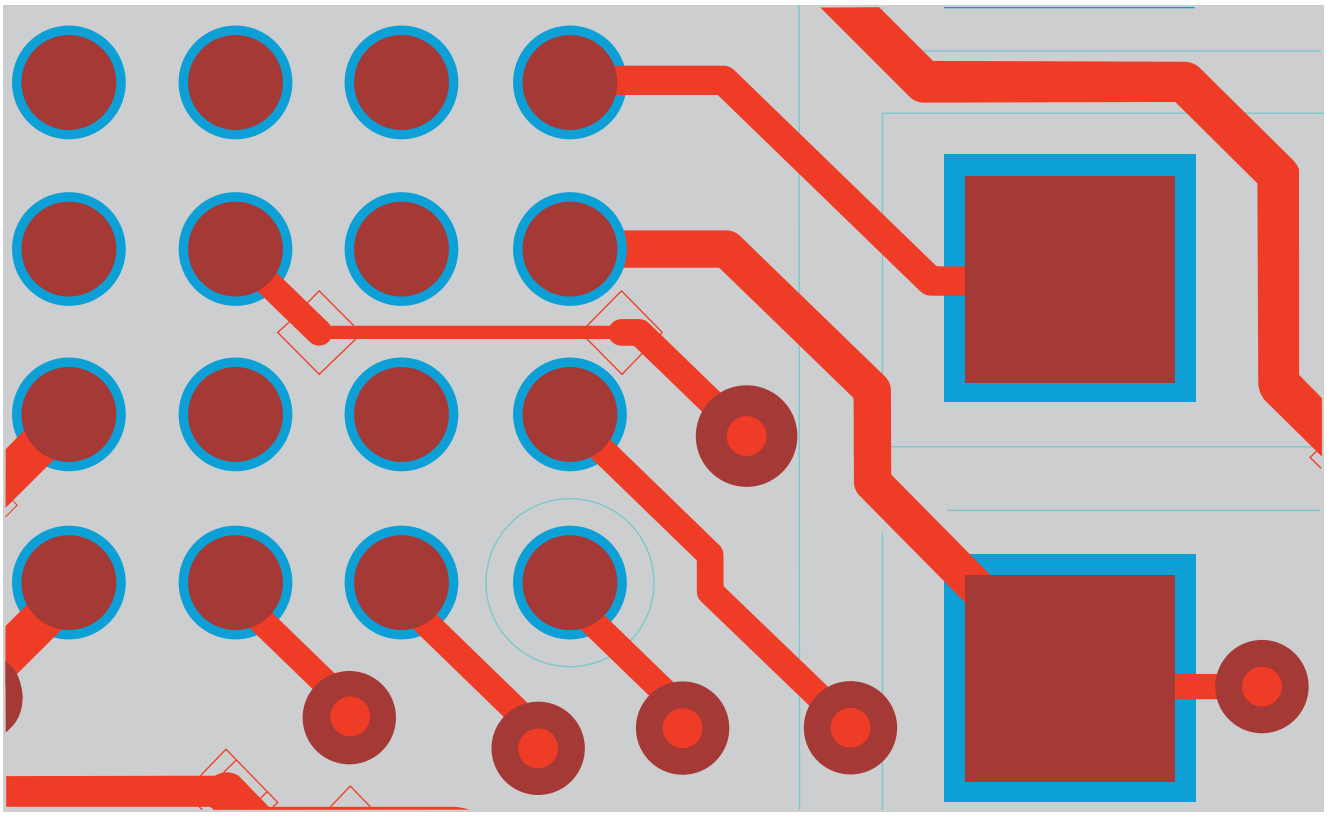


Figure 4 shows a design using 60/60 spacing with two micro via layers.

Figure 4. 60/60 Spacing With Two Micro Via Layers





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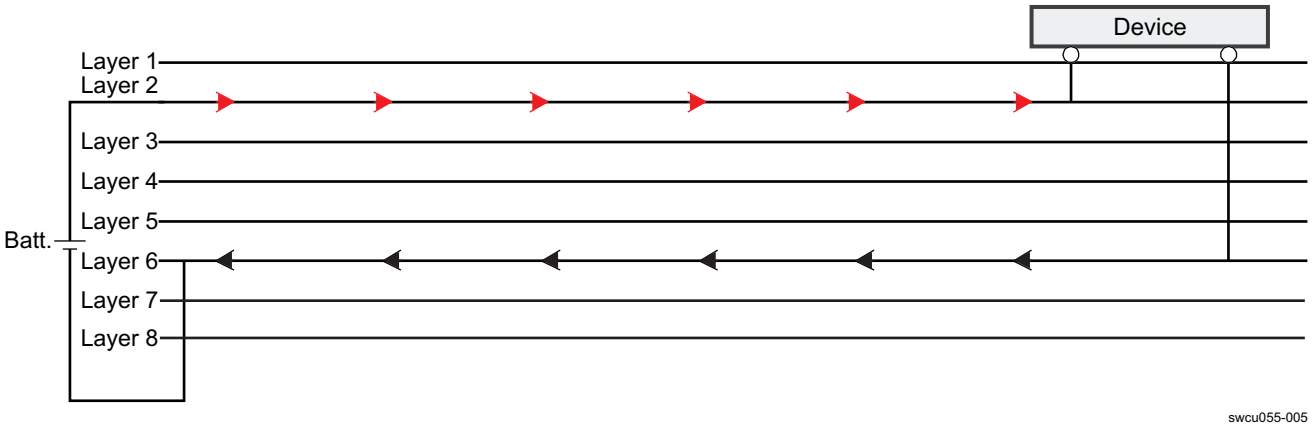
2.2 Layer Definition

Before layout, the engineer and the PCB designer must consider which signals to place where; a preliminary study of the routing is valuable in this case. One example is when the ground loop for high-power consumption devices surrounds other signals that cannot withstand the interference from these signals. Figure 5 shows an example of this situation.

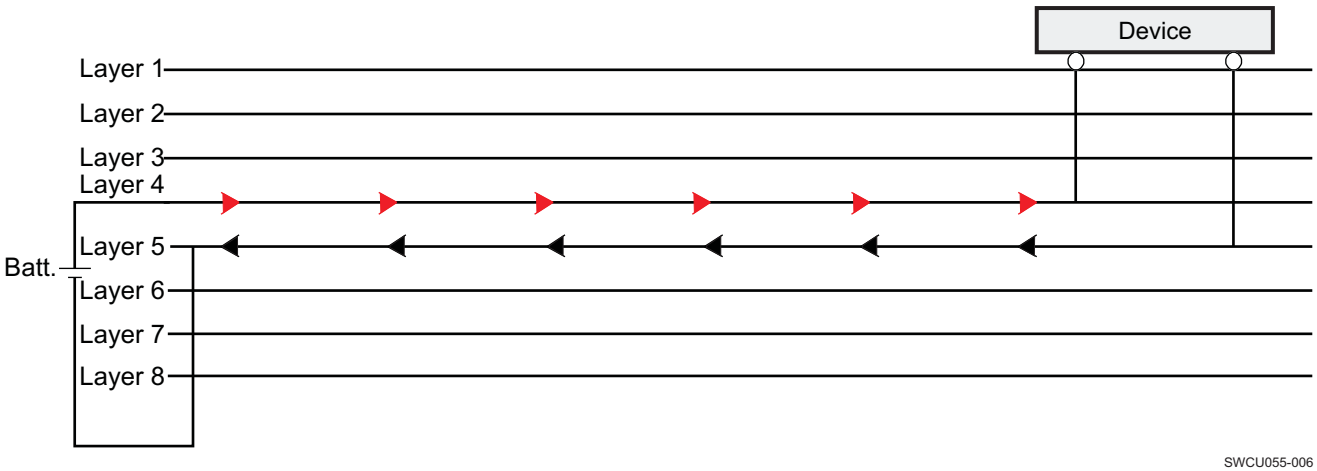
Figure 5. Incorrect Design: Signals Inside the Ground Loop



In Figure 5, signals are inside the ground loop, in layers 3, 4, and 5. This is not recommended, because the signals inside the ground loop are affected by the flux generated by the current in the loop. This must be avoided, especially for sensitive signals such as microphones and oscillators.

The supply line and the ground path are equally crucial to the layout. Supply must be placed and calculated so that its flux does not affect any signals that cannot withstand it, and the ground plane must be solid, especially close to the supply trace. If this is not the case, the risk for noise interference is great. Figure 6 shows a design that solves the problem.

Figure 6. Correct Design: Signals Outside the Ground Loop



In Figure 6, separate layers are used for supply and ground, and there is no signal layer inside the ground loop.

In addition, because capacitive coupling across layers (caused by flux generated in the supply path or the ground path) affects neighboring layers, no sensitive signals can be parallel to the supply line and the corresponding ground path.

3 Signal Grouping

3.1 High Power

3.1.1 Ground for Power

Table 1. Ground for Power

Group	BGA Pin Number	Pin Name	Function
GND signal	C12	GND.RIGHT	Power
	C11	GND.RIGHT	Power
	C10	GND.LEFT	Power
	C9	GND.LEFT	Power
GND digital	H9	DGND	Power
	H10	DGND	Power
	H11	DGND	Power
	H13	DGND	Power

3.1.2 Sensitive Ground

Table 2. Sensitive Ground

Group	BGA Pin Number	Pin Name	Function
GND signal	D3	MICBIAS.GND	Power
	N15	AGND	Power
GND power	C7	AVSS4	Power
	M15	AVSS3	Power
	R10	AVSS2	Power
	E5	AVSS1	Passive
	J4	AVSS1	Power
	J6	AVSS1	Power
	J7	AVSS1	Power
	J8	AVSS1	Power
	R2	VIO.GND	Power
	T3	VIO.GND	Power
	B15	VDD1.GND	Power
	C15	VDD1.GND	Power
	C16	VDD1.GND	Power
	T14	VDD2.GND	Power
	R15	VDD2.GND	Power

3.1.3 Power Input Lines

Table 3. Power Input Lines

Group	BGA Pin Number	Pin Name	Function
Power	K15	VINT	Power
Input	H15	VPLLA3R	Power
	L1	VAUX12S	Power
	K1	VDAC.IN	Power
	R9	VBAT.USB	Power
	B2	VAUX4.IN	Power

Table 3. Power Input Lines (continued)

Group	BGA Pin Number	Pin Name	Function
	C1	VMMC1.IN	Power
	A3	VMMC2.IN	Power
	D9	VBAT.LEFT	Power
	D10	VBAT.LEFT	Power
	D11	VBAT.RIGHT	Power
	D12	VBAT.RIGHT	Power
	D14	VDD1.IN	Power
	E14	VDD1.IN	Power
	E15	VDD1.IN	Power
	R13	VDD2.IN	Power
	P14	VDD2.IN	Power
	P3	VIO.IN	Power
	R4	VIO.IN	Power

3.1.4 Power Output Lines

Table 4. Power Output Lines

Group	BGA Pin Number	Pin Name	Function
Power	M2	VAUX1.OUT	Power
Output	M3	VAUX2.OUT	Power
	G16	VAUX3.OUT	Power
	B3	VAUX4.OUT	Power
	C2	VMMC1.OUT	Power
	A4	VMMC2.OUT	Power
	K2	VSIM	Power
	L2	VDAC.OUT	Power
	H14	VPLL1	Power
	J15	VPLL2	Power
	E13	VDD1.OUT	Power
	C14	VDD1.L	Passive
	D15	VDD1.L	Passive
	D16	VDD1.L	Passive
	N13	VDD2.OUT	Power
	T13	VDD2.L	Power
	R14	VDD2.L	Power
	N3	VIO.OUT	Passive
	R3	VIO.L	Passive
	T4	VIO.L	Passive

3.1.5 Decoupling for Internal Functions

Table 5. Decoupling for Internal Functions

Group	BGA Pin Number	Pin Name	Function
Internal power decoupling	H3	VINTANA1.OUT	Power
	J2	VINTANA2.OUT	Power
	B6	VINTANA2.OUT	Power

Table 5. Decoupling for Internal Functions (continued)

Group	BGA Pin Number	Pin Name	Function
	K16	VRTC	Power
	L16	VINTDIG	Power

3.1.6 Power for USB Connection

Table 6. Power for USB Connection

Group	BGA Pin Number	Pin Name	Function
	P9	VUSB.3P1	Power
	P8	VINTUSB1P5	Power
	P10	VINTUSB1P8	Power

3.1.7 Sensitive Signals

Table 7. Sensitive Signals

Group	BGA Pin Number	Pin Name	Function
ADC	H4	ADCIN0	Bidirectional
	J3	ADCIN1	Bidirectional
	G3	ADCIN2	Input
	J9	START.ADC	Input
slow clk	N10	32KCLKOUT	Output
	P16	32KXIN	Input
	P15	32KXOUT	Output
Audio	D1	MICBIAS1/VMIC1	Output
	E2	MIC.MAIN.P	Input
	F2	MIC.MAIN.M	Input
	D2	MICBIAS2/VMIC2	Output
	G2	MIC.SUB.P/DIG.MIC.0	Input
	H2	MIC.SUB.M/DIG.MIC1	Input
	E4	VHSMIC	Output
	E3	HSMIC.P	Input
	F3	HSMIC.M	Input
	F1	AUXL	Input
	G1	AUXR	Input

3.1.8 Signals That can Introduce Noise

Table 8. Signals That can Introduce Noise

Group	BGA Pin Number	Pin Name	Function
Charger interface	N5	VAC	Power
	N7	ICTLAC1	Output
	P2	ICTLAC2	Output
	P6	ICTLUSB1	Output
	P1	ICTLUSB2	Output
	N2	VPRECH	Output
	N4	PCHGAC	Input
	N6	PCHGUSB	Input

Table 8. Signals That can Introduce Noise (continued)

Group	BGA Pin Number	Pin Name	Function
	P5	VCCS	Input
	P4	VBATS	Input
	R5	VBAT	Input
	N1	BCIAUTO	Input

3.1.9 Class-D Amplifier Switching Input

Table 9. Class D Amplifier Switching Input

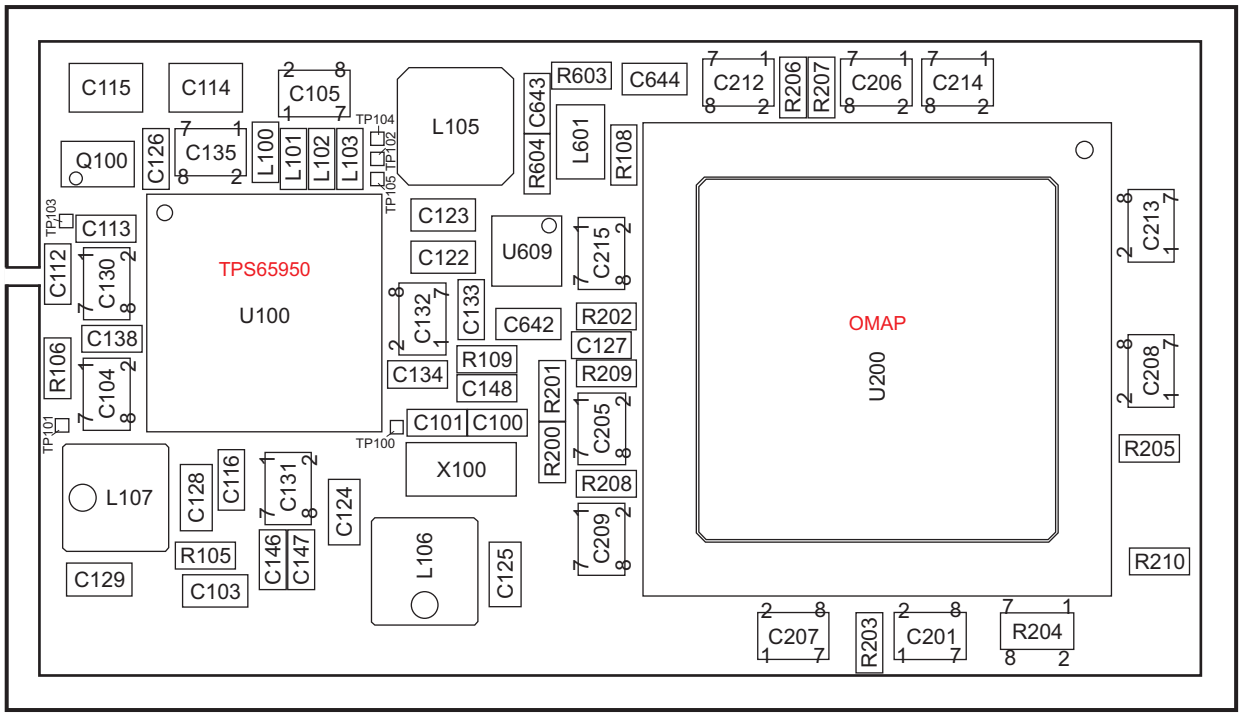
Group	BGA Pin Number	Pin Name	Function
Class D	B9	IHF.LEFT.P	Output
	B10	IHF.LEFT.M	Output
	B11	IHF.RIGHT.P	Output
	B12	IHF.RIGHT.M	Output

4 Placement of External Components

Placement of external components requires engineering skill. Placement is affected by the mechanical dimension, and therefore by the placement of the TPS65950. Placement of the TPS65950 relative to other components must conform to specific requirements. This is especially critical for routing power lines from the TPS65950 to the devices requiring the supply. When performing design calculations, consider that the tolerances on DC/DC converter outputs are ±4 percent.

Figure 7 shows board layout. In the following sections, all references to board design are to Figure 7.

Figure 7. Board Layout



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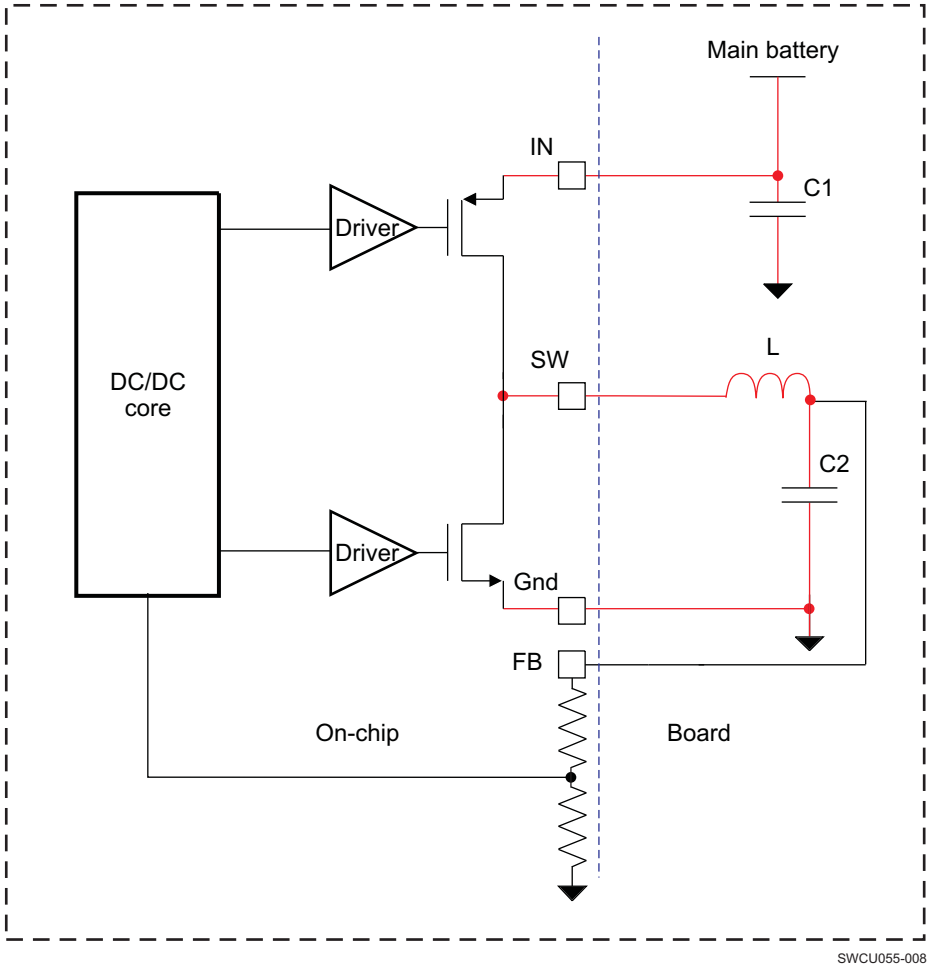
4.1 DC/DC Converter Outputs

Board layout is an important step in the design of all switching power supplies. High-speed (HS) operation of the TPS65950 demands careful attention to PCB layout. Care must be taken in designing board layout to achieve the specified performance. If the layout is not carefully done, the regulator can show poor line and/or load regulation, stability issues, and EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, wide and short traces must be used for the main current paths, as indicated in bold red lines in Figure 8.

Figure 8. DC/DC Converter



Follow these general steps:

1. Place the input capacitor as close as possible to the integrated circuit (IC) pins as well as the inductor and output capacitor.
2. Separate the grounds between the control and the power devices to minimize the effects of ground noise.
3. Connect these ground nodes (star point) under the IC and ensure that small signal components returning to the AGND pin do not share the high current path of C1 and C2.

VDD1 components:

- Coil: L105
- Capacitors: C123, C122 (C122 decoupling battery input)

VDD2 components:

- Coil: L106
- Capacitors: C125, C124 (C124 decoupling battery input)

VIO components:

- Coil: L107
- Capacitors: C129, C128 (C128 decoupling battery input)

The connection between the capacitor (C1) and the IN ball must be less than 5 mΩ and the connection between the inductor (L) and the SW ball should be less than 8 mΩ.

CAUTION

Failure to meet these parameters can have a severe impact on the performance and reliability of the device.

4.1.1 Sense Signal for DC/DC Converter

The output voltage sense line (VFDBACK) must be connected directly to the output capacitor and routed away from noisy components and traces (for example, the SWITCH line). Its trace must be minimized and placed so that no signals can affect the voltage level, because the voltage level is used to adjust the output voltage from the DC/DC converter.

4.1.2 Placement of USB Charge Pump Components

Place charge-pump fly and tank capacitors as close as possible to related balls. Target 10 mΩ or less trace resistance:

1. From CP.OUT to CVBUS positive terminal
2. From CP.CAPP to CCP.FC positive terminal
3. From CP.CAPN to CCP.FC negative terminal

If these recommendations cannot be achieved, consider the risk of degrading the functionality of the USB charge pump and take relevant actions to compensate.

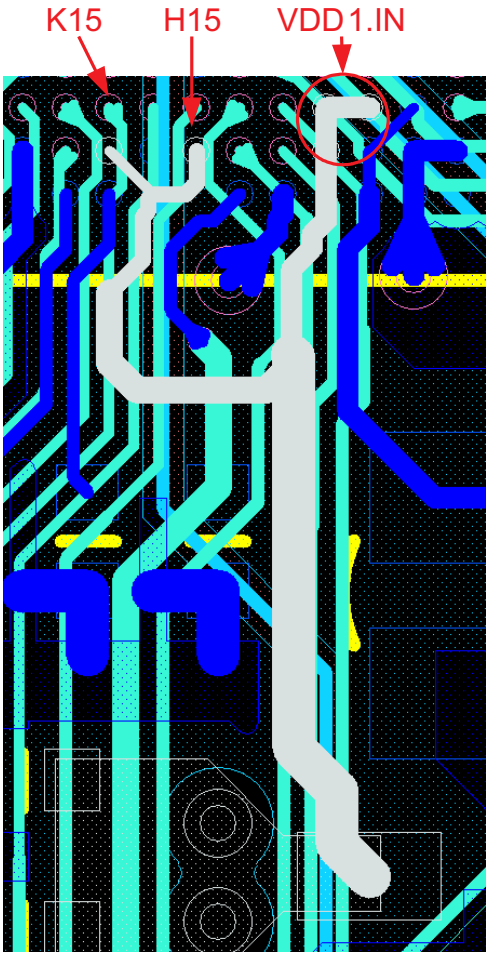
4.1.3 Incorrect DC/DC Converter Layout

The following subsections describe incorrect design examples that required a redesign of the PCB, and suggest solutions.

4.1.3.1 Supply for DC/DC Converters

In the design example in Figure 9, the designer connected VBAT for VDD1 input with a connection that is too small, but the major problem is that the design connects balls H15 and K15 to the same line. K15 and H15 supply sensitive circuits in the TPS65950, and these circuits are affected by the current drawn by VDD1. The in-rush current for VDD1 causes a ripple in the supply line. This ripple must be minimized before it is propagated to other circuits; this can be done by using the small impedances in the PCB and the decoupling capacitors.

Figure 9. Incorrect Supply for DC/DC Converters



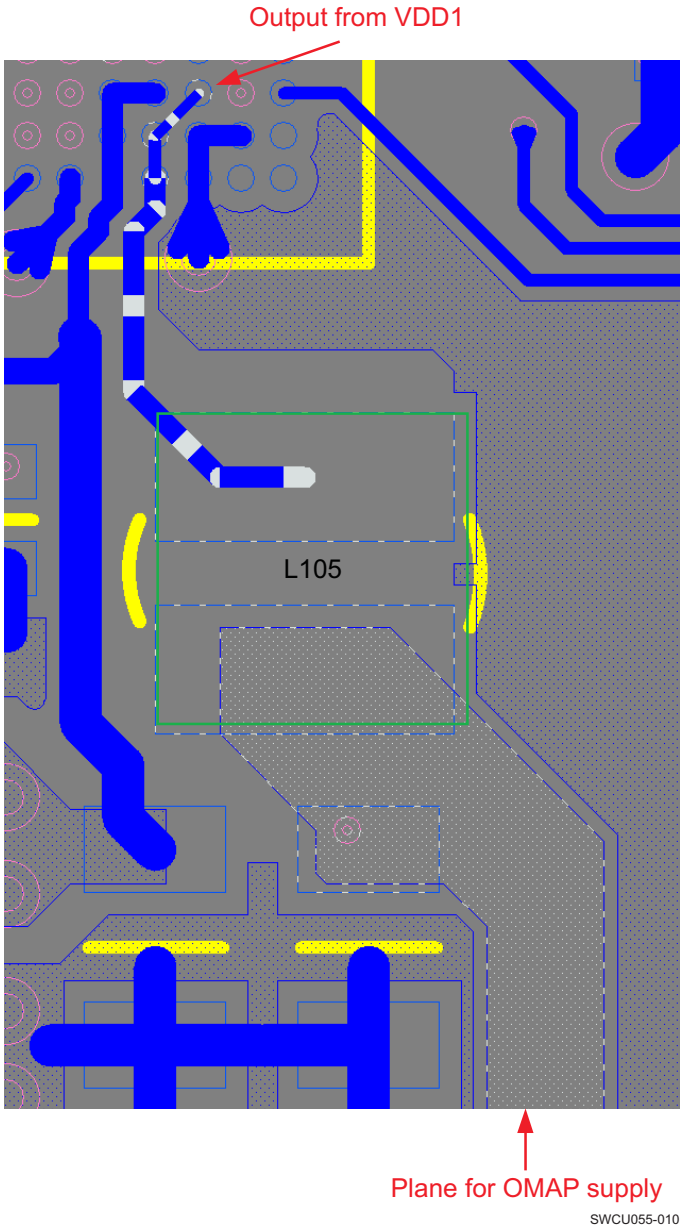
Solution:

Make a connection directly from the tank capacitor to supply K15 and H15, also called star topology.

4.1.3.2 Output From DC/DC Converters

In Figure 10, the outputs of TPS65950 are connected to three balls (D15, D16, and C14) to support the high current in the connection. Here a board is made with a thin connection from VDD1.OUT to the coil. This connection is made only on the top layer. After the coil, a plane is defined, and that is acceptable. However, it is unusual that the design uses a plane from the coil to the consumer but not from the DC/DC converter to the coil. This will become a bottleneck. Because the impedance in the connection affects the efficiency of the DC/DC converter, the impedance in the connection from VDD1.OUT causes poor efficiency in VDD1.

Figure 10. Output From DC/DC Converter



Solution:

Improve the connection from the output balls and make parallel tracks in a minimum of three planes: layers 2 and 3 when possible. This can be achieved by using vias on the output balls.

4.2 USB Signal Routing

To minimize signal problems with quality and EMI, use the following general routing and placement guidelines for laying out the USB section:

- With minimum trace lengths, route HS clock and HS USB differential pairs first. Maintain maximum possible distance between HS clocks/periodic signals to HS USB differential pairs and any connector leaving the PCB (such as I/O connectors, control and signal headers, or power connectors). Consider routing the signals in a tunnel.
- The D+ and D– circuit board traces that run between a transceiver and its associated connector should also have a nominal differential impedance of 90 Ω, and together they may add an additional 4 ns of delay between the transceivers. (In the USB specification, see Section 7.1.6 for details about impedance specifications for boards and transceivers.)
- Route HS USB signals using minimum vias and corners to reduce signal reflections and impedance changes. When it becomes necessary to turn 90 degrees, use two 45-degree turns or an arc instead of making a single 90-degree turn. This reduces reflections on the signal by minimizing impedance discontinuities.
- Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with HS traces as much as practical. It is preferable to change layers to avoid crossing a plane split.
- Place all needed components before starting the routing. ESD components must be close to the connector; TPD3E001 from TI are convenient because of their small size.
- The signal pair must be routed in parallel with equal trace length. Avoid differences between signals. If this is not possible, keep signals as close to equal as possible.
- The impedance from wire to wire should be from 80 to 100 Ω; the impedance from track to ground should be 50 Ω. For more information, see the USB specification.
- If the requirements from USB connections conflict with other signals, give the highest priority to the USB signals.

Signals Between TPS65950 and OMAP

Signals for USB between OMAP and TPS65950 (ULPI) also need attention, because the speed is approximately 60 to 70 MHz. Because signals are digital, they can introduce noise to other signals if the capacitive coupling is not considered:

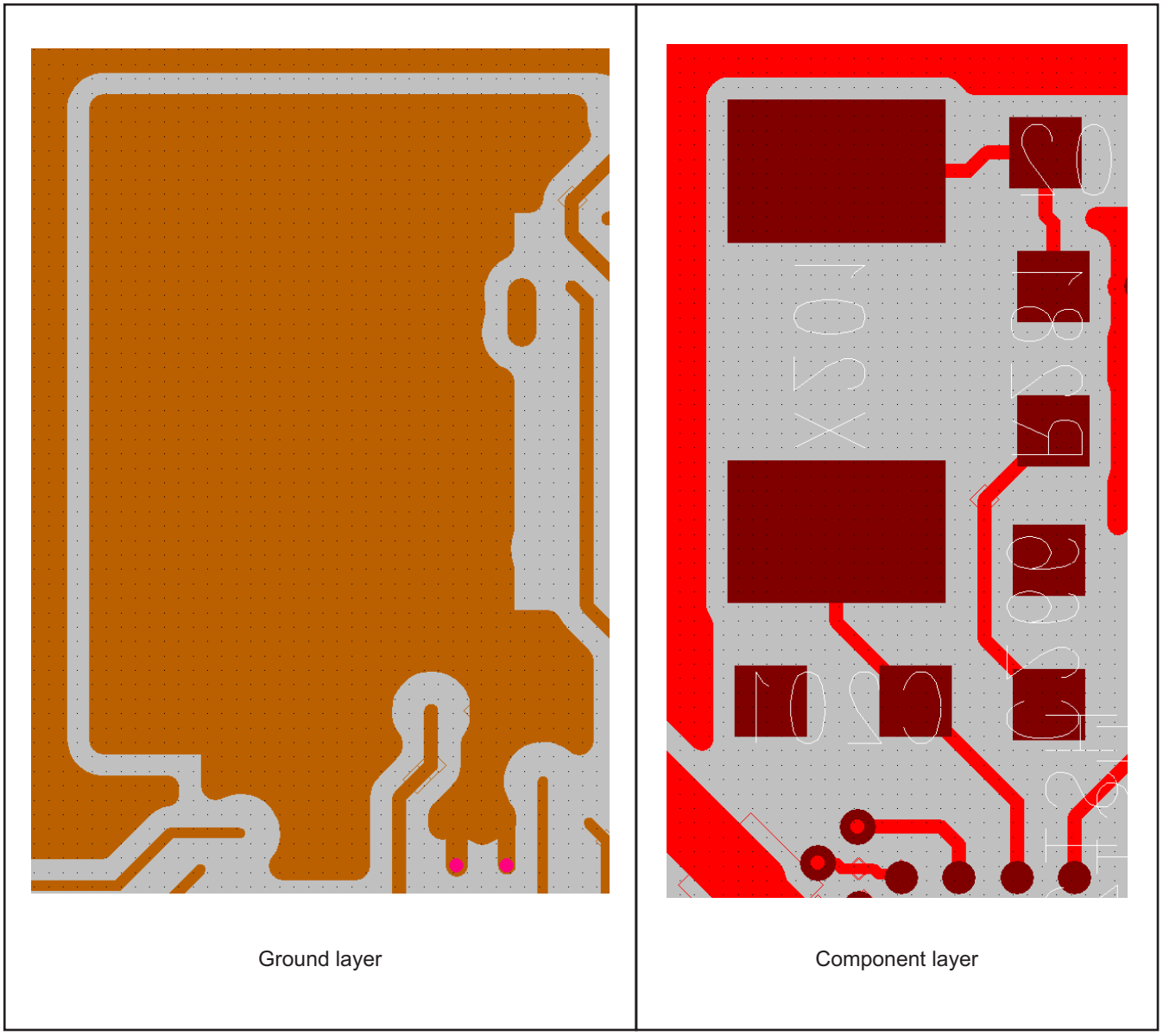
- Length should be as equal as possible.
- Length cannot exceed 50 mm.
- Trace impedance from track to ground should be 80 to 100 Ω.
- Route signals in parallel.

4.3 32-kHz Oscillator Circuit

The 32-kHz clock circuit is sensitive, and special considerations must be taken to prevent any influence on the circuit.

To protect the circuit from disturbance in the ground plane, a special restricted area can be defined. In the layer directly under the components, place a plane that refers only to the AGND ball N15 on TPS65950 (see Figure 11).

Figure 11. 32-kHz Oscillator Circuit



4.3.1 Use of 32-kHz Output

If the 32-kHz signal must be distributed to more than one device, use star topology to avoid timing differences. Output is on ball N10. Tunneling should also be used to prevent noise on this clock line from other signals.

4.4 Audio Considerations

This document describes only a few requirements and recommendations for audio circuits. For detailed information about requirements and recommendations for audio circuits, see the TPS65950 *Data Manual*.

4.4.1 Class-D Amplifier Output

The class-D amplifier requires special attention when the board layout is planned, to secure good performance and to minimize EMI emission. The class-D amplifier output is a switching element and requires a filter on the output to reduce noise emission.

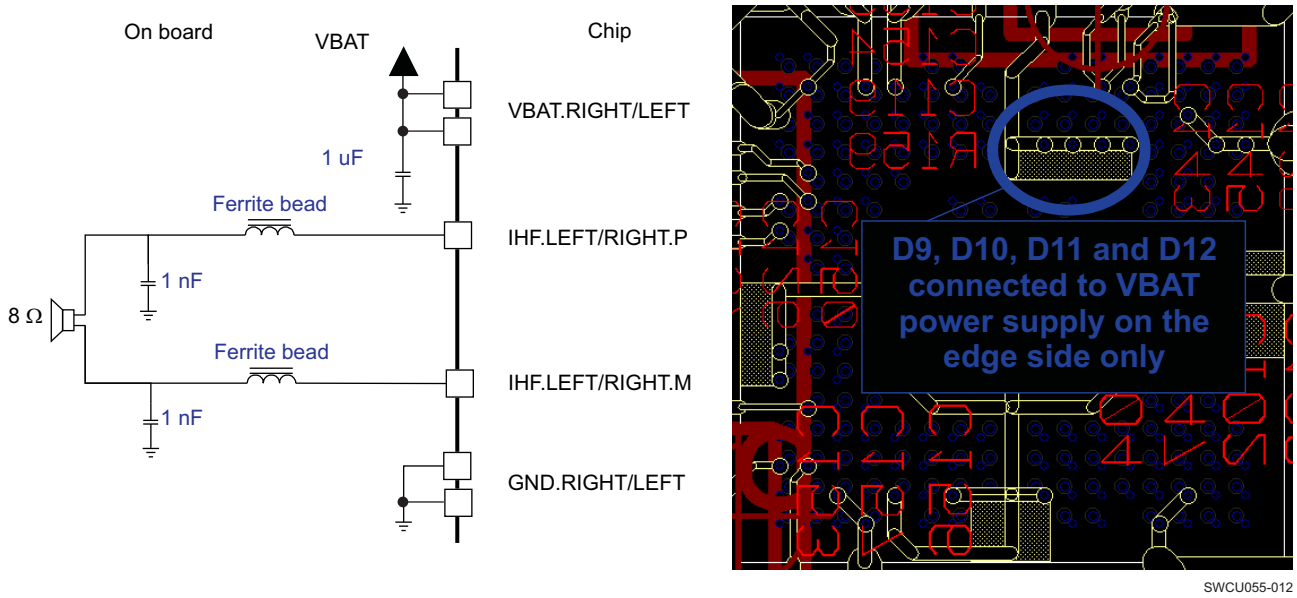
The supply for the class-D amplifier must be taken as directly as possible from the battery. It is best if the supply is made as a connection where the amplifier is the only consumer (that is, a direct connection from battery to amplifier supply). This circuit is given special attention because the input current on the class-D amplifier is high. This causes noise on the supply line and that can affect other circuits.

The following parameters require special attention:

- Low impedance on VBAT connection
- Low inductance; no or limited layer shift

Figure 12 shows a class-D amplifier output.

Figure 12. Class-D Amplifier Output



Output Filter

The output filter must be as close to the TPS65950 as possible. Connections on where the signal are transported must be as wide as possible; the combination of a high frequency and an 8-Ω load produces large currents. Use an LC output filter if there are low-frequency EMI-sensitive circuits and/or there are long leads from the amplifier to the speaker. It is critical to provide a low inductance, impedance ground path for the class-D power. The amplifier ground must be separated from other ground to minimize the effects of ground noise.

The ferrite bead filter and capacitor must be as close as possible to the IC pins. The amplifier grounds must be separated from other ground to minimize the effects of ground noise.

Routing of the signals is important relative to other sensitive signals. The class-D amplifier output signals are strongly driven and can create problems. Take special care with the sensitive audio signals connected to balls in the same area on the TPS65950.

Example of ferrite beads: N2012ZPS121, Murata BLM15AG102SN1, and MDP BKP1608HS271.

4.5 LED/Vibrator Output

To minimize the risk of EMI emission from open-drain output, place external components as close as possible. To minimize the degradation of the function, make the connecting PCB traces as wide as possible, reducing impedances.

4.6 BCI Routing Constraints

4.6.1 BCI Layout Consideration

Board layout should use the following recommendations for routing external components and traces concerned with battery charging circuit on TPS65950. Special attention should be given to placement of R_{sense}. R_{sense} should be placed close to the device as mentioned below. If not placed close to the device then the actual charging current would be lower (due to excessive IR drop in the path) than what the device shows in the internal device registers.

Table 10. BCI Layout Consideration

PAD	Guildelines
VAC	High current (defined by the user but could be max 1.7 A in theory) from VAC into the charge path.
VBUS	High current (defined by the user but could be max 1.7 A in theory) from VBUS into the charge path.
VCCS	R_{sense} (sense resistor), must be placed close to VCCS pin. Routing matched with VBATS. Maximum trace resistance is 3 Ω.
VBATS	R_{sense} (sense resistor), must be placed close to the VCCS pin. Maximum trace resistance should be 3 Ω. Routing matched with VCCS. This pin will have max 6 mA in pre-charge.
VBAT	Connection close to the battery. Maximum trace resistance is 3 Ω.
VPRECH	Place 1uF capacitor close to VPRECH pin. Maximum trace resistance is 200 mΩ
BCIAUTO	$R_{BCIAUTO}$, BCIAUTO external resistor must be placed close to BCIAUTO pin.
ADCIN1	Max resistance on the pad: 10 Ω
ADCIN2	Max resistance on the pad: 10 Ω

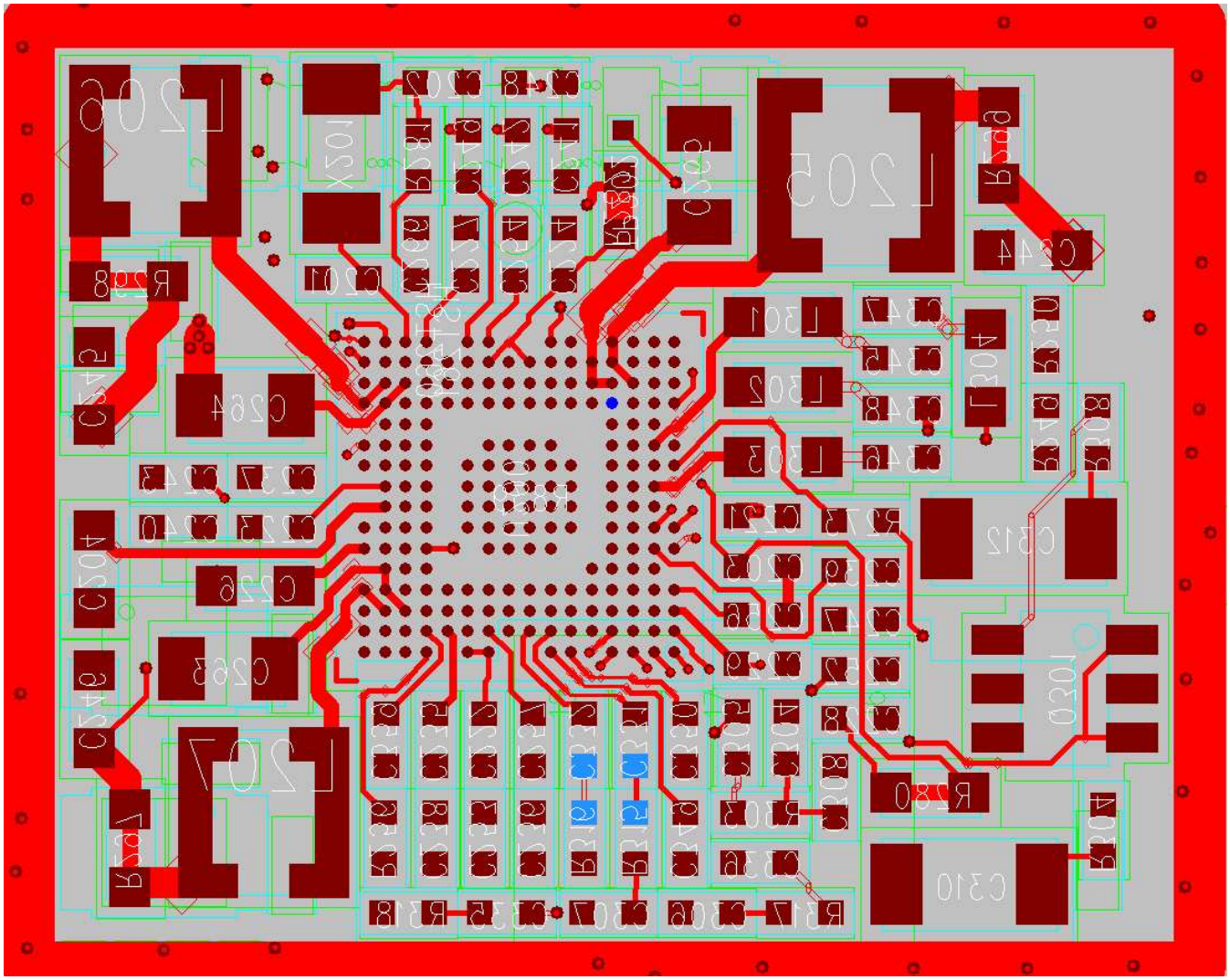
5 Sample Layouts

This section describes some examples of PCB design.

5.1 Bottom Layer

Figure 13 shows a bottom-layer design.

Figure 13. Bottom-Layer Design



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In this design, the DC/DC outputs are close to TPS65950.

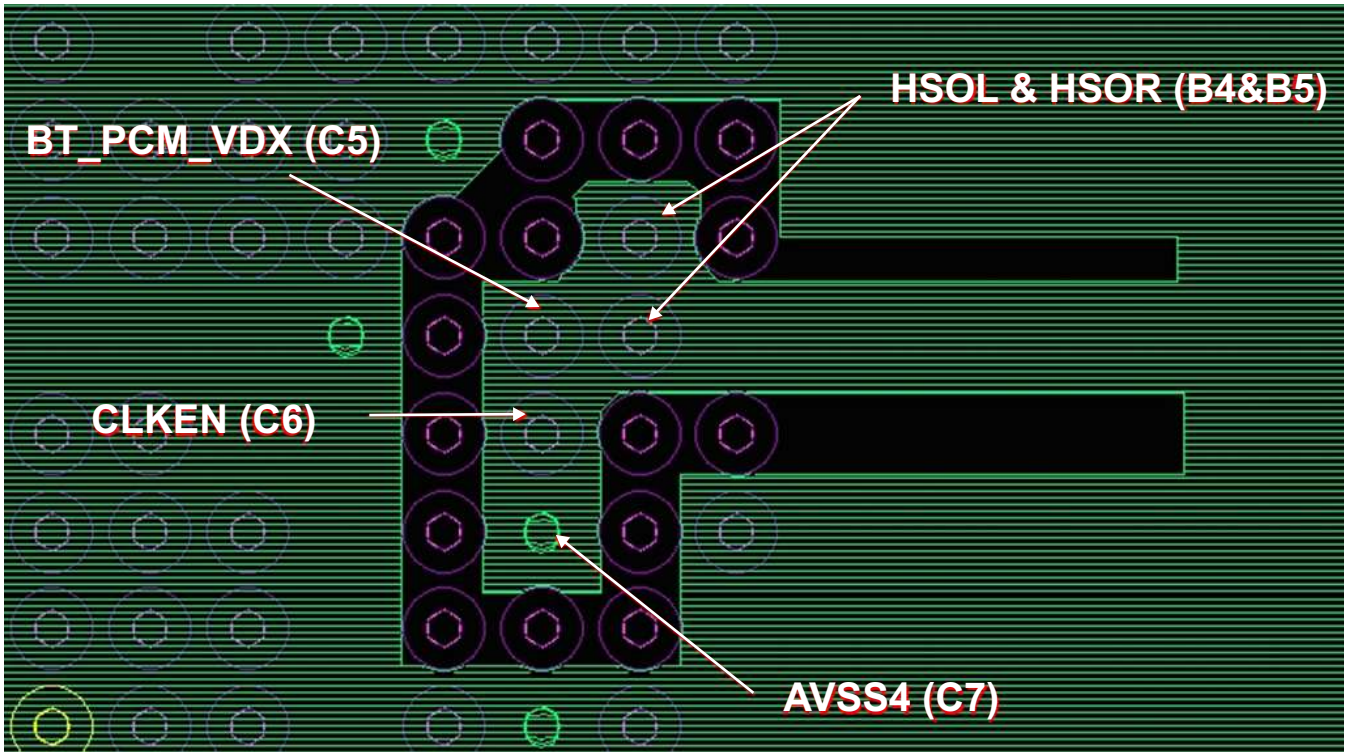
L205, L206, and L207 are all coils for the DC/DC regulators. The feedback connection for each coil is placed on an inner layer with sufficient distance from noisy signals.

For the USB DC/DC supply, capacitor C226 is close to the TPS65950 to minimize the track resistance and avoid efficiency degradation.

5.2 Ground Reference for Headset Output Amplifier

Figure 14 shows a ground reference for a headset output amplifier.

Figure 14. Ground Reference for Headset Output Amplifier



Make a split in the ground plane. The return path from ball C7 must have a direct reference to the output of the headset amplifiers.

The impedance from ball C7 to the real ground cannot exceed 50 mΩ.

6 Routing of Parallel Balls

Routing of parallel balls can be divided into three scenarios:

- High-power supply outputs
- High-power supply inputs
- Multiple power inputs

6.1 Signals That May Not be Directly Connected to High-Power Nets

The VBATS, VPLL3R.IN, are sensitive to noise and require a separate connection to the battery from the other supply balls.

VBATS measures battery voltage and can be affected by noise on the supply, thus causing incorrect measurements.

VPLL3R.IN is the supply for the internal phase-locked loop (PLL) and is sensitive to noise on the supply line. This must be considered during layout. A small filter can be useful here.

6.2 High-Power Outputs

When routing high-power supply outputs, ensure low impedance in the tracks to ensure low IR drop. Furthermore, it is crucial that the routing of the parallel balls ensures that power is distributed evenly between the balls. This can be done by connecting the parallel balls to a power plane. The current distribution, and hence the power distribution, can be controlled by consciously connecting to the plane with a well-planned distribution of via connections.

6.3 High-Power Inputs

High-power supply inputs must be routed with low impedance tracks to meet requirements for IR drop. Decoupling capacitors are recommended one per supply connection; these must be as close as possible to the inputs. To ensure good decoupling, power must first pass the footprint of the decoupling capacitor and then continue to the power input. Even the smallest stub from the power track to the capacitor significantly degrades the effect of the capacitor. To ensure best possible performance from the capacitor, ground the capacitor with a solid connection to the same ground as the high-power device.

6.4 Multiple Power Inputs

With multiple power inputs, the same power source is distributed to a number of devices or multiple power connections on a single device. In this case, select a point of distribution from which to branch out the power supply to various devices or to various locations on the same device.

6.4.1 Point of Distribution

A point of distribution can be the decoupling capacitor of the device that generates the power or a similar point in the PCB where there is good decoupling of the power and low impedance tracks from the power supply. From this point, power is distributed to the various locations where it is needed. Use the point of distribution as a star point.

CAUTION

Do not distribute power in a daisy-chain manner. Doing so causes the quality of the power to deteriorate as the chain moves from power consumer to power consumer.

6.4.2 Connecting Multiple Devices

For the reasons described in Section 6.4.1, use a star point approach when distributing power to multiple devices. Consider how much decoupling is required. To ensure good decoupling, power must first pass the footprint of the decoupling capacitor and then continue to the power input. Even the smallest stub from the power track to the capacitor significantly degrades the effect of the capacitor. To ensure the best possible performance from the capacitor, ground the capacitor with a solid connection to the same ground as the high-power device.

6.4.3 Connecting Multiple Pins on a Single Device

When connecting multiple pins on a device, assess the amount of decoupling. If in doubt, provide one capacitor per pin; however, this is not possible in every case. Make groups of pins that can share decoupling, route the power from the point of distribution to the decoupling capacitor, and route from the pins to the decoupling capacitor to create a common star connection at the decoupling capacitor. This prevents the different balls from affecting each other by injecting ripple/noise. Do not make interconnections between parallel balls other than at the decoupling capacitor.

6.4.4 Routing of Balanced Signals

Signals that must be balanced must be routed in parallel: the same distance from start to end, the same impedance for both signals.

Examples of balanced signals:

- MICMAIN.P – MICMAIN.N
- MICSUB.P – MICSUB.N
- HSMIC.P – HCMIC.P

6.4.5 Special Considerations for Ground for Microphone

The analog microphone biases (MICBIAS1, MICBIAS2, and VHSMIC) use MICBIAS.GND as the reference ground. Therefore, this ground is sensitive and special considerations must be taken. To prevent noise on analog microphone output from disturbance in the ground plane, define a special restricted area, such as a plane where the microphone ground and MICBIAS.GND are connected:

- This plane can refer only to the AGND ball N15 on the TPS65950.
- This plane, which is a split in the ground plane, must not be shared with AVSS4.
- This plane cannot have coupling with other ground planes; restricted areas in neighbor layers are required.

7 Use of Tunnels for Signal Isolation

Tunneling or shielding in the PCB ensures signal integrity on sensitive signals. Tunneling is space-consuming in a PCB and must be used only on signals for which this is required.

The tunneling of signals must be made on a dedicated layer in the PCB on which the signals are routed. The signals are routed with unbroken ground on both sides, and the shield is formed by having ground on the PCB layers above and below the signals. The surrounding ground planes must be firmly connected with vias to ensure connection between the ground layers and to the main ground in the PCB. When using tunneling on signals, ensure that the signals are not accidentally exposed to other signals, especially HS digital signals.

7.1 Signals That Require Tunneling

The following signals require tunneling:

- MICP: Positive signal on the differential microphone input. Signal level is in mV range.
- MICN: Negative signal on the differential microphone input. Signal level is in mV range.
- HSMICN: Negative signal on the headset microphone input. Signal level is in mV range.
- XTAL: The connections to the 32-kHz crystal should also be tunneled. The 32-kHz oscillator is a low-power circuit; therefore, the connections to the crystal should be protected.
- 26 MHz: This signal is active only when the system is in active mode, but it is a higher-frequency clock that can degrade other signals or cause system clocking issues if the clock signal is not clean. It is recommended to route the signal in a tunnel.

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